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# DDR2 SDRAM on the ColdFire MCF5445*x* Microprocessor

## Designing for power and performance with DDR2 on ColdFire

by: John Weil
Microcontroller Division

## 1 Introduction

The ColdFire® microcontrollers and microprocessors support numerous memory technologies. The MCF5445*x* family adds DDR2 to an already comprehensive list of SDRAM memory support in the ColdFire family, bringing DDR2 memory into the embedded market space with a high performance, cost effective, and low power embedded controller. This V4m-based ColdFire uses DDR2 memory to lower system cost, minimize energy usage, and maximize performance by leveraging the advantages of DDR2 in today's embedded system designs. The MCF5445*x* family, combined with DDR2 memory technology, is well-suited for a range of products where price, performance, and overall power consumption are key selection criteria.

The MCF5445*x* embeds a new V4m core, which includes a memory management unit, with a rich set of integrated features such as Ethernet, USB, serial memory boot, audio support, DSP acceleration, a cryptography acceleration coprocessor, and a PCI controller.

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This application note helps hardware and software engineers understand how DDR2 memory can have a positive impact on embedded system design. A quick overview of DDR2 memory advantages and disadvantages is provided, followed by a software and hardware overview that shows how simple it is to incorporate DDR2 memory in any embedded design.

# 2 DDR2 Overview

DDR2 memory has quickly become a commodity memory for the PC and PC peripheral industry. It is the next generation in double data rate synchronous memory technology and is specified by the JEDEC JESD79-2C standard. DDR2 memory was created to extend the frequency range of DDR memory technologies to much higher levels and also to reduce the amount of energy that is consumed by DDR memories.

The SDRAM companies accomplished this speed improvement and net power savings by making some fundamental architecture changes and introducing new I/O signaling that better supports higher frequencies. The frequency improvement provides little benefit to the embedded customer, as most embedded systems are not pushing the upper limit of DDR memory, but the new power saving features do provide significant benefits. The embedded designer now has access to a commodity SDRAM with high performance and low voltage (1.8V) I/O to help minimize energy usage in the system. This means output drivers can be sized to accomplish the same speed targets as 2.5-V DDR, but with reduced voltage swing and subsequently lower I/O power, without the need to use LPDDR (mobile DDR).

## 2.1 DDR2 Power Savings

The DDR2 standard achieves significant energy savings by implementing several architectural changes to the SDRAM array, while maintaining the same performance level as DDR. The DDR2 memories implement a 4n-prefetch internal bus, compared to the 2n-prefetch of DDR, which allows the SDRAM's internal array to be accessed by a bus that is four times wider than the external bus. For example, a 16-bit wide DDR2 memory uses a 64-bit wide internal bus to access the core array. This allows the core array in a DDR2 memory to be clocked slower than the equivalent DDR memory, which considerably reduces dynamic power (dynamic power utilization is due to switching losses of logic and memory cells). The prefetch architecture takes this 64-bit fetch and loads it into four 16-bit prefetch buffers. During the DDR2 burst cycle these four registers are selected by the column addresses. The DDR2 memory realizes the majority of its energy savings by combining this prefetch architecture with low voltage I/O. Like other SDRAM memory architectures, DDR2 also incorporates several power-down features, and includes support for partial array self-refresh found in LPDDR (mobile DDR).

This design has a few drawbacks, DDR2 memories support only two burst modes compared with the three modes of DDR. The burst sequences are also changed and this affects how a processor accesses data at misaligned (non-burst) boundaries. DDR2 memories have two options for burst length (4 or 8), and because the prefetch architecture is 4n-based any non-burst aligned access causes a wrap on a 4-bit boundary ($2^2$). DDR2 memories also have a new JEDEC minimum frequency of 125 MHz or 8 ns, as compared to 83 MHz for DDR.

# 3 ColdFire Implementation of DDR2

This section reviews how the MCF5445*x* implements support for DDR2.

## 3.1 ColdFire Internal Architecture and DDR2

The ColdFire architecture supports a variety of internal bus implementations. The V4m core used in the MCF5445*x* has a 16-byte cache line, which translates to four 32-bit transactions (data beats) on the internal bus. The DDR/DDR2/mobile-DDR controller supports converting these 32-bit transactions into 16-bit double data rate transactions on the external bus. This allows the external bus to run at the same clock rate as the internal bus, but with a reduced number of I/O pins, which allows the MCF5445*x* to have a lower pin count, and still maintain full internal bus performance.

DDR2 mode in the memory controller adds support for the 4n-prefetch feature for DDR2 memories. This allows the ColdFire core to perform critical word-first fetches from DDR2 memories when the cache controller detects a miss. Subsequently, this minimizes instruction fetch delays by allowing the core to fetch the desired instruction and the DDR2 memory and controller to finish the cache line fetch by wrapping on the 4-bit boundary. Please see Figure 1 for an example of misaligned (critical word first) fetches and how they can differ from DDR fetches. With a 16-bit external bus, the burst length for the MCF5445*x* should be set to eight, as each data beat on the external bus only produces two bytes of data.

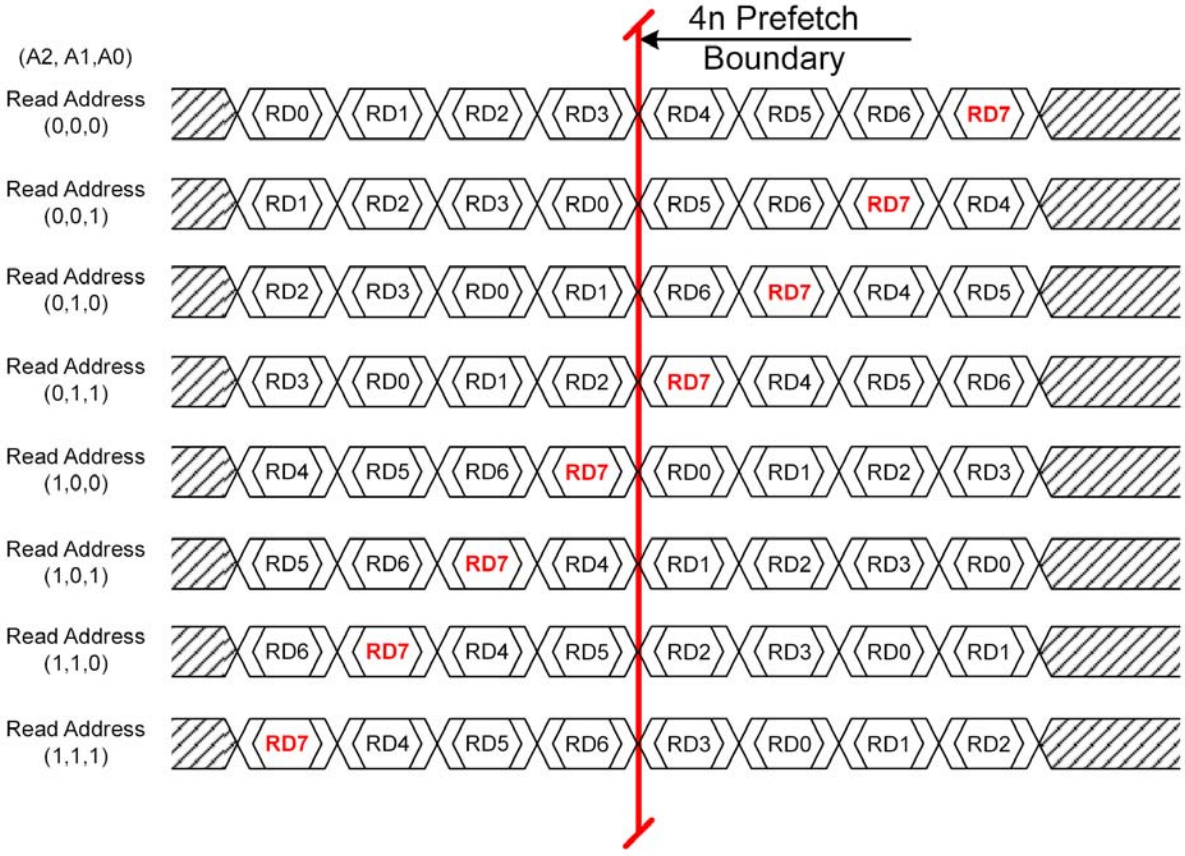


**Figure 1. 16-Byte Fetch on DDR2: Using 4n-Prefetch**

The MCF5445*x* adds new register fields, beyond previous DDR controllers in the ColdFire family, that must be used when implementing a DDR2 solution. DDR2 memories also incorporate some technology that is not used by the ColdFire memory controller, such as ODT (on-die-termination) and support for eight internal banks. Please review Table 1 for more details on supported and unsupported features.

The memory controller on the MCF5445*x* family includes support for up to 512 MB of DDR/DDR2/mobile DDR memory, using 25 address bits (row and column combined), two bank select bits, two chip selects, and a 16-bit wide bus.

**Table 1. DDR2 Feature Implementation Guide**

| DDR2 Feature/Option | MCF5445*x* Memory Controller | Implementation Notes |
|---|---|---|
| 1.8 V I/O Support | YES | Drive strength and mode set in MSCR_SDRAM register |
| Densities | Less than 1Gb in DDR2 per chip | Two chip selects for max of 256 MB in DDR2 and 512 MB in DDR and mobile DDR |
| DDR2 Memory Banks | 4 Banks YES | DDR2 memory offers an eight bank version. This is not supported. |
| 4n-Prefetch | YES | Correct burst sequence support for burst of 8. Critical word first support included. |
| Speed | 133 MHz Maximum | |
| READ Latency & Additive Latency | YES | SDCFG1/2 registers configure READ latency plus additive latency. |
| WRITE Latency | YES | SDCFG1/2 registers configure WRITE latency |
| Termination (On-Die/Motherboard) | Motherboard | SSTL1.8 support using on-board parallel termination. In limited cases, parallel termination may not be needed. |
| Data Strobes (Differential/Single-Ended) | Single-Ended | Maximum clock rate of 133 MHz does not require differential and saves energy. |
| Module Support | 144-pin DDR2 16-bit SO-DIMM | 16-Bit DDR2 SODIMM is JEDEC ratified and is available for purchase |

# 3.2 Programming Model for DDR2 Functionality

## 3.2.1 SDRAM Mode/Extended Mode Register (SDMR)

This register has changed from previous controllers, and the low order address bits of this register now have LMR/LEMR (load mode register/load extended mode register) capability. It still works in the same manner as previous generations, but now includes the option to use the low 14 bits of this register to issue DDR2 specific LMR/LEMR values. Please see the “SDRAM Mode/Extended Mode Register (SDMR)” section in the *MCF54455 Reference Manual* for more information. The SDRAM control register (SDCR) contains a DDR2_MODE bit, which must be set to enable the LMR and LEMR functionality in the SDMR register.

### 3.2.2 SDRAM Control Register (SDCR)

This register has only minor changes from previous controllers, as it adds the enable for DDR2 mode. This register controls the address multiplexing, refresh count, and operating modes of the memory controller. Please see the “SDRAM Control Register (SDCR)” section in the *MCF54455 Reference Manual* for more information. For summary purposes the features of this register are listed below.

- Capability to lock SDMR register and prohibit write cycles. This bit is used only during configuration/initialization routines or when access is required to the mode or extended mode registers in the DDR memories.
- CKE enable bit allows memories to be placed into self-refresh or power-down modes. Typically only used during chip initialization and for power management of DDR memories. This enable bit gives direct control over the state of the CKE signal from the MCF5445*x*.
- DDR2 mode bit allows selection of DDR or DDR2 memory. This bit must be set for DDR2 functionality to work.
- DDR mode bit must be set. The reset value of 0 is reserved.
- Refresh enable activates the automatic refresh capability of the memory controller.
- Address mux changes the linear address inside the ColdFire device to a multiplexed address of rows, columns, and banks. Please see the tables in the SDRAM controller’s “Supported Memory Configurations” section in the *MCF54455 Reference Manual*.
  - The first table provides a simple view of how the internal addresses are changed to external rows or columns based on the address mux setting.
  - The second shows how to configure the address mux setting based on memory density and configuration (row, column, bank).
- Drive rule selection is a useful feature, but not commonly used. This feature forces the DQ (data signals) and DQS signals to drive at all times, except during a read cycle when the DDR memories drive the bus. If this bit is set, the DQ lines drive the last state when the bus cycle completes, and the DQS signals drive low. When a read cycle starts, the memory controller tristates both DQ and DQS to allow the memories to drive the signals.
  This is typically used for a minimal system to minimize floating signals and possibly remove termination. This feature can also be used to debug a DDR bus, since it provides a deterministic state with no floating levels and is helpful when looking for shorts or other situations that might cause bus contention.
- Refresh count configures the refresh interval when the controller’s auto-refresh is enabled.
- Memory port size bit must always be set for the MCF5445*x* family.
- DQS output enable field disables/enables individual DQS signals. This is only important if the selection of memory devices causes only one DQS to be needed to drive the memories. This is not the typical scenario. Typical scenario is to use one DQS for each byte lane. If only one DQS is used, short the DQS to both DQS pins on the MCF5445*x*, as the clock recovery circuits in the MCF5445*x* still need to see DQS edges on both byte lanes during read cycles.

- Initiate refresh command causes an immediate refresh. This is most commonly used during initialization and power management routines, where the memories require specific events to occur and refresh commands must be issued. This feature is only available when the mode/extended mode register is enabled.
- Initiate precharge all command forces a software-initiated precharge. The clock enable (CKE) must be enabled before issuing a software precharge command.
- Deep power-down mode bit generates a deep power-down command for mobile DDR devices. It is not supported on DDR2 devices, so clear this bit.

### 3.2.3 SDRAM Configuration Register 1 & 2 (SDCFG1/SDCFG2)

The SDRAM configuration registers store the required delay values between specific memory commands. Each DDR memory manufacturer has provided values on their data sheets for each of these delays. These values must be converted into appropriate delay values (typically clock cycles) and loaded into the SDCFG1/2 registers.

## 3.3 DDR2 Sample Initialization

The following pseudo-code illustrates DDR2 initialization using the M54455EVB. The M54455EVB features 256 MBytes of DDR2, using four 8-bit wide Micron MT47H64M8 (512-Mbit) devices, configured as two 16 M × 8 × 4 banks per memory controller chip select.

**Example 1. Pseudo-code for DDR2 Initialization**

1. Setup the MSCR register to use SSTL 1.8V I/O for DDR2 on all memory controller pins:

```
writemem.b 0xFC0A4074 0xAA              ; MSCR_SDRAM
```

2. Setup the memory controller chip selects for 128 Mbytes each.

```
writemem.l 0xFC0B8110 0x4000001A        ; SDCS0

writemem.l 0xFC0B8114 0x4800001A        ; SDCS1
```

3. Setup the required memory vendor's delays for various DDR commands

```
writemem.l 0xFC0B8008 0x65311810        ; SDCFG1
```

   – SRD2RWP = 0x6 = Burst Length / 2 + 2
   – SWT2RWP = 0x5 = CAS + Additive Latency + $t_{wr}$ – 1 = 3 + 1 + (15 ns/7.5) – 1
   – RD_LAT = 0x3 = CAS Latency in clock cycles
   – ACT2RW = 0x1 = ($t_{RCD}$ / $t_{CLK}$) – 1 = (15 ns /7.5 ns) – 1 = 1 clock cycle
   – PRE2ACT = 0x1 = ($t_{RP}$ / $t_{CLK}$) – 1 = (15 ns/7.5 ns) – 1 = 1 clock cycle
   – REF2ACT = 0x8 = ($t_{RFC}$ / ($t_{CLK}$ x 2)) + (1 for math rounding) = (105 ns / 15 ns) + 1 = 8
   – WT_LAT = 0x1 = Additive Latency = ($t_{RCD(min)}$ / $t_{CLK}$) – 1 = 15 ns/7.5 ns – 1 = 1

```
writemem.l 0xFC0B800C 0x59670000        ; SDCFG2
```

   – BRD2RP = 0x5 = Burst Length / 2 + Additive Latency = 8 / 2 + 1 = 5
   – BWT2RWP = 0x9 = CAS Latency + Additive Latency + Burst Length / 2 + $t_{WR}$/$t_{CLK}$ – 1 =

3 + 1 + 4 + 2 – 1 = 9

- BRD2W = 0x6 = Burst Length / 2 + 2 = 6
- BL = 0x7 = Burst Length – 1 = 7

4. Delay (DDR2 memories have a delay requirement, typically 200 µs.) A delay should be included in the initialization sequence before going to next step, which asserts CKE.

```
writemem.l 0xFC0B8004 0xEA0F2002        ; SDCR
```

- Set mode enable (1)
- Enable CKE (1)
- Enable DDR Mode (1)
- Disable automatic refresh (0)
- Enable DDR2 Mode (1)
- Configure address mux to (10) = 512 Mbits configured as 14 × 10 × 4 and 8-bit wide
- Drive rule set to tri-state mode between reads and writes. Board uses parallel termination.
- Refresh count set to 0xF which means (8k / (7.5 ns × 64)) – 1 = 15. This value is always rounded down, as refreshing slightly more often than required is the goal.
- Memory port size is set to 16 bits
- DQS outputs are still disabled
- Issue pre-charge all command
- Deep power down is not used during initialization sequence

```
writemem.l 0xFC0B8000 0x40010408        ; SDMR
```

- Write extended mode register command for non-mobile DDR
- Set CMD bit to issue load extended mode command
- Set extended mode: DLL is enabled, full strength output drive, internal parallel termination is disabled, posted CAS (additive latency) of 1, OCD not supported, differential DQS disabled, RDQS disabled, outputs enabled.

```
writemem.l 0xFC0B8000 0x00010333        ; SDMR
```

- Write mode register command
- Set CMD bit to issue load mode register command
- Set mode register contents: burst length of 8, sequential burst mode, CAS latency of 3, normal mode, DLL held in reset, write recovery set to 2, and power down set to fast exit mode.

5. Delay 200 memory clock cycles before issuing the pre-charge all command in the next step

```
writemem.l 0xFC0B8004 0xEA0F2002        ; SDCR, issue PALL
```

- Same as last SDCR write, which effectively issues another pre-charge all command

```
writemem.l 0xFC0B8004 0xEA0F2004        ; SDCR
```

- Same as last SDCR write but now issue a refresh command

```
writemem.l 0xFC0B8004 0xEA0F2004        ; SDCR
```

– Issue another refresh command

```
writemem.l 0xFC0B8000 0x00010233        ; SDMR
```

– Same as last mode register write, except the DLL reset is removed and the DLL is allowed to lock

```
writemem.l 0xFC0B8004 0x7A0F2C00        ; SDCR
```

– Clear mode enable to lock-out from further SDMR register write cycles, enable self refresh, enable DQS signals, and everything else stays the same

— Delay 200 bus clocks after DLL reset is removed.

## 3.4 DDR2 Hardware Design Considerations

This section provides the embedded hardware engineer with all the necessary information to use DDR2 memory with the ColdFire MCF5445*x* family in a simple and efficient manner. The MCF5445*x* memory controller and SSTL I/O are very flexible and give the hardware designer quite a bit of design freedom. A very important concept for all embedded designers is to understand that DDR2 specifications were written for the desktop/notebook/server market and have little directed information for an embedded hardware designer. Many of the DDR2 hardware guidelines that are available on the web can generate extra cost for the embedded designer.

This section reviews the M54455EVB's DDR2 implementation and shows an ideal scenario and some areas for cost improvement or system reduction. By using the content in the following sections, the embedded hardware designer should feel comfortable that DDR2 is an easy, effective, and viable choice to use with ColdFire in a high-performance/low-power embedded platform.

### 3.4.1 DDR2 Package and Layout Considerations

One of the key differences between DDR2 and other DDR solutions is the package. DDR memories are available in TSOP and BGA packages, but DDR2 is only available in the FBGA package. The advantages of this package are its signal quality and small, efficient board footprint. It does make manual debug a bit more difficult, but this can be solved using through-hole vias that give access to signals on the bottom of the board.

The M54455EVB uses four x8 Micron MT47H64M8 memories. The small size and ideal signal placement for address, control, and data make the layout of this board very simple. The M54455EVB takes advantage of populating components on the top and bottom of the board. This is not a requirement to implement a DDR2 solution, but it does result in a clean and efficient configuration. See Figure 2 for a diagram of a DDR2 x8 memory using the FBGA signal layout.

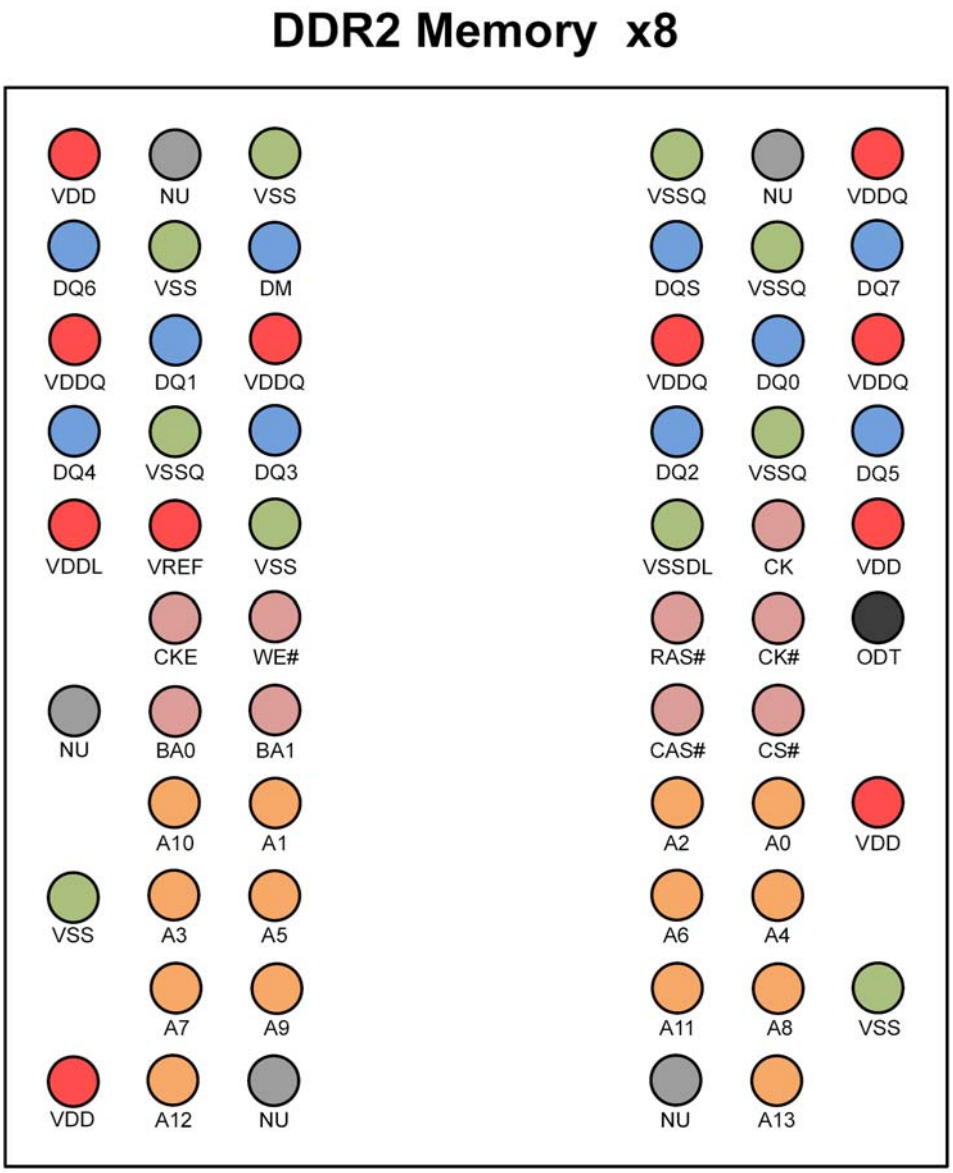


**Figure 2. Example DDR2 Memory Configuration x8 (View Through Package)**

In Figure 2 it is easy to see how to escape the signals from the BGA. The data lines are located toward the top, the control lines are in the middle, and the address lines are located at the bottom of the package. The physical placement of the spheres on this package permits a simple routing path down the middle of the package. This gives the layout designer a clear path to access the various sections, and it allows easy segmentation of the address from control signals.

Freescale took advantage of this escape pattern and the ability to place chips on the top and bottom of the board. By placing two DDR2 memory chips directly above and below the board, the signal integrity is ideal and the routing is very clean.

The actual floorplan of the M54455EVB's DDR2 bus is shown in Figure 3. From left to right:

- The MCF54455 processor in the middle of the board
- A set of series terminators
- Three logic analyzer connectors
- The DDR2 memories
- The VTT resistor packs

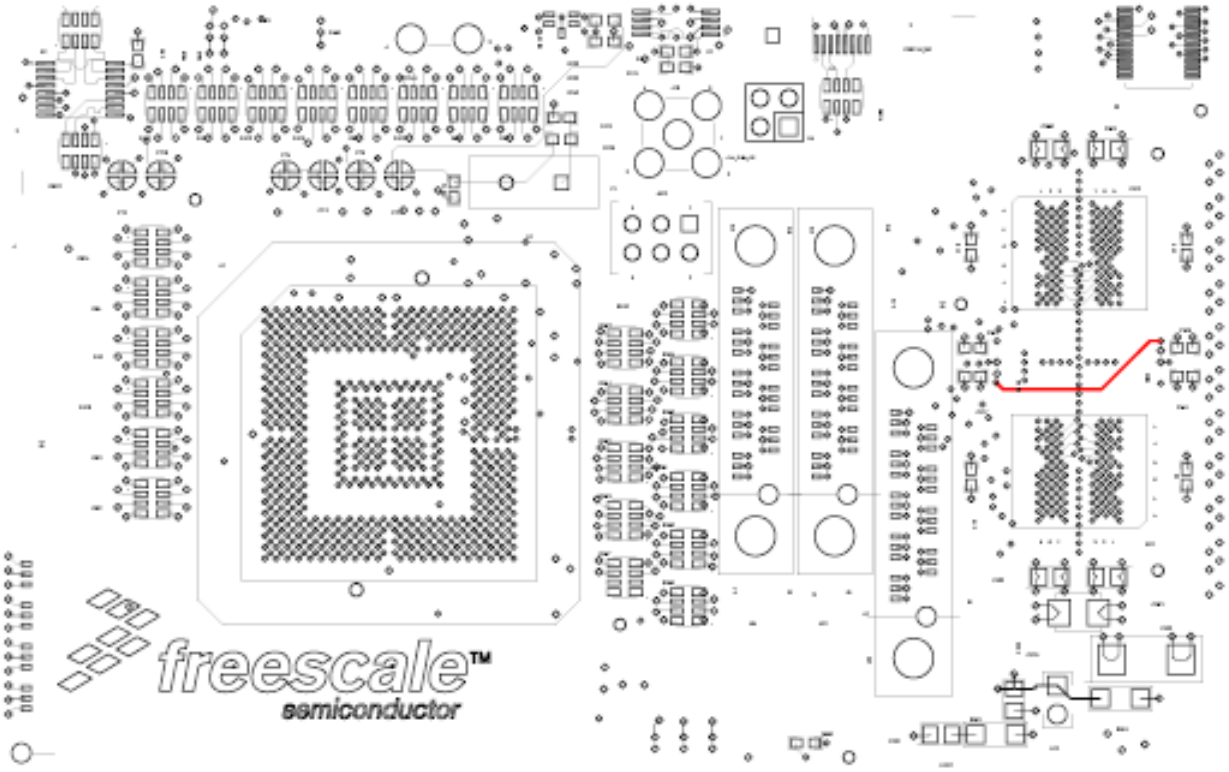


**Figure 3. Top Layer of U1 (MCF54455) to DDR2 Memories**

The address bus is routed from the ColdFire device to the vias located half way between the two sets of memory chips. This permits a clean route to the address bus located on both ends of the memory chips. Figure 4 show how the address bus routes to these vias, and then forms a T-junction to the two sets of DDR2 memories. Figure 4 also shows an example of data lines that are coming in from the top and bottom of the DDR2 memories. Again, the routing of address in the middle supports a T-junction with equal length stubs going to each DDR2 memory. The data buses come from the left and connect to the ends of the DDR memories. Each of the data bus sections (each byte lane) are routed to a set of vias that provide a T-junction to the two memories on that byte lane. The vias are visible in Figure 4 and are located in the wide channel between the left and right sections of the BGA.

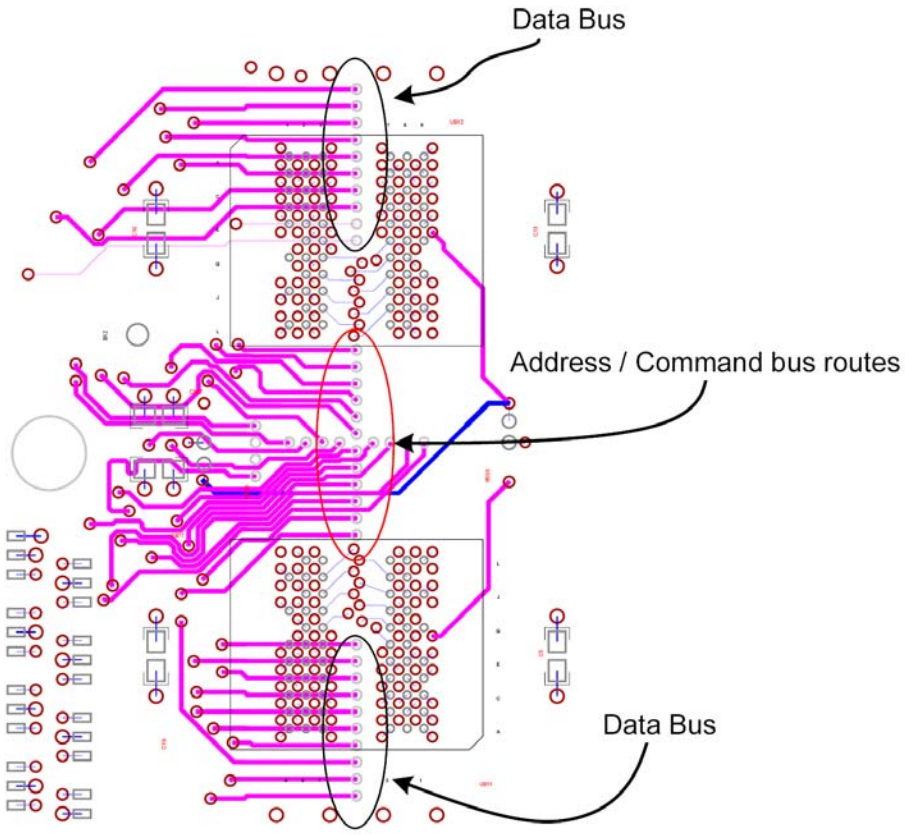


**Figure 4. Address Bus T-Junction**

The logic analyzer connectors can be one of several new styles that are offered by various test and measurement companies. The version used on the M54455EVB board are designed for use with Tektronix P6860/P6880 probes. Traditional Mictor connectors do not have the signal fidelity that is typically required for higher speed signals (edge rate being the most critical factor not frequency). The SSTL pads on the MCF5445*x* and the DDR2 memories are too fast for standard mictor connectors. The new high speed logic analyzer connectors are very useful, because they have a minimal affect on signal quality when a logic analyzer is not present.

## 3.5 DDR2/ColdFire Trace Routing Guidelines

The most common type of DDR trace routing is a series/parallel termination scheme using a 50-ohm transmission line model. This scheme is used on the M54455EVB, and is easy to see in Figure 3. Looking left to right, the series resistors are located very close to the ColdFire processor, and the parallel termination resistors are located just to the right of the DDR2 memories. The following are key concepts for the series/parallel termination scheme and how it is applied to DDR/DDR2 board designs:

- Series terminators must be placed close to the source driver. This example uses single series termination. This means that only one set of series terminators are used, and they are placed next to the ColdFire processor. A dual series termination scheme can be used, but is rarely necessary in embedded systems. Dual series termination is the least common scheme in the embedded memory world.

- Parallel terminators should be placed close to the memories. Again, a dual parallel scenario can be used, but in typical situations would be overkill for embedded applications.
- Always make sure the distance from the series terminator to the source output driver is much shorter in length than the distance from the series terminator to the load (DDR memory).
- DDR2 series/parallel termination requires a VTT voltage supply. VTT is always half of the DDR2 memory voltage. In this example, VTT is 0.9 V for a 1.8-V DDR2 memory system.
- VREF must be supplied, as SSTL input buffers are differential in nature.
- $R_S$ should be sized such that the output impedance of the driver plus the resistor is roughly the same as the line impedance. On the MCF5445*x*, a starting point that produces good results is 22-Ω series resistors. Depending on the layer stack-up and material used, the desired size of $R_S$ can vary from less than 22 Ω to 33 Ω.
- $R_P$ is typically sized based on the drive currents used in the system. On the M54455EVB, 51-Ω resistors were chosen. In DDR2 mode, the MCF5445*x* only supports one output drive level for SSTL18 (SSTL18 is an SSTL pad at 1.8v).
- Figure 5 shows an example series/parallel termination scheme used most commonly for address, data, and command signals.

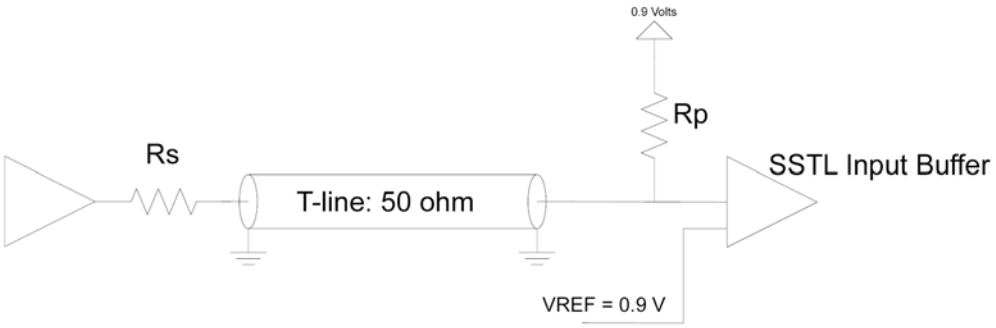


**Figure 5. SSTL Series/Parallel Termination Scheme for Address/Data/Command**

- DDR/DDR2 clocks are differential and the MCF5445*x* provides a clock output and the complement of that clock. These two signals must be routed together with matched impedance as a differential pair with design rules set between 100- and 120-Ω differential impedance.
- Differential clocks can be terminated with a single resistor between the two phases of the clock. See Figure 6 for an example of this parallel termination scheme, which produces excellent clock crossovers and reduces the number of components needed. One key item to consider is that all DDR/DDR2 DIMMs include this single parallel terminator (between clock phases) on each DDR DIMM module. If a design contains on-board DDR2 memories and a slot for a DDR2 DIMM module, it is strongly recommended that a separate clock pair is routed to the on-board memories and to the DDR/DDR2 DIMM.

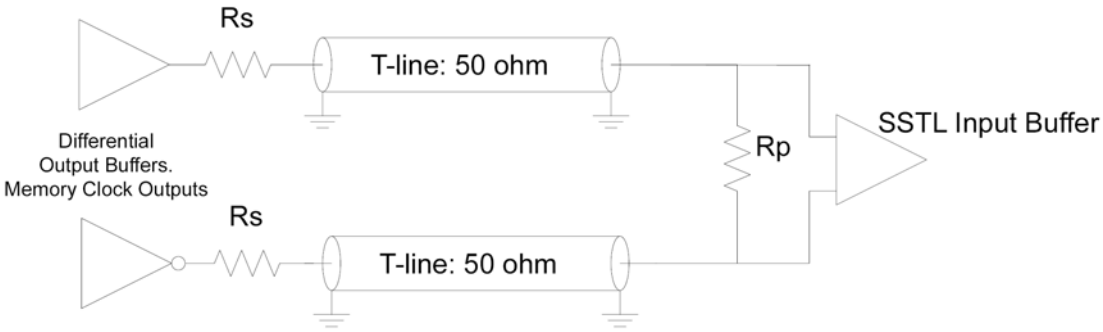


**Figure 6. SSTL Clock Parallel Termination—Alternate Method**

## 3.6 Sample Connection Diagram

Figure 7 shows an example diagram for connecting the MCF5445*x* DDR2 controller to a DDR2 memory. The connections are very straightforward, as the DDR2 bus on the MCF5445*x* family is not multiplexed with other buses. MCF5445*x*'s dedicated pinout maximizes performance and simplifies connectivity.

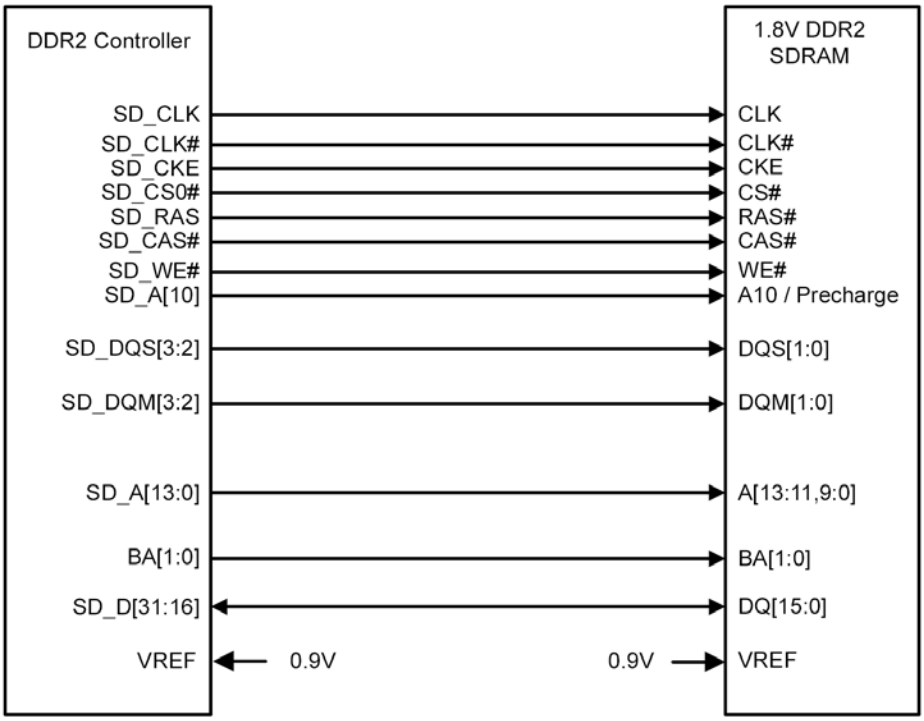


**Figure 7. Example Connection Diagram for DDR2**

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**Home Page:**
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**E-mail:**
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Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
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**Europe, Middle East, and Africa:**
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Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
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+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

**Japan:**
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

**Asia/Pacific:**
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
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