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Migrating from the MC68332 to the ColdFire® MCF523*x*

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Leveraging the widespread industry success of Motorola's 68K family, the ColdFire® architecture is designed specifically to provide higher performance in embedded applications at a lower cost. Since the ColdFire architecture stems from the Freescale 68000 architecture, it allows designers to take advantage of the established tool support, code evolution, and engineering expertise. This architectural relationship encourages users to migrate from 68K to ColdFire, the next high-performance, highly integrated generation of the 68K family of processors.

This application note describes what designers and engineers would consider when migrating from the 68K family to the ColdFire family. Specifically, this application note focuses on the migration from the MC68332 to the MCF523*x*. For additional information about the MCF523*x* Family, refer to the *MCF5235 Reference Manual* (MCF5235RM/D).

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This document organizes the differences between these two devices into two major categories: hardware and software. Specifically, this document:

- Examines parametric differences, i.e., electrical parameters that specify the conditions under which the device must operate, and discusses performance and power requirements
- Compares mechanical characteristics, in particular, packaging and external signals
- Examines on-chip modules, contrasting shared modules, and introducing modules not found on the MC68332
- Discusses operating modes and how they are entered

Throughout each of the following sections, there will be frequent references to more detailed information, as this application note is not intended to be an all-encompassing reference for either of these two devices or families. A list of all suggested references is given at the end of this document.

To locate any published errata or updates for this document, refer to the web site at http://www.freescale.com/coldfire.

1 Comparison Overview

Many current users of the MC68332 will find several advantages in migrating to the MCF523*x*:

- Increases in device performance and functionality, including expanded on-chip memory size for both static RAM and cache
- Enhancement of core architectural features and ability of the core's register set, inherent execution control, and instruction set to support efficient code execution in an embedded application
- Improvements in system control capabilities, such as memory/module access control

Migration from the MC68332 to the MCF523*x* includes the following increases in device performance and functionality:

- Maximum CPU operating speed increases from 25 MHz to 150 MHz
- Maximum system bus frequency tripling from 25 MHz to 75 MHz
- On-chip SRAM memory increases from 2 Kbytes to 64 Kbytes
- Addition of 8 Kbytes of configurable instruction/data cache RAM for faster code execution
- Upgrade from 16-channel Time Processor Unit (TPU) to 32-channel enhanced Time Processor Unit (eTPU) with dual action on each channel
- Upgrade from 200 Bytes on the TPU to 1.5 KBytes Shared Parameter RAM (SPRAM) on the eTPU
- Upgrade from 2 KBytes on the TPU to 6 KBytes Shared Code Memory (SCM) on the eTPU
- Full-function asynchronous communication with three Universal Asynchronous Receiver/Transmitter (UART) modules, rather than limited handshaking functionality of the MC68332's Serial Communication Interface (SCI) module
- Addition of several modules:

- 10/100 Fast Ethernet (media access) controller (FEC)
- Controller Area Network (CAN) controller
- I^2C communication controller
- 4-channel Direct Memory Access controller (DMA)
- 4 DMA-supported 32-bit timer modules
- Synchronous/asynchronous Dynamic Random Access Memory (SDRAM) controller
- Optional hardware cryptography accelerator modules

The MCF523*x* core includes the following:

- Version 2 ColdFire core providing up to 144 Dhrystone 2.1 MIPS at 150 MHz
  - Processor core runs at twice the bus frequency
  - Implements the ColdFire Instruction Set Architecture, ISA_A+, with extensions to support the user stack pointer, and four new instructions for improved bit processing
  - Illegal instruction decode that allows for 68K emulation support
- System debug support
  - Background debug mode (BDM) for in-circuit debugging
  - Real time debug support, with two user-visible hardware breakpoint registers (PC and address with optional data) that can be configured for a 1- or 2- level triggered
  - Real time trace for determining dynamic execution path
  - New fully-integrated eTPU debug support. This provides access to the eTPU debug registers via the standard ColdFire BDM serial interface or the processor WDEBUG instruction and run/halt triggering capability between eTPU and ColdFire BDM.
- The MCF523*x*'s Enhanced Multiply-Accumulate controller (EMAC) unit provides a common set of simple DSP operations, and speeds the execution of the integer multiply instructions for both signed and unsigned operands in the ColdFire core.
  - Multiplies of 16x16 and 32x32 with 32-bit accumulates are supported. The EMAC unit is tightly coupled to the Operand Execution Pipeline (OEP) and features a four-stage execution pipeline.
  - The OEP can issue a 16x16 multiply with a 32-bit accumulation and fetch a 32-bit operand in the same cycle.
- A hardware divide module is also coupled to the core's OEP, which allows the processor to support signed divides, unsigned divides, and remainder instructions.

System control options and capabilities offered in the MCF523*x* are the following:

- A base address register that provides relocation of internal resources
- Two interrupt controllers that support seven programmable interrupt levels for internal peripheral interrupts and seven external interrupt pins; each interrupt level has eight programmable and one fixed priority levels
- A software watchdog timer to prevent erratic operation caused by runaway code execution

- Seven types of resets, including low power supply voltage detection, and a status register to indicate the cause of last reset
- Up to eight chip selects with programmable wait states, port sizes, and transfer burstability on reads or writes, as well as support for paged mode Flash memories
- Module access control, including read/write access in either user or supervisor mode, for on-chip modules
- Bus master arbitration and prioritization for three on-chip masters (core, FEC, and DMA controller)

Table 1 provides a brief look at the design considerations and benefits of migration from the MC68332 to the MCF523*x*. It also provides a page reference to the detailed description of the specific migrating issue.

Table 1. MC68332 to MCF523*x* Migration Issue Summary

Device Feature	Device Implementation					Impact		Migration Criticality	Page Number
	MC68332	MCF5235	MCF5234	MCF5233	MCF5232	Hardware	Code		
CPU Core	CPU32	V2 ColdFire				√	√	High	25
CPU Frequency	25 MHz	150 MHz				√	√	Low	6
Performance	7.5 MIPS	144 MIPS				—	√	Low	6
System Frequency	25 MHz	75 MHz				√	√	Low	6
Voltage	5.0V	3.3V I/O, 1.5V Core				√	—	Medium	5
Packaging	144 LQFP, 132 PQF	256 MAPBGA			160 QFP, 196 MAPBGA	√	—	High	6
SRAM Size	2 Kbytes	64 Kbytes				—	√	Low	12
Instruction/Data Cache Size	—	8 Kbytes				—	√	Low	18
Time Processing Unit Channels	16-channel TPU	16 or 32-channel eTPU	16-channel eTPU	32-channel eTPU	16-channel eTPU	√	√	High	11
TPU Memory SPRAM/SCM	200bytes/ 2kbytes	1.5Kbytes/ 6 Kbytes				—	√	Medium	11
External Interrupt Pins	7	7			7 (MAPBGA) 3 (QFP)	√	√	Low	16
Chip Selects	12	Up to 7				√	√	Low	
SDRAMC	—	Up to 2 blocks				√	√	Low	19
DMA	—	4 channel				√	√	Low	19
Serial Communication	1 SCI	3 UARTs				√	√	Medium	13
	QSPI	QSPI				√	√	Medium	14
	—	I^2C				√	√	Low	20
Ethernet	—	√	√	—	—	√	√	Low	18

Table 1. MC68332 to MCF523*x* Migration Issue Summary (continued)

Device Feature	Device Implementation					Impact		Migration Criticality	Page Number
	MC68332	MCF5235	MCF5234	MCF5233	MCF5232	Hardware	Code		
CAN	—	2 FlexCAN	1 FlexCAN	2 FlexCAN	1 FlexCAN	√	√	Low	19
Crypto	—	√	—	—	—	—	√	Low	20
WDT	√	√	√	√	√	—	√	Low	15
PITs	1	4	4	4	4	—	√	Low	14
32-bit DMA Timer	—	4	4	4	4	√	√	Low	21

2 Device Differences

This section addresses differences between the MC68332 and the MCF523*x*, and highlights what the user needs to consider when making this migration. The categories discussed in this section include electrical characteristics, mechanical characteristics, on-chip modules, and memory maps.

2.1 Electrical Characteristics

The following sections discuss differences in electrical characteristics between the two devices, including voltage conversion, driver strength/capacitive loading, frequency and performance, and operating in 16-bit mode.

2.1.1 Voltage Conversion

One important consideration in migrating from the MC68332 to the MCF523*x* is the difference in voltage. The MC68332 is a 5V only device, while the MCF523*x* is a dual supply device—3.3V supply for I/Os and 1.5V supply for the core. In addition, the MCF523*x* I/Os are not 5V tolerant, so the memories and external peripheral devices used in an existing MC68332 system might not be compatible with the MCF523*x* bus without proper system design. Bulk memories are readily available in 3.3V, so finding replacements for memory devices should not present a problem. If any external peripherals that are only available as 5V devices are needed, then level shifters/buffers will be required to isolate the peripherals 5V I/Os from the MCF523*x*. Refer to Figure 2 for an example of how buffers can be used to isolate 5V memories and peripherals from a 3.3V bus.

2.1.2 Driver Strength/Capacitive Loading

Another issue to take into consideration when migrating from the MC68332 to the MCF523*x* is the drive capability of the parts. Whereas the majority of MC68332 specifications assume a capacitive load between 90-130pF on the pin, the MCF523*x* tolerates loading up to 25pF for low drive strength and 50pF for high drive. In many systems, external buffers will be needed to reduce the loading on the MCF523*x* bus. Figure 2 shows a possible buffering scheme that can be used to reduce loading. (Note: SDRAM should remain unbuffered.)

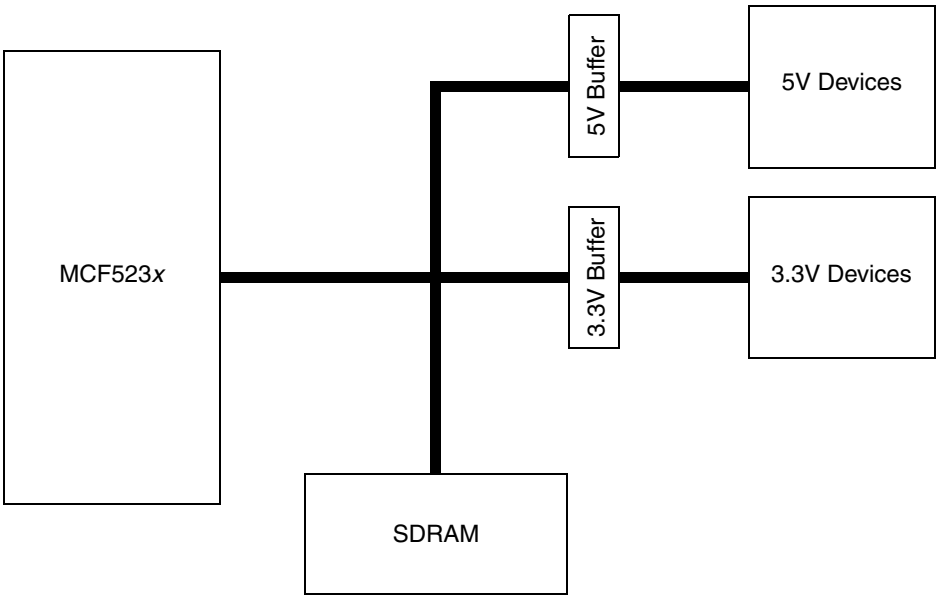

Figure 2. Buffering Scheme for Isolating 5V Memories and Peripherals on a 3.3V Bus

2.1.3 Frequency and Performance

One of the primary advantages of migrating to the MCF523*x* is the significant increase in performance and frequency. Whereas the MC68332 has a Dhrystone 2.1 MIPS rating of approximately 7.5 MIPS when running at 25 MHz, the MCF523*x* offers approximately 24 MIPS of performance at the same frequency. That is, the MCF523*x* offers over a 3x performance boost without changing the frequency. Moreover, the MCF523*x* can provide 144 MIPS performance at its maximum frequency of 150 MHz.

2.1.4 Operating the MCF523*x* in 16-bit Data Bus Mode

Unlike the MC68332, the MCF523*x* has a 32-bit external data bus. In order to maintain as much compatibility as possible with the MC68332, customers can choose to operate the MCF523*x* in a 16-bit data bus mode. At reset, if the boot port width is configured for an 8- or 16-bit port, then only the upper half of the data bus (D[31:16]) will be configured for data bus functionality; the lower half of the 32-bit data bus (D[15:0]) will default to GPIO pin functions. The lower data bus pins can be enabled as data bus pins later if needed.

2.2 Mechanical Characteristics

With the trend toward miniaturization, smaller, lighter, and higher performance products have paved the way for smaller component packages and higher pin counts. For this reason, the Mold Array Process-Ball Grid Array (MAPBGA) is used as the production package for the MCF523*x*. It is a surface mount package that uses solder balls arranged in a grid array instead of the lead pins normally used in Quad Flat Pack (QFP) and other packages. The MCF523*x*'s 256-pin and 196-pin MAPBGA packages give it many advantages over a QFP. For compatibility, the MCF5232 is also available in a 160-pin QFP; however, it is the only member of the MCF523*x* family available in a QFP package.

The most evident advantage of the MAPBGA versus the QFP is the savings in board real estate. Most BGAs are typically 20-25% smaller than their QFP counterparts. For the MAPBGA package, the entire surface of the die, rather than just the edges, can be used for interconnection. When the total board area required to place and route the package is taken into account, the MAPBGA can reduce size by as much as 50%. Figure 3 illustrates the differences between the QFP and the MAPBGA.

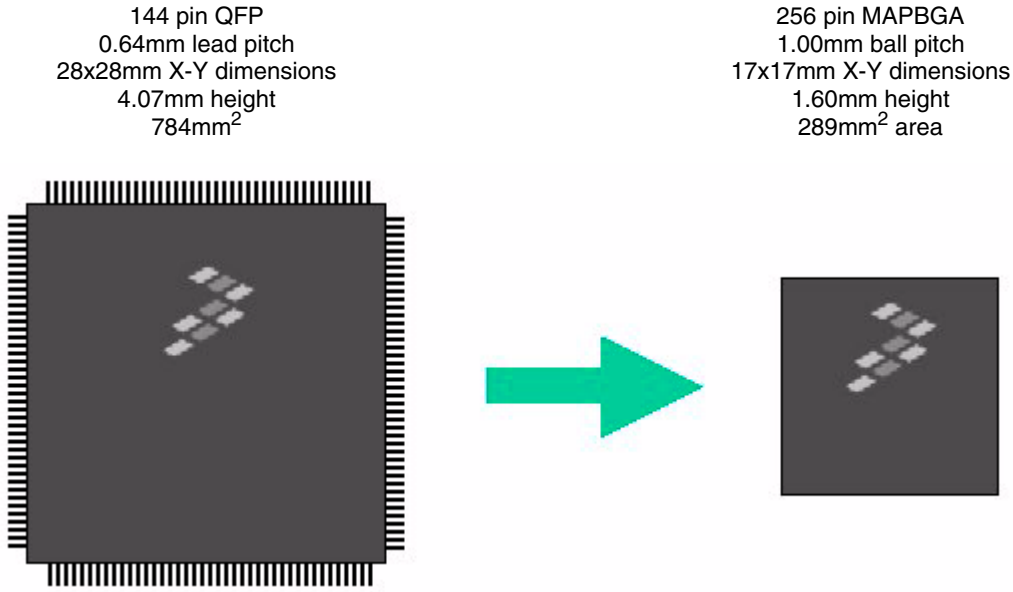

Figure 3. Customer Board Area Reduction Example

Lead pitch is a major consideration when working with high pin count QFPs. For these packages, the lead pitch can be as fine as 0.64 mm. The BGA package with the same number of pins is easier to mount, since the lead pitch is wider than a QFP package. BGAs are also less fragile and easier to handle both before and during assembly. The placement operation for this package is usually far easier and more reliable than for fine-pitch QFPs.

BGAs also have higher assembly yields. For example, BGAs typically have less than 5 parts per million joints (ppmj) compared to the 50–100 ppmj of QFP devices. BGAs have higher assembly yields than QFPs for the following reasons:

- No bent leads or coplanarity problems
- Self-aligning on solder pads
- Solder balls are always solderable (unlike plated leads)
- Easy solder paste printing
- Large pitch: 1.0 mm, 1.5 mm, 1.27 mm
- Large ball diameter sizes: MAPBGA 19.68 mils

In general, BGAs have better electrical and thermal properties than their QFP counterparts. The long fingers of the QFP lead frame make it more inductive than shorter ones. Additional enhancements can be made to the BGA package by adding metal layers for power and ground.

2.3 External Signal Comparison

Because of the devices' different packages, it is not useful to compare their pinouts. It is useful to discuss the commonality of signals brought out of each device. Table 1 is a summary of each device's externally-accessible signals.

Table 1. MC68332/MCF523*x* External Signal Comparison

Module	MC68332 Signal	MCF523*x* Signal	Comment
Reset	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	
	—	$\overline{\text{RSTOUT}}$	
Clocks	EXTAL	EXTAL	
	XTAL	XTAL	
	CLKOUT	CLKOUT	
	XFC	—	
Mode Selects	MODCK	CLDMOD[1:0]	
	—	$\overline{\text{RCON}}$	Reset configuration can be overriden via D[26:24, 21, 19:16]
	—	eTPU/$\overline{\text{EthENB}}$	Selects either upper eTPU channel or Ethernet functionality
	—	JTAG_EN	Can now select between JTAG and BDM functionality

Table 1. MC68332/MCF523*x* External Signal Comparison (continued)

Module	MC68332 Signal	MCF523*x* Signal	Comment
External Memory Interface	A[23:0]	A[23:0]	A[23:21] are muxed with CS[6:4] on the MCF523*x*; Please note that the MCF523*x* does not support E clock functionality, which is used for M6800-Type peripheral support.
	D[15:0]	D[31:16]	
	—	D[15:0]	These pins can be used as GPIOs on the MCF523*x* if a 32-bit data bus is not needed.
	DSACK[1:0]	BS[3:0]	During bus transfers, external devices can drive these signals to indicate port width.
	—	$\overline{OE}$	
	DSACK[1:0]	$\overline{TA}$	These signals are active even if the bus transfer is to or from a peripheral that is using one of the chipselects to terminate the bus cycle.
	$\overline{BERR}$	$\overline{TEA}$	
	R/$\overline{W}$	R/$\overline{W}$	
	SIZ[1:0]	TSIZ[1:0]	
	—	$\overline{TIP}$	
	—	$\overline{TS}$	
	$\overline{RMC}$	—	
	$\overline{AS}$	—	
	$\overline{DS}$	—	
Chip Selects	$\overline{CSBOOT}$	$\overline{CS0}$	
	CS[10:0]	CS[7:1]	muxing with SD_CS?
Bus Arbitration	BR	—	
	BG	—	
	BGACK	—	
SDRAM Controller	—	SD_SRAS	
	—	SD_SCAS	
	—	SD_WE	
	—	SD_CS[1:0]	
	—	SD_CKE	

Table 1. MC68332/MCF523*x* External Signal Comparison (continued)

Module	MC68332 Signal	MCF523*x* Signal	Comment
External Interrupts	IRQ[7:1]	IRQ[7:1]	
	$\overline{\text{AVEC}}$	—	The MCF523*x* does not perform external IACK bus cycles, so $\overline{\text{AVEC}}$ is not needed.
TPU	—	TPUCH[31:16]	
	TP[15:0]	TPUCH[15:0]	
	T2CLK	TCRCLK	external TPU CLKIN
Fast Ethernet Controller	—	EMDIO	
	—	EMDC	
	—	ECOL	
	—	ECRS	
	—	ERXCLK	
	—	ERXDV	
	—	ERXD[3:0]	
	—	ERXER	
	—	ETXCLK	
	—	ETXEN	
	—	ETXER	
	—	ETXD[3:0]	
I^2C	—	I2C_SDA	
	—	I2C_SCL	
QSPI	$\overline{\text{PCS}}$[3:0]	QSPI_CS[1:0]	
	$\overline{\text{SS}}$	—	
	SCK	QSPI_CLK	
	MISO	QSPI_DIN	
	MOSI	QSPI_DOUT	
Serial Ports	RXD	URXD[2:0]	
	TXD	UTXD[2:0]	
	—	$\overline{\text{UCTS}}$[2:0]	
	—	$\overline{\text{URTS}}$[2:0]	
General Purpose Timers	—	DTIN[3:0]	
	—	DTOUT[3:0]	

Table 1. MC68332/MCF523*x* External Signal Comparison (continued)

Module	MC68332 Signal	MCF523*x* Signal	Comment
Debug Port	DSCLK	DSCLK	
	—	PSTCLK	
	$\overline{\text{BKPT}}$	$\overline{\text{BKPT}}$	
	DSI	DSI	
	DSO	DSO	
	—	DDATA[3:0]	
	FC[2:0]/FREEZE	PST[3:0]	
	$\overline{\text{FETCH}}$	—	
	$\overline{\text{IPIPE}}$	—	
	$\overline{\text{HALT}}$	—	
Test	$\overline{\text{TSTME}}$	TEST	
	—	PLL_TEST	
Misc.	QUOT	—	quotient out
	TSC	—	three state control
Power Supplies	VDD	VDD	
	VSS	VSS	
	—	OVDD	
	—	OVSS	
	VDDSYN	VDDPLL	
	—	VSSPLL	
	VSTBY	—	

2.4 On-chip Modules

This section examines the MCF523*x* on-chip modules and highlights differences between these modules and those found on the MC68332. Modules with similar functionality are compared first followed by modules found only on the MCF523*x*.

2.4.1 Similar Modules

The MCF523*x* and MC68332 share several modules that provide similar functionality. Each of these modules is discussed in the following sections.

2.4.1.1 TPU vs. eTPU

One of the most compelling reasons to migrate to the MCF523*x* family from the MC68332 is the addition of an enhanced Time Processing Unit (eTPU) to the V2 ColdFire core. The MC68332 includes a Time

Processor Unit (TPU) to address complex timing problems in embedded control applications. Since the TPU is a microcontroller itself, it can perform timing tasks with little or no CPU intervention, thus improving overall system performance. The eTPU on the MCF523*x* is an enhanced version of TPU. These enhancements include a more powerful processor, more channels, and an increase in Parameter RAM and code memory, allowing for more functionality and increased performance. Consequently, the eTPU significantly increases overall system performance. The MCF523*x* is the first ColdFire device to include an eTPU module.

2.4.1.1.1 Software Considerations

One of the primary enhancements of the eTPU is a more powerful processor that is capable of efficiently handling high-level C code. This allows for greater range of functionality at a higher level of performance.

Although there is no compatibility at the microcode level, the eTPU maintains several features of older TPU versions and is conceptually almost identical. As most TPU users utilized the standard set of TPU functions on the 68332, this identical functionality and more will also be provided on the eTPU. Therefore, porting is not a major concern. The eTPU library is a superset of the standard TPU library functions modified to take advantage of enhancements in the eTPU. These, along with a C compiler and source code from the Freescale library, make it is possible for the eTPU to support the user's own function development.

For a list of eTPU functions, please refer to the *eTPU Reference Manual* (ETPURM).

2.4.1.1.2 Hardware Consideration

The number of timer channels for the eTPU increased from 16 to 32, which allows more control with a single eTPU. The code memory increased from 2 KB to 6 KB, and the parameter RAM also increased from 200 B to 1.5 KB.

Another enhancement is that now the eTPU supports more interrupt types. Not only can each eTPU channel generate an interrupt, but there is also one global interrupt.

With respect to the eTPU resolution of performing timing tasks, the eTPU Core has a resolution of 13.33 ns, and the eTPU Timebases have a resolution of 26.66 ns at 150 MHz. Compared to 120 ns and 240 ns at 16.67 on the 68332, respectively, it shows a 10x improvement.

For more detailed information, please refer to *The Essentials of the Enhanced Time Processing Unit* (AN2353).

2.4.1.2 SRAM

The MC68332 has 2 Kbytes of SRAM while the MCF523*x* has 64 Kbytes. For both devices, the base address of the SRAM is programmable via a base address register. The primary difference between the SRAM is that the MC68332 supports SRAM data retention during power down by supplying voltage to the V_{STBY} pin; while, the MCF523*x* does not support standby power for the SRAM.

2.4.1.3 SCI vs. UART

Moving from the MC68332's single SCI to the three MCF523*x* UARTs is a move toward more functionality; there are very few migration issues as a result of differences between these two asynchronous communication modules. The biggest advantage in moving from the SCI to a UART is the ability to incorporate flow control in the communication link, thereby preventing receiver overruns. This can be accomplished with the $\overline{\text{URTS}}$ and $\overline{\text{UCTS}}$ handshaking signals of the MCF523*x*'s UARTs.

Table 2 contrasts the features of the MC68332's SCIs and the MCF523*x*'s UARTs.

Table 2. SCI and UART Feature Differences

Feature	SCI	UART	Comments
Clock Source	$f_{SYS}/16$	$f_{SYS}/32$, DTIN	DMA Timer input can be used as external UART clock reference on the MCF523*x*
Baud Rate Divider Range	13-bit Prescaler	16-bit Prescaler	Baud rate = Clock source divided by any value in specified range
Hardware Flow Control	—	√	
Programmable Number of Data Bits	8,9	5,6,7,8	
Programmable Number of Stop Bits	√	√	
Programmable Parity Enable	√	√	
Programmable Parity Type	√	√	Even or odd parity
Force Polarity of Parity Bit	—	√	
Send Break	√	√	MCF523*x*'s break signal may be variable length
Indication of Break Received	—	√	
Framing, Parity, and Overrun Error Indications	√	√	
Transmitter Empty, Transmission Complete, Receiver Ready/Full Indications	√	√	
Idle Line, Noise Indication	√	—	
Receive FIFO	1 shift register, 1 shared data register	1 shift register, 3 dedicated Rx data registers	
Transmit FIFO	1 shift register, 1 shared data register	1 shift register, 1 dedicated Tx data register	
Multidrop Mode Support	—	√	Parity bit setting to indicate data or address character
Automatic Echo Mode	—	√	
Local Loop-back Mode	—	√	
Remote Loop-back Mode	—	√	

As indicated in the table, the three UARTs on the MCF523*x* can be externally clocked via the corresponding DMA timer's DTIN inputs. This allows for synchronous operation with respect to the external clock and UART baud rate generation at frequencies totally independent of the internal clock frequency.

One final feature of the MCF523*x* UARTs is their ability to trigger a DMA transfer from any programmed source and destination addresses, when a UART's receive buffer is either full or not empty or when a UART's Transmit buffer is empty.

2.4.1.4 Queued Serial Peripheral Interface (QSPI)

The MC68332 and MCF523*x* both contain a QSPI module that provide a full-duplex, synchronous serial peripheral interface for communicating with peripherals and other MCUs. The MCF523*x* module is based on the MC68332's QSPI, so most of the features, control registers, and bit fields are similar if not identical.

Table 3 contrasts the features of the MC68332 and the MCF523*x* QSPIs.

Table 3. MC68332 and MCF523*x* QSPI Feature Differences

Feature	MC68332	MCF523*x*	Comments
Programmable 16 entry queue	√	√	
Slave mode	√	—	
Master mode	√	√	
Programmable transfer sizes of 8 to 16 bits in 1-bit increments	√	√	
Programmable delays before and after transfers	√	√	
Programmable QSPI clock phase	√	√	
Programmable QSPI clock polarity	√	√	
Wraparound mode	√	√	
Peripheral chip select lines	4	2	
Slave select signal	√	—	The MCF523*x* QSPI only operates in master mode, so no slave select line is needed.
Loopback mode	√	—	
Programmable peripheral chip select polarity	—	√	

2.4.1.5 Periodic Interrupt Timers (PITs)

The MC68332 has a single PIT that is capable of generating interrupts at programmable intervals. The MCF523*x* has four PITs with similar functionality. As with migrating from the SCI to UARTs, the migration from the MC68332 PIT to the MCF523*x* PITs is a move toward more functionality. There should be very few migration issues as a result of differences between these two modules. In addition to the increase in the number of timers, the MCF523*x* offers a wider variety of prescaler and modulus options.

Table 4 contrasts the features of the MC68332 and the MCF523*x* PITs.

Table 4. MC68332 and MCF523*x* PIT Feature Differences

Feature	MC68332	MCF523*x*
Number of PITs	1	4
Prescaler values	1 or 512	2^n (n = 1–16)
Modulus values	1–255	1–65536
Programmable interrupt request level	√	√

2.4.1.6 Watchdog Timer

The MC68332 and MCF523*x* both include a software watchdog timer. As with the PITs, the functionality of the modules is very similar; however, the MCF523*x* family offers a wider range of time-out values. The MCF523*x*'s watchdog has a 16-bit prescaler register, whereas the MC68332 only has eight prescaler options.

2.4.1.7 Interrupt Controller (INTC)

The interrupt architecture of ColdFire is exactly the same as the CPU32 family. A 3-bit encoded interrupt priority level is sent from the interrupt controller to the core, providing 7 levels of interrupt requests. Level 7 represents the highest priority interrupt level, while level 1 is the lowest priority. The processor samples for active interrupt requests once per instruction by comparing the encoded priority level against a 3-bit interrupt mask value (I) contained in bits 10:8 of the machine's status register (SR). If the priority level is greater than the SR[I] field at the sample point, the processor suspends normal instruction execution and initiates interrupt exception processing. Level 7 interrupts are treated as non-maskable and edge-sensitive within the processor, while levels 1-6 are treated as level-sensitive and may be masked depending on the value of the SR[I] field. For correct operation, the ColdFire architecture requires that, once asserted, the interrupt source remain asserted until explicitly disabled by the interrupt service routine.

During the interrupt exception processing, the CPU enters supervisor mode, disables trace mode, and then fetches an 8-bit vector from the interrupt controller. This byte-sized operand fetch is known as the interrupt acknowledge (IACK) cycle, with the ColdFire implementation using a special encoding of the transfer type and transfer modifier attributes to distinguish this data fetch from a "normal" memory access. The fetched data provides an index into the exception vector table that contains 256 addresses, each pointing to the beginning of a specific exception service routine. In particular, vectors 64 - 255 of the exception vector table are reserved for user interrupt service routines. The first 64 exception vectors are reserved for the processor to handle reset, error conditions (access & address), arithmetic faults, system calls, etc. Once the interrupt vector number has been retrieved, the processor continues by creating a stack frame in memory. For ColdFire, all exception stack frames contain 32 bits of vector and status register data, and the 32-bit program counter value of the instruction that was interrupted (refer to the *MCF5235 Reference Manual* for more information on the stack frame format). After the exception stack frame is stored in memory, the processor accesses the 32-bit pointer from the exception vector table using the vector number as the offset, and then jumps to that address to begin execution of the service routine. After the status register is stored in the exception stack frame, the SR[I] mask field is set to the level of the interrupt being acknowledged, effectively masking that level and all lower values while in the service routine. For many

peripheral devices, the processing of the IACK cycle directly negates the interrupt request, while other devices require that request to be explicitly negated during the processing of the service routine.

For the MCF523*x*, the processing of the interrupt acknowledge cycle is fundamentally different than on the MC68332. In the new approach, all IACK cycles are directly handled by the interrupt controller, so IACK cycles are not routed to the requesting peripheral device or the external bus. Instead, every interrupt source (including external interrupt requests on the IRQ[7:1] pins) has a fixed vector assignment.

The MCF523*x* has a set of interrupt control registers (ICR1–ICR63) that has the same functionality as the MC68332's QSM Interrupt Level Register (QILR). That is, they assign an interrupt priority to each of the interrupt sources. The difference here is that the ColdFire architecture supports a priority scheme in which there is both a priority and a level that define an interrupt's overall priority. There are 9 priorities associated with each of the 7 levels of interrupts for a total of 63 unique interrupt priority levels. (It is important that each interrupt source is assigned a unique priority level to guarantee proper operation of the interrupt controller.) Eight of the nine priorities are assignable to each of the interrupt sources. The ninth priority within each interrupt level is a fixed priority interrupt and is automatically assigned to the external $\overline{\text{IRQ}}$ interrupts. The priority and level for these interrupts are fixed such that $\overline{\text{IRQ1}}$ is the fixed priority interrupt within level 1, $\overline{\text{IRQ2}}$ is the fixed priority interrupt within level 2, and so on through $\overline{\text{IRQ7}}$ for level 7. These fixed-priority interrupts have a priority at the midpoint of the 9 priorities within each level such that priority 0 (lowest priority) through priority 3 are lower priority than the fixed priority ($\overline{\text{IRQ}}n$) for a particular level, while priority 4 through priority 7 (highest priority) have a higher priority than the fixed priority for a particular level.

Since there are more than 63 interrupt sources on the MCF523*x*, there are two instantiations of the interrupt controller used to assign levels and vectors to all of the on-chip and off-chip interrupt sources—INTC0 and INTC1. When both interrupt controllers have active interrupts at the same level and priority, then the INTC0 interrupt will be serviced first. If INTC1 has an active interrupt that has a higher level or priority than the highest active INTC0 interrupt, then the INTC1 interrupt will be serviced first.

Once the MCF523*x*'s ICRs are programmed with the desired priority and level for each interrupt source, then that interrupt source's interrupts are enabled by clearing the corresponding bit in the interrupt mask registers (IMRH and IMRL). There is a bit in these two 32-bit registers for each possible interrupt source associated with the interrupt controller, plus another bit that masks all interrupts regardless of the individual mask bit settings. This level of masking is in addition to the interrupt masking using the status register's interrupt priority mask field that is used on both the MC68332 and the MCF523*x*.

These are the basic control differences between the interrupt controllers in these two devices. This section is not the extent of the interrupt servicing and exception handling considerations that need to be examined. However, it does highlight the differences in interrupt control methodology between the two devices.

2.4.1.8 External Interrupt Pins vs. Edge Port (EPORT)

The MC68332 has seven active low external interrupt pins ($\overline{\text{IRQ}}$[7:1]). Similarly, the MCF523*x* has up to seven interrupt signals $\overline{\text{IRQ}}$[7:1] as part of the Edge Port (EPORT) module. The EPORT provides additional programmability for interrupt triggering. The MC68332 only level detects interrupts, but each of the MCF523*x*'s external interrupt pins can be configured for level-sensitive, rising edge triggered, falling edge triggered, or falling and rising edge triggered interrupts on a pin-by-pin basis.

Table 5 contrasts the features of the MC68332's interrupts pins and the MCF523*x*'s EPORT.

Table 5. External Interrupt Pin and EPORT Differences

Feature	Interrupt Pins	EPORT	Comments
Number of external interrupts	7	Up to 7	There are 7 IRQ signals on all 523x device's except for the QFP version of the MCF5232 which has 3 IRQ signals available ($\overline{IRQ7}$, $\overline{IRQ4}$, & $\overline{IRQ1}$)
Programmable interrupt triggering	—	√	Level, rising or falling edge, or both rising and falling edges

2.4.1.9 General Purpose I/O Module

Like the MC68332, unused bus interface and peripheral pins on the MCF523*x* can be used as discrete general-purpose inputs and outputs. These are managed by a dedicated GPIO module that logically groups all pins into ports located within a contiguous block of memory-mapped control registers.

All of the pins associated with the external bus interface may be used for several different functions. Their primary function is to provide an external memory interface to access off-chip resources. When not used for this, all of the pins may be used as general-purpose digital I/O pins. In some cases, the pin function is set by the operating mode, and the alternate pin functions are not supported.

The primary difference between the MC68332 and the MCF523*x* is the number of GPIOs supported. The MC68332 has up to 32 GPIOs, but the MCF523*x* supports up to 81 GPIO pins.

2.4.1.10 PLL and Clocks

Similar to the MC68332, the clock module on the MCF523*x* allows it to be configured for one of several clocking methods. However, the clock module on the MCF523*x* has much more functionality. Clocking modes include internal frequency modulated phase-locked loop (PLL) clocking with either an external clock reference or an external crystal reference supported by an internal crystal amplifier. The PLL can also be disabled and an external oscillator can be used to clock the device directly.

Table 6 contrasts the features of the MC68332 and the MCF523*x* PLL.

Table 6. MC68332 and MCF523*x* PLL Differences

Feature	MC68332	MCF523*x*	Comments
Operating modes			
Normal mode with crystal reference	√	√	
Normal mode with external clock reference (oscillator)	—	√	
1:1 Mode	—	√	
Bypass mode	√	√	
Clock frequency options			
Input clock frequency			
normal mode	25kHz-50kHz	8-25MHz	
bypass mode	0-25MHz	24-75MHz	
System clock frequency			
normal mode	130kHz-25MHz	24-75MHz	
bypass and 1:1 mode	0-25MHz	24-75MHz	
System clock to CLKOUT ratio	16:1, 8:1	1:1	

2.4.2 New/Additional Modules

There are seven modules on the MCF523*x* that have no functional equivalent on the MC68332. They are the Fast Ethernet controller (FEC), Cache, FlexCAN, SDRAM controller, Direct Memory Access controller (DMA), I^2C, and cryptographic hardware accelerators (SKHA, MDHA, and RNG). The following sections give a high-level description of these modules. The only migration issue with these modules is whether or not they could be of use in an existing design when porting to the MCF523*x*. If an existing MC68332 design has similar functionality implemented off-chip, then it may be beneficial to eliminate the external components and bring the functionality on chip.

2.4.2.1 Fast Ethernet Controller (FEC)

The MCF523*x*'s integrated Fast Ethernet controller (FEC) performs the full set of IEEE 802.3/Ethernet CSMA/CD media access control and channel-interface functions. The FEC supports connection and functionality for either 10 or 100 Mbps 802.3 media independent interface (MII), with either half or full duplex capability. It requires an external transceiver (PHY) to complete the interface to the media. There are on-chip transmit and receive FIFOs, a built-in dedicated DMA controller, and memory-based flexible descriptor rings.

2.4.2.2 Cache

The 8-Kbyte cache can be configured into one of three possible organizations: an 8-Kbyte instruction cache, an 8-Kbyte data cache, or a split 4-Kbyte instruction/4-Kbyte data cache. The configuration is software-programmable by control bits within the privileged Cache Configuration Register (CACR). In all configurations, the cache is a direct-mapped, single-cycle memory, organized as 512 lines, each containing

16 bytes of data. The memories consist of a 512-entry tag array (containing addresses and control bits) and an 8-Kbyte data array, organized as 2048 x 32 bits.

If the desired address is mapped into the cache memory, the output of the data array is driven onto the ColdFire core's local data bus, completing the access in a single cycle. If the data is not mapped into the tag memory, a cache miss occurs and the processor core initiates a 16-byte, line-sized fetch. The cache module includes a 16-byte line fill buffer used as temporary storage during miss processing. For all data cache configurations, the memory operates in write-through mode, and all operand writes generate an external bus cycle.

2.4.2.3 FlexCAN

The FlexCAN module is a communication controller that implements the CAN 2.0B protocol. The CAN protocol can be used as an industrial control serial data bus, meeting the specific requirements of real-time processing, reliable operation in harsh EMI environments, cost-effectiveness, and required bandwidth. The FlexCAN is based on, and includes, all existing features of the Freescale TouCAN module. The communication data structure supports both standard data and remote frames (up to 109 bits long) and extended data and remote frames (up to 127 bits long). Each message's data block size is programmable at 0–8 bytes in length, and the bit rate is programmable up to 1 Mbit/sec.

A total of 16 flexible message buffers (MBs), each with 0–8 byte data length, are configurable for received or transmitted messages, all supporting standard and extended messages. Unused MB space can be used as general purpose RAM space.

2.4.2.4 SDRAM Controller

The SDRAM controller provides all required signals for glueless interfacing to a variety of JEDEC-compliant SDRAM devices. SRAS/SCAS address multiplexing is software-configurable for different page sizes. To maintain refresh capability without conflicting with concurrent accesses on the address and data buses, $\overline{\text{SRAS}}$, $\overline{\text{SCAS}}$, $\overline{\text{DRAMW}}$, $\overline{\text{SDRAM\_CS}}$[1:0], and SCKE are dedicated SDRAM signals.

The SDRAM controller module provides glueless integration of the SDRAM with the MCF523*x*. The key features of the DRAM controller include the following:

- Support for two independent blocks of SDRAM
- Interface to standard SDRAM components
- Programmable SRAS, SCAS, and refresh timing
- Support for 8-, 16-, and 32-bit wide SDRAM blocks

2.4.2.5 Direct Memory Access Controller (DMA)

The Direct Memory Access controller (DMA) module provides an efficient way to move blocks of data with minimal processor interaction. The DMA module provides four fully programmable channels (DMA0–DMA3) that allow byte, word, longword, or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCR*n*[START] bit. In addition to software triggering, the DMA

support hardware triggers via the external $\overline{\text{DREQ}}n$ signals, UARTs, eTPU, and DMA timers (DTIM0–DTIM3).

The DMA controller supports dual address mode to on-chip devices. The transfers are dual-address and support 8-, 16- and 32-bit data transfer sizes, as well as 16-byte (4 x 32-bit) burst transfers. The source and destination address pointers can be incremented, or they can remain constant upon each transfer; there is also one 24-bit byte-transfer counter per DMA channel. There is auto-alignment transfer support for efficient block movement, and bursting and cycle stealing is also supported. A crossbar switch in the DMA controller allows software-programmable connections from the DMA requesters (external $\overline{\text{DREQ}}$[2:0], the eTPU, the three UARTs and the four DMA timers) to the four DMA channels to trigger the transfer for each of the channels.

2.4.2.6 I²C

The I²C™ bus is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. It is used primarily as an inter-chip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads. It is fully compatible with the industry-standard I²C bus.

2.4.2.7 Cryptography

The superset device, MCF5235, incorporates small, fast, dedicated hardware accelerators for random number generation, message digest and hashing, and the DES, 3DES, and AES block cipher functions. This allows for the implementation of common Internet security protocol cryptography operations with performance well in excess of software-only algorithms.

2.4.2.7.1 Symmetric Key Hardware Accelerator (SKHA) Features

The Symmetric Key Hardware Accelerator (SKHA) supports the following block ciphers:

- AES
  - 128-bit key
  - Electronic Code Book (ECB), Cipher Block Chaining (CBC), Counter (CTR) cipher modes
- DES
  - 64-bit key (with parity)
  - ECB, CBC, and CTR modes
- Triple-DES
  - 2 key & 3 key (128-bits & 192-bits with parity)
  - Key parity check
  - ECB, CBC, and CTR modes

2.4.2.7.2 Message Digest Hardware Accelerator (MDHA) Features

The Message Digest Hardware Accelerator (MDHA) computes a single message digest (or hash or integrity check) value of all the data presented on the input bus, using either the MD5 or SHA-1 algorithms for bulk data hashing. The MDHA includes these distinctive features:

- MD5 one way 128-bit hash function specified in RFC 1321
- SHA-1 one way 160-bit hash function specified by the ANSI X9.30-2 and FIPS 180-1 standards
- HMAC support for all algorithms, as specified in RFC 2104
- EHMAC support for the SHA-1 algorithm
- EHMAC key support up to 160 bits
- Processes 512 bit blocks organized as 16×32 bit longwords
- Automatic message and key padding
- Internal 16×32 bit FIFO for temporary storage of hashing data

2.4.2.7.3 Random Number Generator (RNG)

The random number generator (RNG) module is capable of generating 32-bit random numbers. It is designed to comply with FIPS-140 standards for randomness and non-determinism.

2.4.2.8 DMA Timers

There are four independent, DMA-transfer-generating 32-bit timers (DTIM0, DTIM1, DTIM2, DTIM3) on the MCF523*x*. Each timer module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DTIN*x* signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler that clocks the actual timer counter register (TCR*n*). The timer counter may be set as free running or restarting, and a timer resolution of 13.33-ns at 75 MHz can be achieved.

Each of these timers can be configured for input capture or reference compare mode. By setting the internal registers, each timer may be configured to assert an external signal, generate an interrupt (maskable) on a particular event or cause a DMA transfer. Input capture may be set to sense either edge transition on the input pin. Output compare supports programmable modes for the output pin toggling.

2.5 Operating Modes

During reset, the MC68332 latches the values on the MODCK pin to determine boot options such as clock mode, $\overline{\text{CSBOOT}}$ port size, and chip select configuration. The MCF523*x* determines operating modes at reset in a similar manner, but the MCF523*x* has more boot chip configuration options. The MCF523*x* gives the user the capability of configuring various modes of operation such as boot device, output pad strength, clock mode options, and chip select configuration.

2.5.1 Chip Configuration

When the $\overline{\text{RCON}}$ pin is asserted at reset, the state of several of the device's pins determines the mode of operation for the device. If $\overline{\text{RCON}}$ is not asserted at reset, then the default configuration is used. This section discusses the modes of operation and how the device is configured for the various modes.

For the MCF523*x*, there are four mode settings used to configure the device for a specific configuration. These mode settings are boot data port size, output pad drive strength, chip clock mode, and chip select configuration. Each of these mode parameters have two to four different selections:

- Boot data port size
  - 32-bit (default)
  - 16-bit
  - 8-bit
- Output pad strength
  - Partial drive strength (default)
  - Full drive strength
- Clock mode
  - Normal PLL with external crystal (default)
  - Normal PLL with external oscillator
  - 1:1 PLL Mode
  - External oscillator mode (no PLL)
- Chip select configuration
  - PADDR[7:5] configured as A[23:A21] (default)
  - PADDR7 configured as $\overline{\text{CS6}}$, PADDR[6:5] as A[22:A21]
  - PADDR[7:6] configured as $\overline{\text{CS}}$[6:5], PADDR5 as A21
  - PADDR[7:5] configured as $\overline{\text{CS}}$[6:4]

Table 7 shows the data bus pins and the dedicated pins used by each device for chip configuration.

Table 7. MC68332/MCF523*x* Configuration Pin Descriptions

MCF523*x* Pin	Chip Configuration Function	Pin State/Meaning	Comments
$\overline{\text{RCON}}$	Chip configuration enable	0 Enabled 1 Disabled	Active low: if asserted, then all configuration pins must be driven appropriately for desired operation
D26, D17, D16	Select chip operating mode	111 Master All other settings are reserved	
D20, D19	Select boot data port size	00 32-bit port 10 8-bit port 01 16-bit port 11 32-bit port	
D21	Select output pad drive strength	0 Partial 1 Full	
CLKMOD1, CLKMOD0	Select clock mode	00 External clock mode (no PLL) 01 1:1 PLL mode 10 Normal PLL with external clock reference 11 Normal PLL with crystal reference	V_{DDPLL} must be supplied if a PLL mode is selected
D25, D24	Select chip select / address line	00 PADDR[7:5] configured as A[23:A21] (default) 10 PADDR7 configured as $\overline{\text{CS6}}$, PADDR[6:5] as A[22:A21] 01 PADDR[7:6] configured as $\overline{\text{CS}}$[6:5], PADDR5 as A21 11 PADDR[7:5] configured as $\overline{\text{CS}}$[6:4]	

Chip configuration is performed at reset, and reset out ($\overline{\text{RSTOUT}}$) can be used to gate an external latch to provide the desired polarity on each of the pins during chip configuration. The recommended chip configuration circuit is shown in Figure 4.

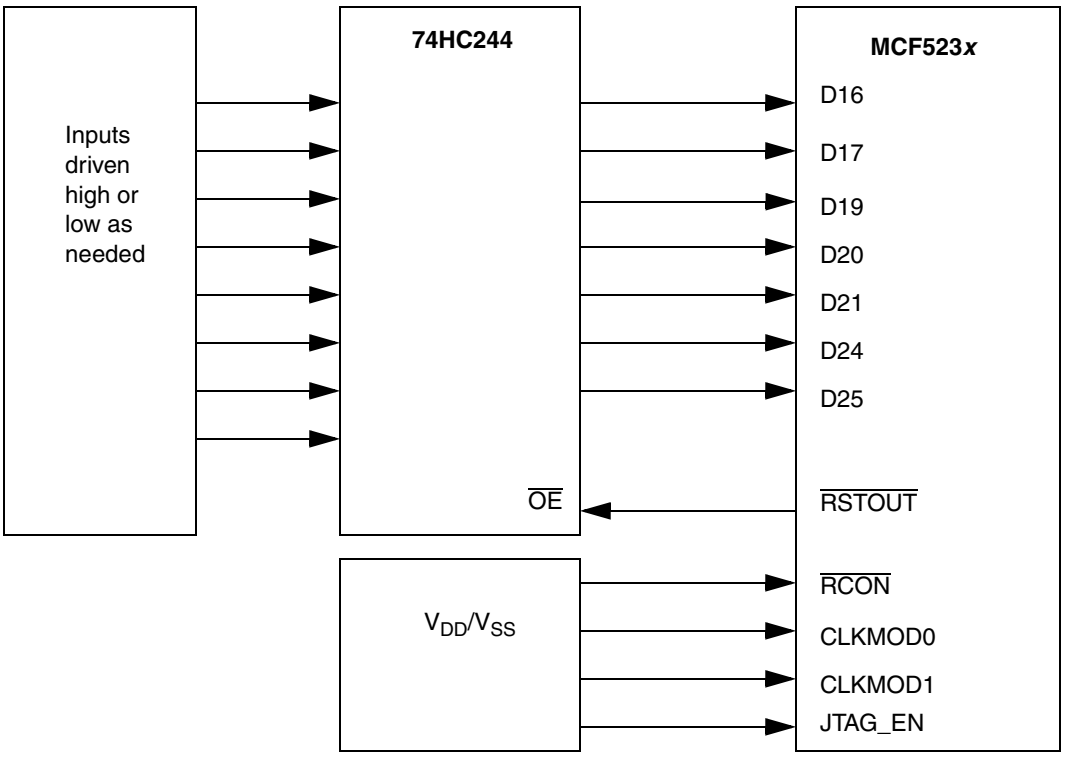

Figure 4. MCF523*x* Recommended Reset Configuration Circuit

2.6 Software Considerations

2.6.1 Mapping 24-bit MC68332 Addresses to the 32-bit MCF523*x*

The fact that the MCF523*x* supports 32-bit addressing and the MC68332 supports 24-bit addressing should make no difference when porting the system software, because the MCF523*x* can use a 24-bit addressing scheme. This is accomplished by treating the upper 8-bits as a “don't-care” (except when using on-chip cache). The MCF523*x* has three registers that control how specific regions of address space are assigned access control attributes: two access control registers (ACR0 and ACR1) and the cache control register (CACR). Since the ACRs and the CACR use address bits 31–24 to define reference attributes for memory regions, virtual-to-physical memory mapping can be used to map unique 24-bit address space regions to unique 16-Mbyte regions in the 32-bit address space. This will enable certain areas of the physical memory map to utilize the capabilities of MCF523*x* caching. For instance, this can be accomplished by concatenating A[31:24] = $01 in front of the first 24-bit address region, and using ACR0 to control the caching scheme for this region. This can also be done for ACR1 and CACR to configure cacheable memory regions. For more details, please refer to Chapter 5, “Cache,” of the *MCF5235 Reference Manual*.

2.6.2 Read-Modify-Write (RMW) Cycles

If the original MC68332 code uses the Test And Set (TAS) instruction for implementing the locked or read-modify-write transfer sequence in hardware, the instruction must be emulated in software on the MCF523*x*. In order to do this, the interrupt mask should be raised to level 7, the read, modify, and write instructions should be executed, and then the mask should be lowered to the appropriate level. Performing this sequence of instructions will guarantee that they will execute uninterrupted with the exception of a level 7 interrupt, which is nonmaskable.

2.6.3 Software Porting from M68000 Family Devices

One of the primary advantages of migrating an existing MC680X0 or MC683XX design to ColdFire is the ease of software migration. Retargeting C or other high level programming language code to ColdFire is relatively easy, and the risk of introducing errors into the code during the process is low. In addition, the majority of ColdFire assembly instructions are derived directly from the 68K assembly language. This makes porting assembly code from 68K to ColdFire much easier than porting to a completely new architecture.

There are a number of tools available to address the handling of 68K assembly code. MicroAPL has two free tools available—PortASM-68K and CF68KLib. The PortASM-68K tool is an assembly translation tool that takes 68K assembly, flags instructions or instructions that use addressing modes that are not supported by ColdFire, and replaces them with a ColdFire compatible emulation sequence. CF68KLib is an emulation library that allows for 68K targeted assembly to be run directly on a ColdFire target without translation. The library makes use of the ColdFire's illegal instruction exception (vector 4) to trap on 68K instructions that are unsupported by ColdFire. When the processor encounters one of these instructions, an exception is generated and the library's exception handler will decode the instruction and run a ColdFire code sequence to emulate the instruction.

One of the other advantages is that in most cases the ColdFire targeted code can be run on the existing M68K hardware. This allows for testing the software conversion on known good hardware. In addition, software development can start in parallel with development of the ColdFire based hardware.

It is assumed that target software consists of C (or another high level programming language) and assembly source code. The first step to create an executable that will run on existing M68K hardware to test the conversion from M68K to the proper ColdFire subset. This step verifies that the process of code conversion.

For more information on porting from M68000, please refer to Appendix B of the *MCF5206e User's Manual*.

3 Summary

There is little or no lost functionality, memory, or performance when migrating from the MC68332 to the MCF523*x*. With the capability of triplingthe operating frequency, there should not be any additional performance issues. Furthermore, most module functionality available on the MC68332 is either duplicated or improved upon on the MCF523*x*, and the additional set of MCF523*x* on-chip peripheral modules should enable many off-chip functions to be incorporated on chip, reducing hardware costs.

If the advantages gained from more functional integration and higher performance make this migration beneficial, then this document should serve as a valuable reference to make the transition as smooth as possible.

4 References

Table 8. References

Freescale Document Number	Title	Revision
MCF5235RM/D	MCF5235 Microprocessor Reference Manual	1
MC68332UM/D	MC68332 User's Manual	1
AN2353	TPU to eTPU Migration Application Note	
M5206EUM/D	M5206e User's Manual	1
CFPRM/D	ColdFire Family Programmer's Reference Manual	2
CFPRODFACT/D	The ColdFire Family of 32-Bit Microprocessors Family Overview and Technology Roadmap	0
MCF5XXXWP	MCF5XXXWP WHITE PAPER: Freescale ColdFire VL RISC Processors	0

5 Document Revision History

Table 9 provides a revision history for this application note.

Table 9. Document Revision History

Rev. No.	Substantive Change(s)	Date of Release
1	Official release	October 2004

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