



High-Speed CAN/LIN Fail-Safe System Basis Chip

UJA1065TW

Not Recommended for New Designs

This page contains information on a product that is not recommended for new designs.

Last Updated: Dec 15, 2024

The UJA1065 fail-safe System Basis Chip (SBC) replaces basic discrete components that are common in every Electronic Control Unit (ECU) with a Controller Area Network (CAN) and a Local Interconnect Network (LIN) interface. The fail-safe SBC supports all networking applications that control various power and sensor peripherals by using high-speed CAN as the main network interface and LIN as a local sub-bus. The fail-safe SBC contains the following integrated devices:

- High-speed CAN transceiver, interoperable and downward compatible with CAN transceivers TJA1041 and TJA1041A, and compatible with the ISO 11898-2 standard and the ISO 11898-5 standard (in preparation)
- LIN transceiver compliant with LIN 2.0 and SAE J2602, and compatible with LIN 1.3
- Advanced independent watchdog
- Dedicated voltage regulators for microcontroller and CAN transceiver
- Serial peripheral interface (full duplex)
- Local wake-up input port
- Inhibit/limp-home output port

In addition to the advantages of integrating these common ECU functions in a single package, the fail-safe SBC offers an intelligent combination of system-specific functions such as:

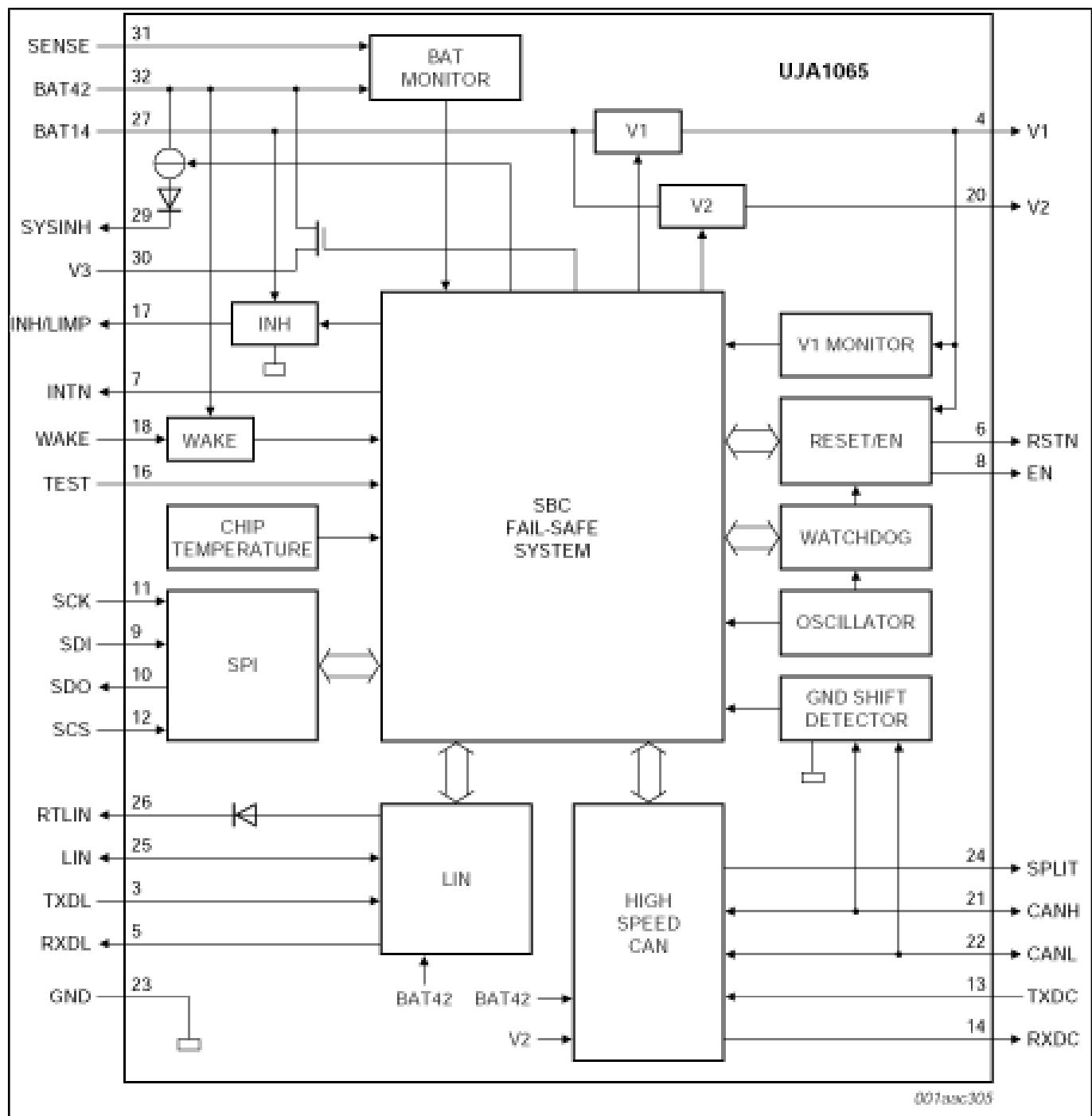
- Advanced low-power concept
- Safe and controlled system start-up behavior
- Advanced fail-safe system behavior that prevents any conceivable deadlock
- Detailed status reporting on system and subsystem levels

The UJA1065 is designed to be used in combination with a microcontroller that incorporates a CAN controller. The fail-safe SBC ensures that the microcontroller is always started up in a

defined manner. In failure situations, the fail-safe SBC will maintain microcontroller functionality for as long as possible to provide full monitoring and a software-driven fall-back operation.

The UJA1065 is designed for 14 V single power supply architectures and for 14 V and 42 V dual power supply architectures.

UJA1065TW CAN/LIN Fail-Safe SBC Block Diagram



View additional information for [High-Speed CAN/LIN Fail-Safe System Basis Chip](#).

Note: The information on this document is subject to change without notice.

www.nxp.com

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. © 2025 NXP B.V.