LIN 2.2A/SAE J2602 Transceiver with TXD Dominant Timeout

TJA1029

Last Updated: Feb 12, 2025

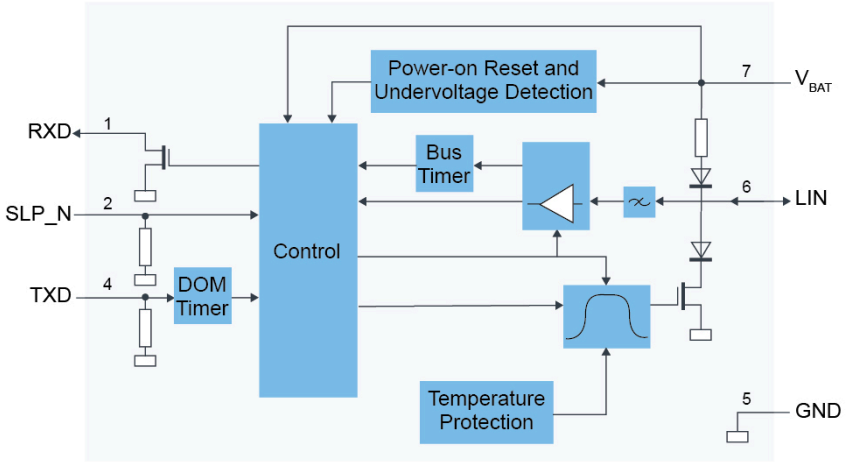
The TJA1029 is the interface between the Local Interconnect Network (LIN) leader/follower protocol controller and the physical bus in a LIN network. It is primarily intended for in-vehicle subnetworks using baud rates up to 20 kBd and is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2 A and SAE J2602. The TJA1029 is pin-compatible with the TJA1020, TJA1021, TJA1022 and TJA1027.

The protocol controller generates the transmit data stream. The TJA1029 converts the data stream into an optimized bus signal shaped to minimize ElectroMagnetic Emissions (EME). The LIN bus output pin is pulled HIGH via an internal termination resistor. For a leader application, connect an external resistor in series with a diode between pin VBAT and pin LIN. The receiver detects a receive data stream on the LIN bus input pin and transfers it via pin RXD to the microcontroller.

Power consumption is very low in Sleep mode. However, the TJA1029 can still be woken up via pins LIN and SLP_N. An integrated TXD dominant time-out function prevents the bus being driven to a permanent dominant state.

LIN 2.2A/SAE J2602 Transceiver with TXD Dominant Timeout Block Diagram

TJA1029



View additional information for LIN 2.2A/SAE J2602 Transceiver with TXD Dominant Timeout.

Note: The information on this document is subject to change without notice.