RapidRF LDMOS Front-End Designs

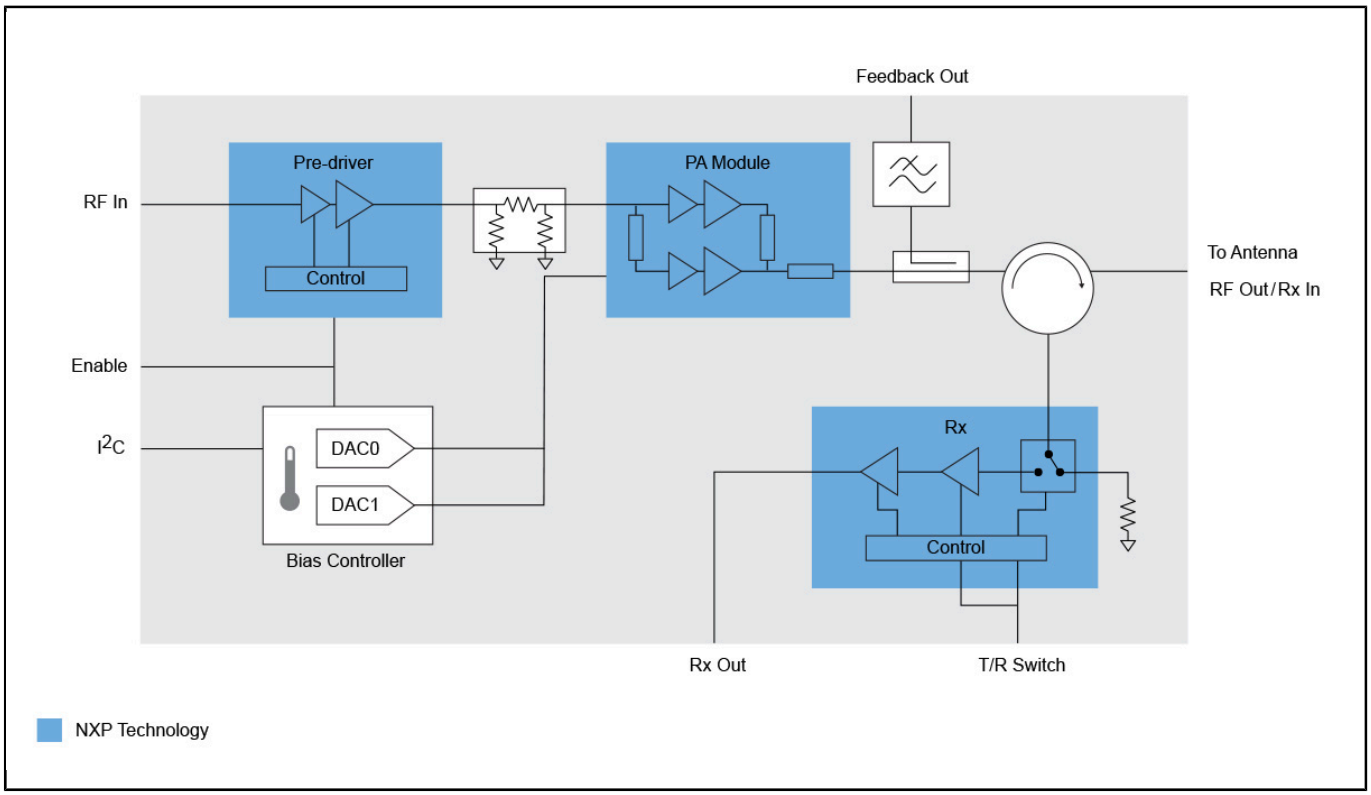
RAPIDRF-FRONTEND

Last Updated: Feb 12, 2025

NXP’s RapidRF front-end designs for 5G infrastructure integrate a linear pre-driver, RF power amplifier, Rx LNA with T/R switch, a circulator and a bias controller in a compact footprint. They incorporate a coupler for DPD feedback and are to be used with digital pre-distortion.

RapidRF reference boards are ideal for 5G radio units requiring 2.5 to 5 Watts (34-37 dBm) average transmit power at the antenna. Versions for different bands use a common PCB layout, simplifying both design and manufacturing for faster time-to-market.

RapidRF Front-end Block Diagram Block Diagram



View additional information for RapidRF LDMOS Front-End Designs.

Note: The information on this document is subject to change without notice.