Bootable CPU RTC with Two I²C Buses, 128 Byte SRAM and Alarm Function

PCF85053A

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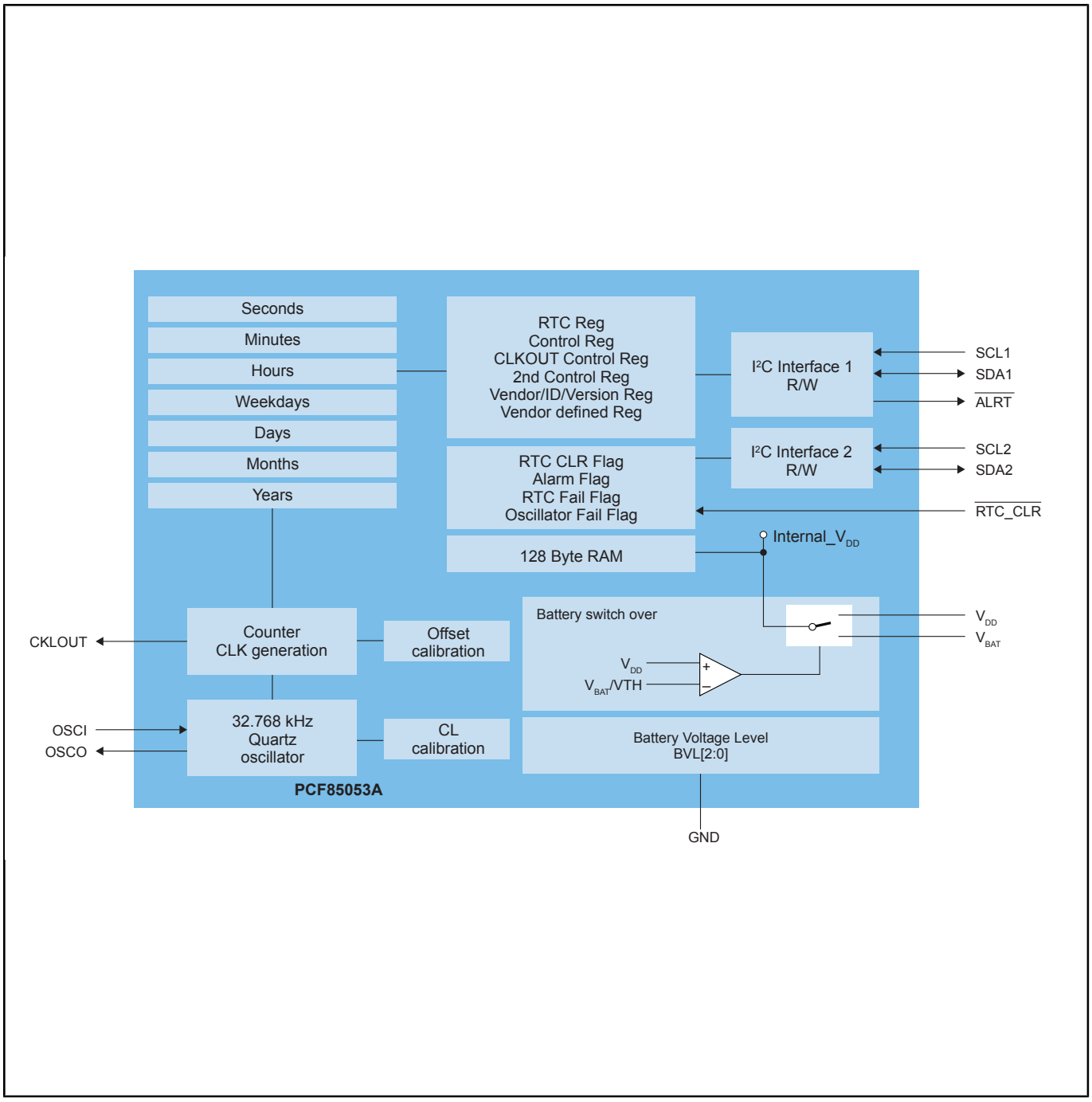
PCF85053A is a CMOS real-time clock (RTC) and calendar, optimized for low power consumption and automatic switching to battery on primary power loss. Featuring clock output, alert interrupt output and 128-byte battery backed-up SRAM, the PCF85053A includes two I²C buses. The primary I²C bus has the read / write capability on RTC and SRAM registers; the second I²C bus also can read / write most registers with the control bits set by primary I²C controller.

PCF85053A offers clock output calibration-related registers such as crystal capacitive load (CL) configuration and offset register setting.

Bootable CPU RTC with Two I²C Buses, 128 Byte SRAM and Alarm Function Block Diagram



View additional information for Bootable CPU RTC with Two I²C Buses, 128 Byte SRAM and Alarm Function.

Note: The information on this document is subject to change without notice.

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