



# Expandable 5-Channel I<sup>2</sup>C-Bus Hub

## PCA9518

### Archived

This page contains information on a product that is no longer manufactured (discontinued). Specifications and information herein are available for historical reference only.

Last Updated: Sep 13, 2024

The PCA9518 is a BiCMOS integrated circuit intended for application in I<sup>2</sup>C-bus and SMBus systems.

While retaining all the operating modes and features of the I<sup>2</sup>C-bus system, it permits extension of the I<sup>2</sup>C-bus by buffering both the data (SDA) and the clock (SCL) lines, thus enabling virtually an unlimited number of buses of 400 pF.

The I<sup>2</sup>C-bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9518 enables the system designer to divide the bus into an unlimited number of segments off of a hub where any segment to segment transition sees only one repeater delay and is multiple controller capable on each segment.

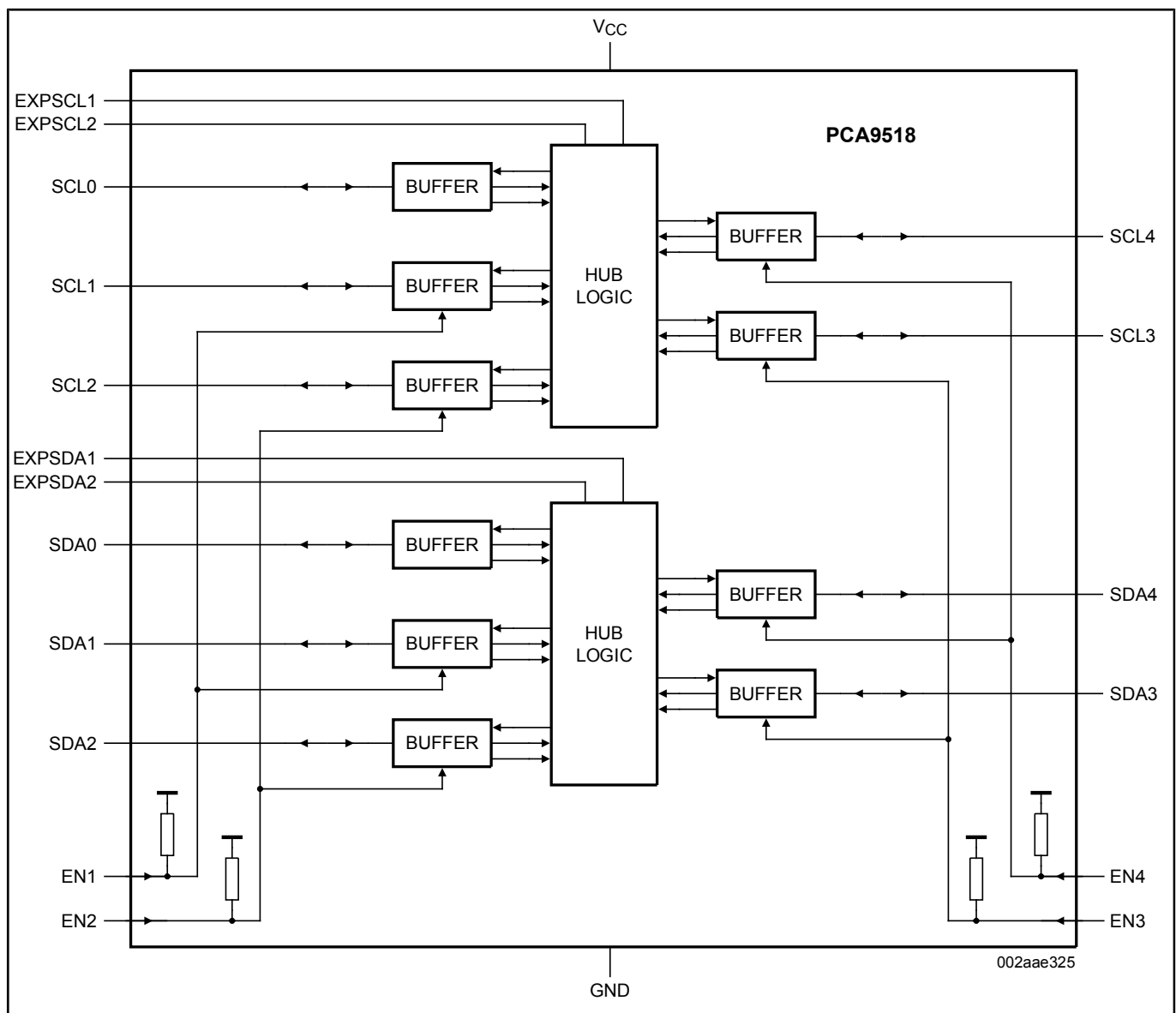
Using multiple PCA9518 parts, any width hub (in multiples of five) can be implemented using the expansion pins.

The PCA9518 is a wider voltage range (2.3 V to 3.6 V) version of the PCA9518 and also improves partial power-down performance, keeping I<sup>2</sup>C-bus I/O pins in high-impedance state when VDD is below 2.0 V.

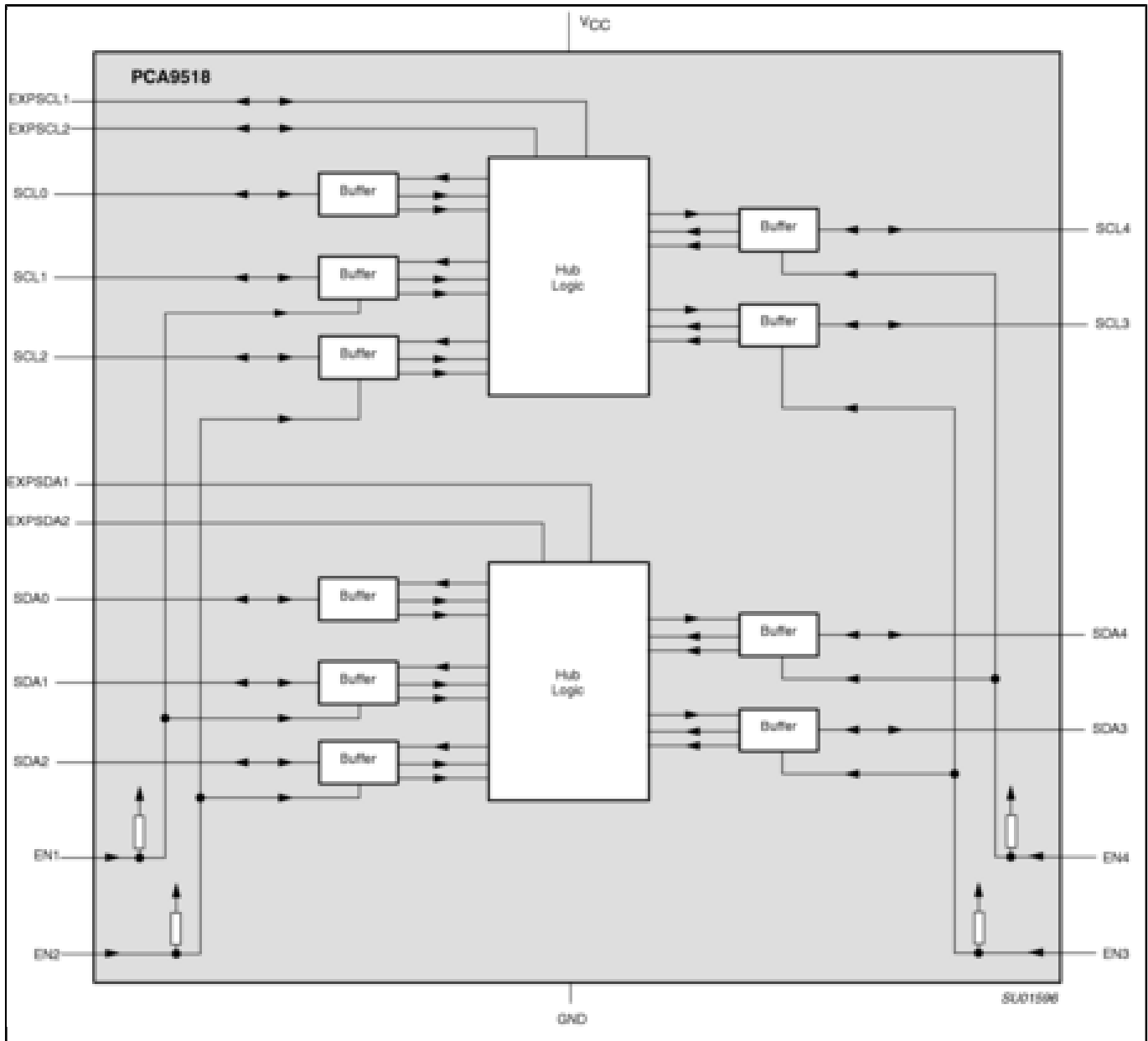
A PCA9518 cluster cannot be put in series with a PCA9515/16 or with another PCA9518 cluster. Multiple PCA9518 devices can be grouped with other PCA9518 devices into any size cluster thanks to the EXPxxn pins that allow the I<sup>2</sup>C-bus signals to be sent/received from/to one PCA9518 to/from another PCA9518 within the cluster. Since there is no direction pin, slightly different 'legal' low voltage levels are used to avoid lock-up conditions between the input and the output of individual repeaters in the cluster. A 'regular LOW' applied at the input of any of

the PCA9518 devices will then be propagated as a 'buffered LOW' with a slightly higher value to all enabled outputs in the PCA9518 cluster. When this 'buffered LOW' is applied to a PCA9515 and PCA9516 or separate PCA9518 cluster (not connected via the EXPxxxn pins) in series, the second PCA9515 and PCA9516 or PCA9518 cluster will not recognize it as a 'regular LOW' and will not propagate it as a 'buffered LOW' again. The PCA9510/9511/9513/9514 and PCA9512 cannot be used in series with the PCA9515 and PCA9516 or PCA9518, but can be used in series with themselves since they use shifting instead of static offsets to avoid lock-up conditions.

## PCA9518 Block Diagram



## PCA9518D, PCA9518PW Block Diagram



View additional information for [Expandable 5-Channel I²C-Bus Hub](#).

**Note:** The information on this document is subject to change without notice.

**www.nxp.com**

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. © 2025 NXP B.V.