80C51 8-Bit Microcontroller

P87C554SBAA

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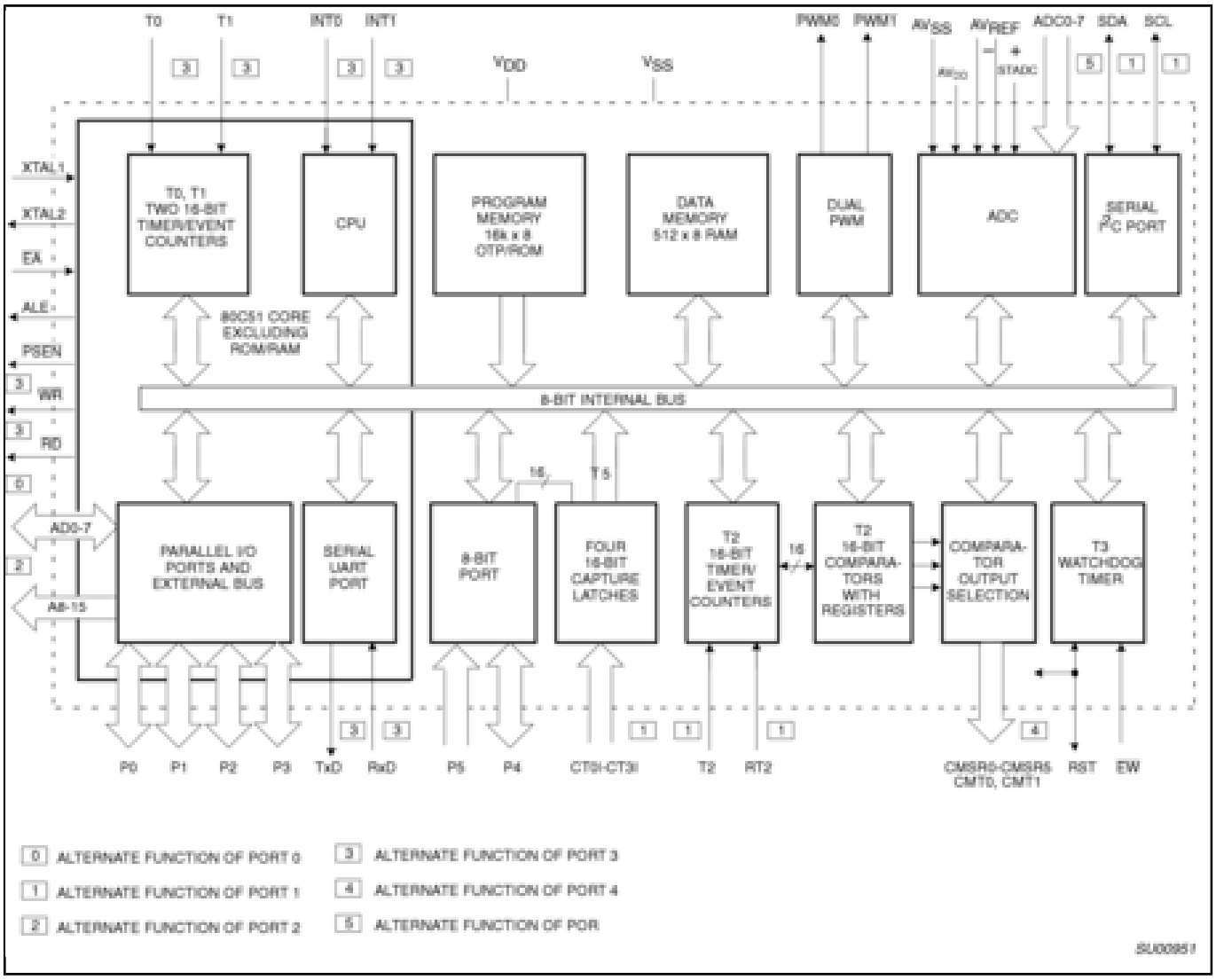
The P87C554 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 87C554 has the same instruction set as the 80C51.

The 87C554 contains a 16k x 8 non-volatile EPROM, a 512 x 8 read/write data memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, four-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I²C-bus), a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the P87C554 can be expanded using standard TTL compatible memories and logic.

In addition, the P87C554 has two software selectable modes of power reduction-idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning. Optionally, the ADC can be operated in Idle mode. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte, and 17 three-byte. With a 16 MHz crystal, 58 pct. of the instructions are executed in 0.75 us and 40 pct. in 1.5 us. Multiply and divide instructions require 3 us.

Block diagram: P80C554SFBD, P87C554SBAA, P87C554SFAA Block Diagram



View additional information for 80C51 8-Bit Microcontroller.

Note: The information on this document is subject to change without notice.