



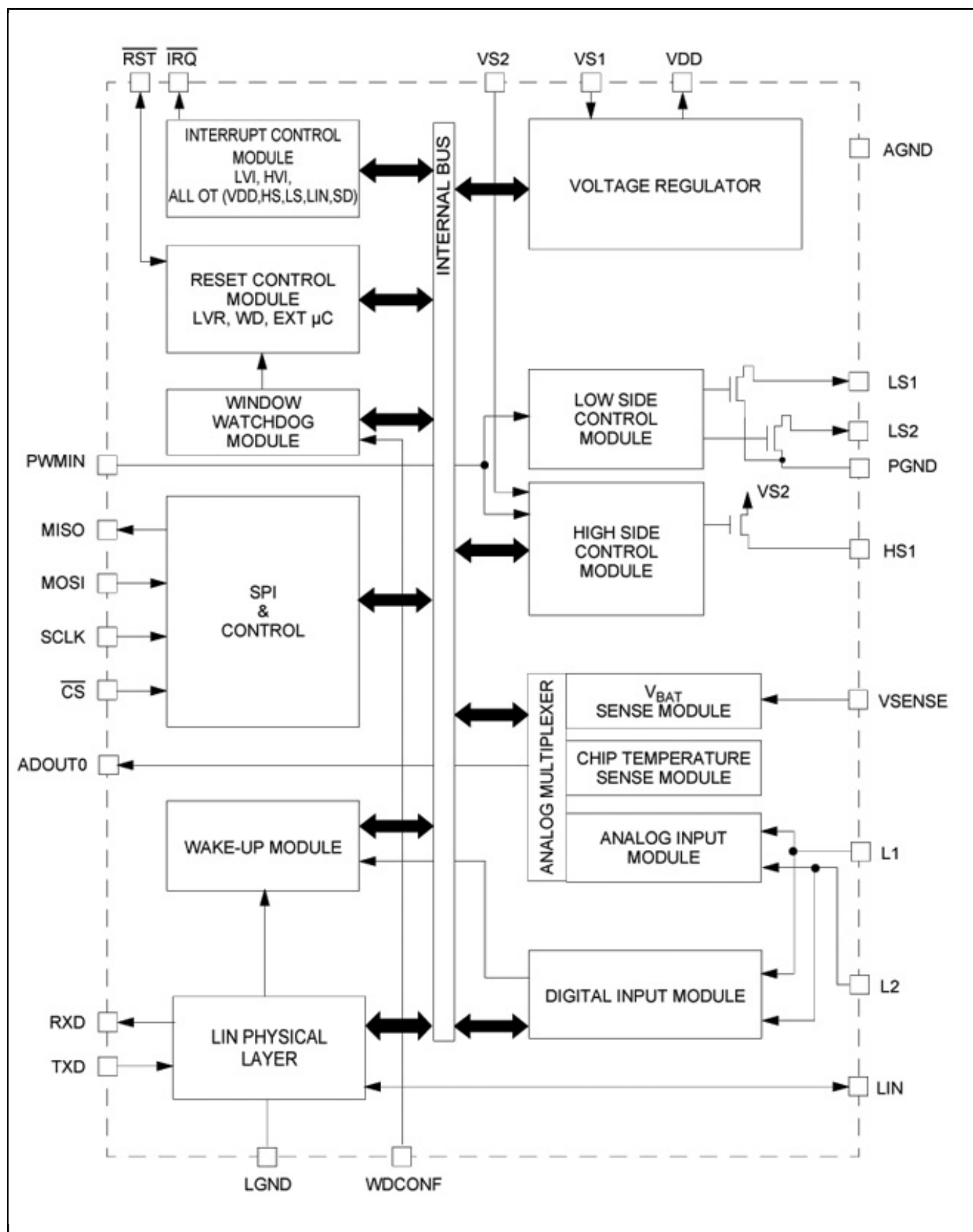
LIN System Basis Chip with DC Motor Predriver

MC33911

Last Updated: Mar 24, 2025

The 33911 is a Serial Peripheral Interface (SPI)-controlled System Basis Chip (SBC) combining many frequently used functions in an MCU-based system, plus a Local Interconnect Network (LIN) transceiver. The 33911 has a 5.0V - 50mA low dropout regulator with full protection and reporting features. The device provides full SPI-readable diagnostics and a selectable timing watchdog for detecting errant operation. The LIN Protocol Specification 2.0 and 2.1 ('G5AC) compliant LIN transceiver, has waveshaping circuitry that can be disabled for higher data rates. One 60mA high side switch and two 160mA low side switches with output protection are available for driving resistive and inductive loads. All outputs can be pulse-width modulated (PWM). Two high-voltage inputs are available for use in contact monitoring, or as external wake-up inputs. These inputs can be used as high-voltage analog Inputs. The voltage on these pins is divided by a selectable ratio and available via an analog multiplexer. The 33911 has three main operating modes: Normal (all functions available), Sleep (VDD off, wake-up via LIN, wake-up inputs (L1,L2), cyclic sense, and forced wake-up), and Stop (VDD on with limited current capability, wake-up via CS, LIN bus, wake-up inputs, cyclic sense, forced wake-up, and external reset). The 33911 is compatible with LIN Protocol Specification 2.0, 2.1 ('G5AC) and SAEJ2602-2 ('G5AC).

MC33911 Network Transceivers Block Diagram



View additional information for [LIN System Basis Chip with DC Motor Predriver](#).

Note: The information on this document is subject to change without notice.

www.nxp.com

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. © 2025 NXP B.V.