



Low-Power Microcontrollers (MCUs) Based on Arm® Cortex®-M4 Cores With Optional Cortex®-M0+ Co- processor

LPC541XX

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The LPC541xx MCU family of single-core and dual-core MCUs are our next-generation of power efficient MCUs. With added scalability and feature integration, these devices enable continued market growth in today's competitive always-on environment.

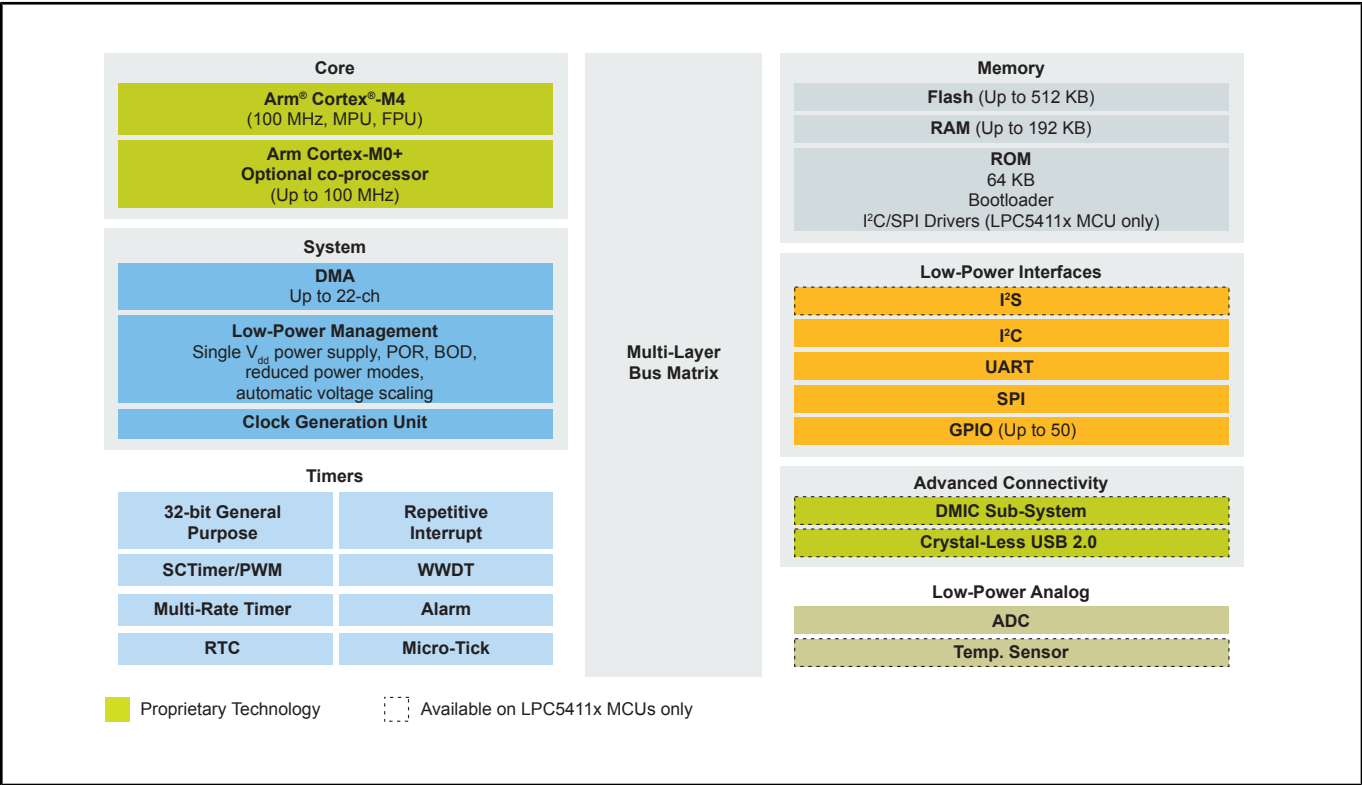
LPC541xx MCUs are based on the power-efficient Arm® Cortex-M4 core, each with an optional Cortex®-M0+ coprocessor. Single Cortex-M4 options are available for architectures that value single core processing without software partitioning.

In an always-on application, these MCUs operate in a power-down mode, listening for incoming data, which when available, can wake either core to acquire or process the information. When in an active mode, developers can optimize power efficiency and throughput by choosing between the power-efficient Cortex-M0+ core for data collection, aggregation, and system task management, or the Cortex-M4 core, which can complete processor-intensive algorithms, such as sensor fusion more quickly helping to reduce power consumed.

The optional dedicated on-chip digital microphone (DMIC) subsystem on the LPC54110 family will also dramatically reduce power in applications that demand voice input and processing, achieving the stringent power efficiencies required for always-on voice-activation in battery-operated products.

This device is fully supported by NXP's [MCUXpresso Software and Tools](#), a comprehensive and cohesive set of free software development tools for Kinetis, LPC and i.MX RT microcontrollers. MCUXpresso SDK also includes project files for Keil MDK and IAR EWARM.

LPC541xx MCU Block Diagram



View additional information for [Low-Power Microcontrollers \(MCUs\) Based on Arm® Cortex®-M4 Cores With Optional Cortex®-M0+ Co-processor](#).

Note: The information on this document is subject to change without notice.