NXP's Energy Efficient Cortex-M4 MCU with Cortex-M0+ and Advanced Security
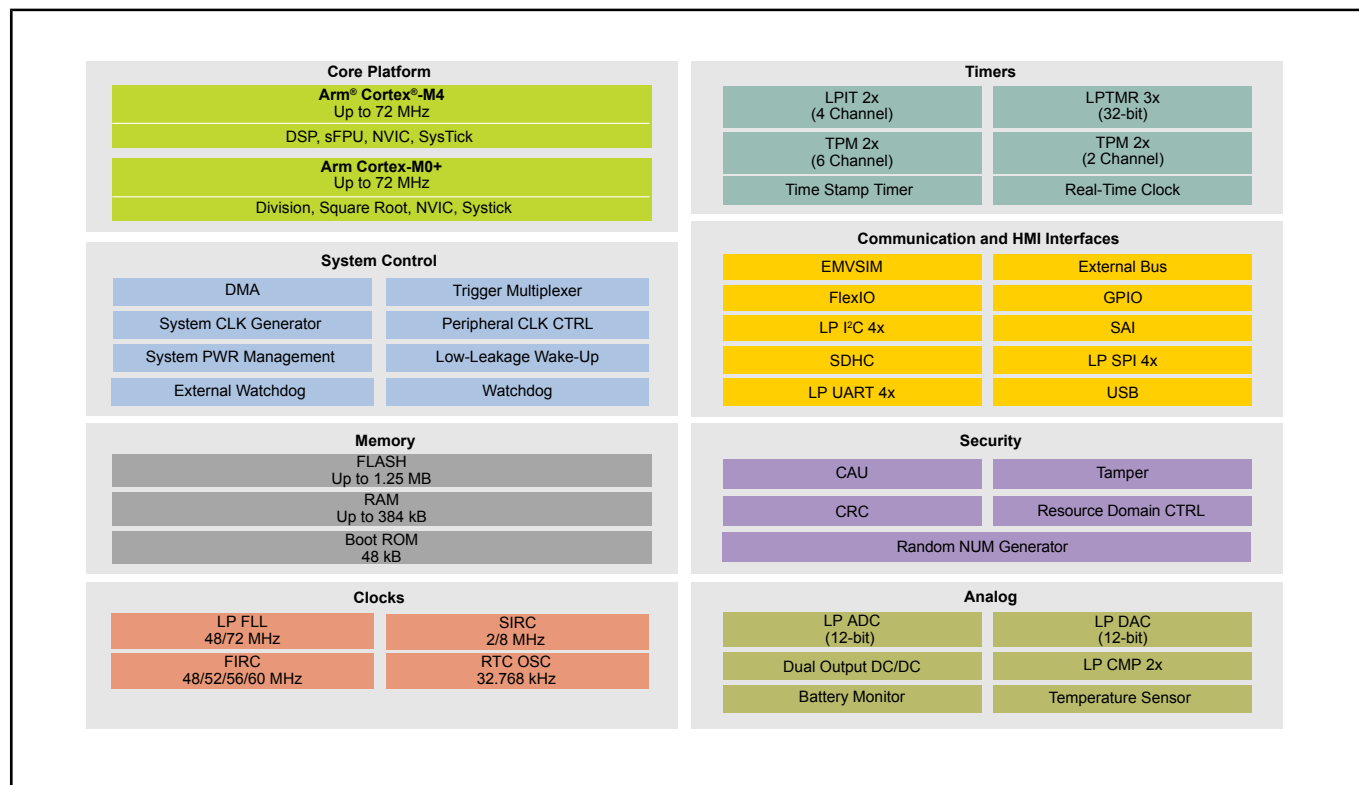
K32-L3

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Building on the successful Kinetis K Series (K22 and K24), the K32 L3 family of MCUs delivers a 50% improvement in power optimization and security advancements over the previous generation, to address a wide range of industrial and IoT applications. The K32 L3 MCU family is based on the power-efficient Arm® Cortex® -M4 core and offers a Cortex-M0+, providing new enhancements such as low-leakage power-optimized peripherals, a DC-DC converter, and security features like authenticated boot, secure update and tamper detection pins.

The introduction of the K32 L3 MCU family is the start of a long line of MCUs, which will further advance NXP's security capabilities and power optimization features to lead the market in the next generation of low-leakage applications. The K32 L3 MCU family is complemented by a comprehensive ecosystem including MCUXpresso software and tools and a Freedom development board for easy prototyping.

K32 L3 MCU Block Diagram

Core Platform

Arm® Cortex®-M4
Up to 72 MHz

DSP, sFPU, NVIC, SysTick

Arm Cortex-M0+
Up to 72 MHz

Division, Square Root, NVIC, Systick

System Control

DMA	Trigger Multiplexer
System CLK Generator	Peripheral CLK CTRL
System PWR Management	Low-Leakage Wake-Up
External Watchdog	Watchdog

Memory

FLASH
Up to 1.25 MB

RAM
Up to 384 kB

Boot ROM
48 kB

Clocks

LP FLL 48/72 MHz	SIRC 2/8 MHz
FIRC 48/52/56/60 MHz	RTC OSC 32.768 kHz

Timers

LPIT 2x (4 Channel)	LPTMR 3x (32-bit)
TPM 2x (6 Channel)	TPM 2x (2 Channel)
Time Stamp Timer	Real-Time Clock

Communication and HMI Interfaces

EMVSIM	External Bus
FlexIO	GPIO
LP I²C 4x	SAI
SDHC	LP SPI 4x
LP UART 4x	USB

Security

CAU	Tamper
CRC	Resource Domain CTRL
Random NUM Generator	

Analog

LP ADC (12-bit)	LP DAC (12-bit)
Dual Output DC/DC	LP CMP 2x
Battery Monitor	Temperature Sensor

View additional information for NXP's Energy Efficient Cortex-M4 MCU with Cortex-M0+ and Advanced Security.

Note: The information on this document is subject to change without notice.