HITAG® Reader Solution

HTRC11001T

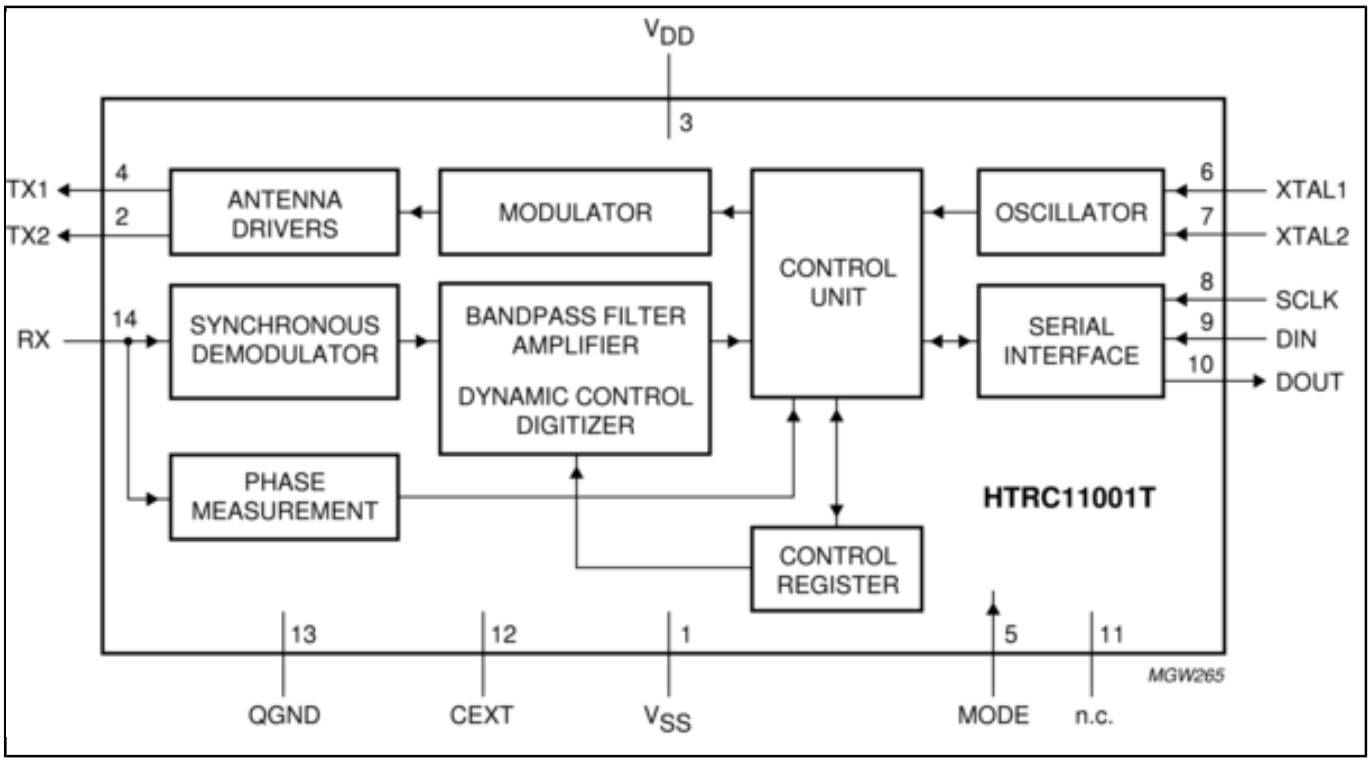
Last Updated: Dec 15, 2024

The HITAG® Reader Chip HTRC110 is intended for use with transponders, which are based on NXP® Semiconductors based HITAG transponder ICs.

In addition the IC supports other 125 kHz transponder types using amplitude modulation for the write operation and AM/PM for the read operation. The receiver parameters (gain factors, filter cutoff frequencies) can be optimized to system and transponder requirements. The HTRC110 is designed for easy integration into RF-identification readers. State-of-the-art technology allows almost complete integration of the necessary building blocks. A powerful antenna driver/ modulator together with a low-noise adaptive sampling time demodulator, programmable filters/ amplifier and digitizer build the complete transceiver unit, required to design high-performance readers. A three-pin microcontroller interface is employed for programming the HTRC110 as well as for the bidirectional communication with the transponders. The three-wire interface can be changed into a two-wire interface by connecting the data input and the data output.

Tolerance dependent zero amplitude modulation caused severe problems in envelope detector systems, resulting in the need of very low tolerance reader antennas. These problems are solved by the Adaptive Sampling Time technique (AST).

Block diagram: HTRC11001T Block Diagram



View additional information for HITAG® Reader Solution.

Note: The information on this document is subject to change without notice.