Digital Signal Controller

DSP56F801

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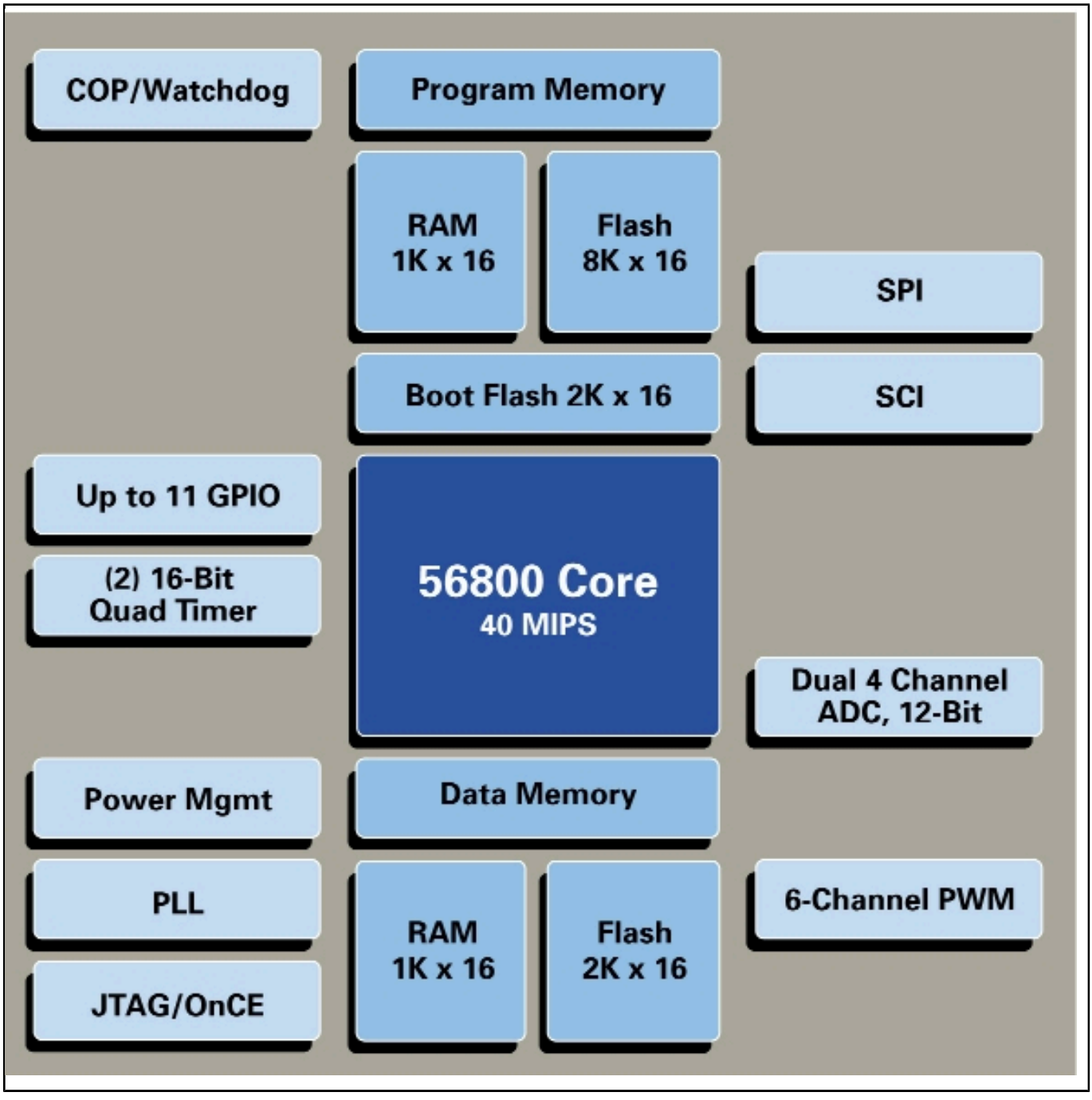
The 56F801, a member of the 56800 core-based family of Digital Signal Controllers, combines the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals on a single chip to create an extremely cost-effective solution for servo and motor control, power inverter, and converter applications.

The 56800 core is based on a Harvard-style architecture consisting of three execution units which operate in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP- and MCU-style applications. The instruction set is also highly efficient for C Compilers, enabling rapid development of optimized control applications.

DSP56F801 Block Diagram Block Diagram



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Note: The information on this document is subject to change without notice.

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