UM10755

PTN3355 (e)DP to VGA bridge IC application board

Rev. 1 — 19 January 2015 **User manual**

Document information

Info	Content
Keywords	PTN3355, PTN3393, DisplayPort, eDP, VGA, bridge, application board
Abstract	This user manual presents demonstration / application board capability of interfacing an (embedded) DisplayPort source to VGA output. The application board (nicknamed "ULT DPVGA") is intended for use as an evaluation and customer demonstration tool, as well as a reference design.

Revision history

Rev	Date	Description
1	20150119	Initial version.

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1. Introduction

PTN3355 is a low-power DisplayPort to VGA bridge IC with an integrated 1-2 VGA switch. PTN3355 consumes approximately 200 mW of power for video streaming in WUXGA resolution and 890 uW of power in low-power mode. The VGA output is powered down when there is no valid DisplayPort source data being transmitted. PTN3355 is suitable for Ultra Low Power Notebook and other low-power devices. PTN3355 also offers a second VGA port for docking design.

PTN3355 is powered from a 3.3 V power source, and generates 1.5 V through an internal step-down switch regulator and buck converter for internal core usage and DAC usage.

For cost saving, the external inductor for the buck converter can be removed; the internal LDO can supply 1.5 V for core usage and DAC usage without any re-work.

However, using LDO consumes twice as much as the buck converter, about 400 mW.

This document describes the user manual of PTN3355 ULT DP-VGA application board, including:

- Overall PCB connectors, jumpers, and power supplies
- Equipment/Tools that this board will be interfacing with for board testing
- System level connections such as cables and connectors that this board will be plugged into

This application board is intended to demonstrate the bridging capabilities of PTN3355 on low power DP to VGA conversion.

1.1 Purposes

This document is for internal engineers to evaluate the performance of PTN3355 and to develop firmware, including collecting and verifying system level features/performances/functionalities such as:

- Verify power management schemes
- Power sequence
- Power consumption measurement during various operating modes.
- Allow access to test points and jumpers for measurement and configuration purposes
- Flash over AUX and MS_I2C
- Programming and debug test via MS_I2C

For marketing to demonstrate ULT DP-VGA to customers in the field:

- Functional and interoperability test.
- This board should be connected to a DP or an eDP source.
- This board can be powered by an external 3V3 power adapter, or
- External power supplies with +3.3V (1A), or
- DP 1.0 cable that carries 3V3 power.

For customers to evaluate PTN3355:

- Use I2C to change configuration.

2. General description

2.1 Co-layout of PTN3355 with PTN3393

This application board is designed to evaluate PTN3393 first then PTN3355 later with component stuffing variation. An HVQFN40 socket footprint is reserved in preparation for socket installation to test and program ICs.

Due to the bulky socket footprint, the bulk converter design has to be placed on the back side to be close to PTN3355. Also due to co-layout for two ICs, extra components are necessary for stuffing option.

Hence the layout is not optimal as if only PTN3355 is placed without the socket.

The placement can be dramatically improved in a real application.

2.2 Block diagram

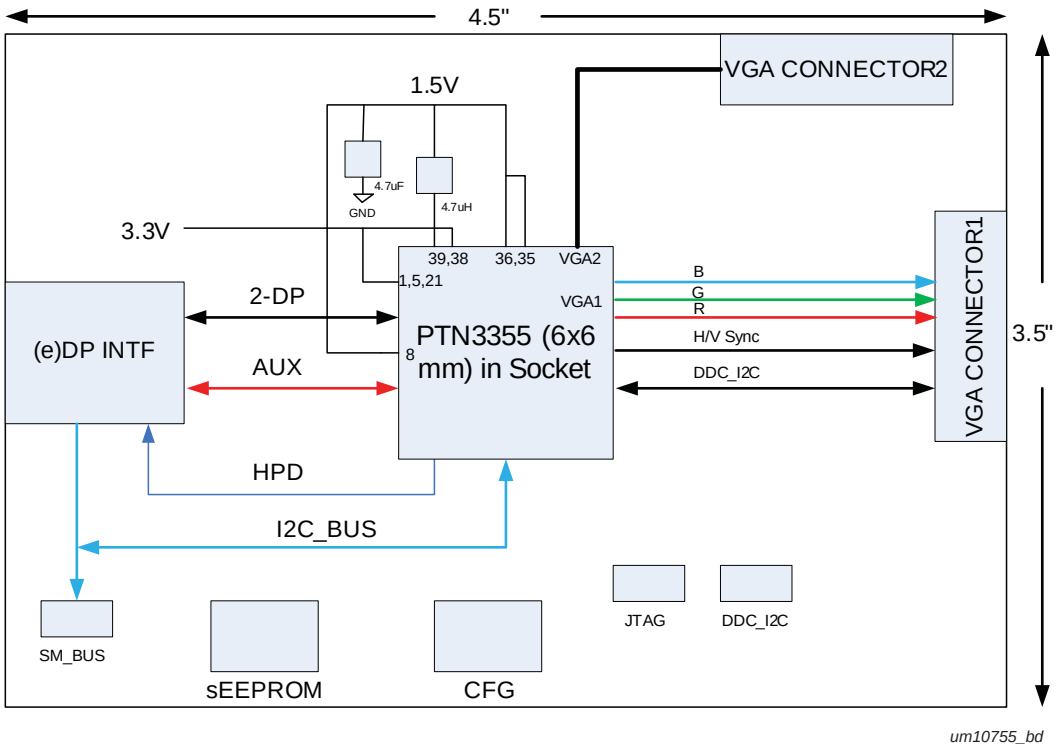

Fig 1. ULT DP-VGA application board block diagram

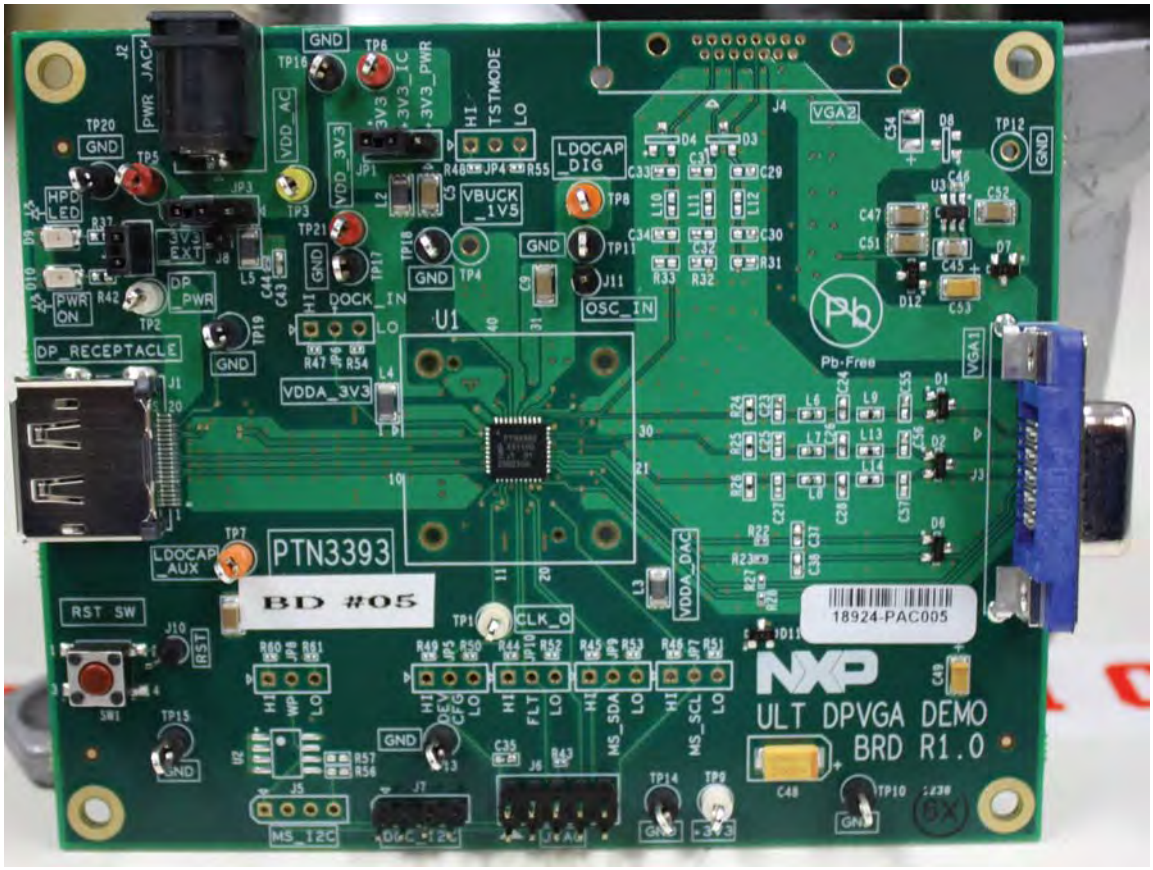

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Fig 2. PTN3393 application board

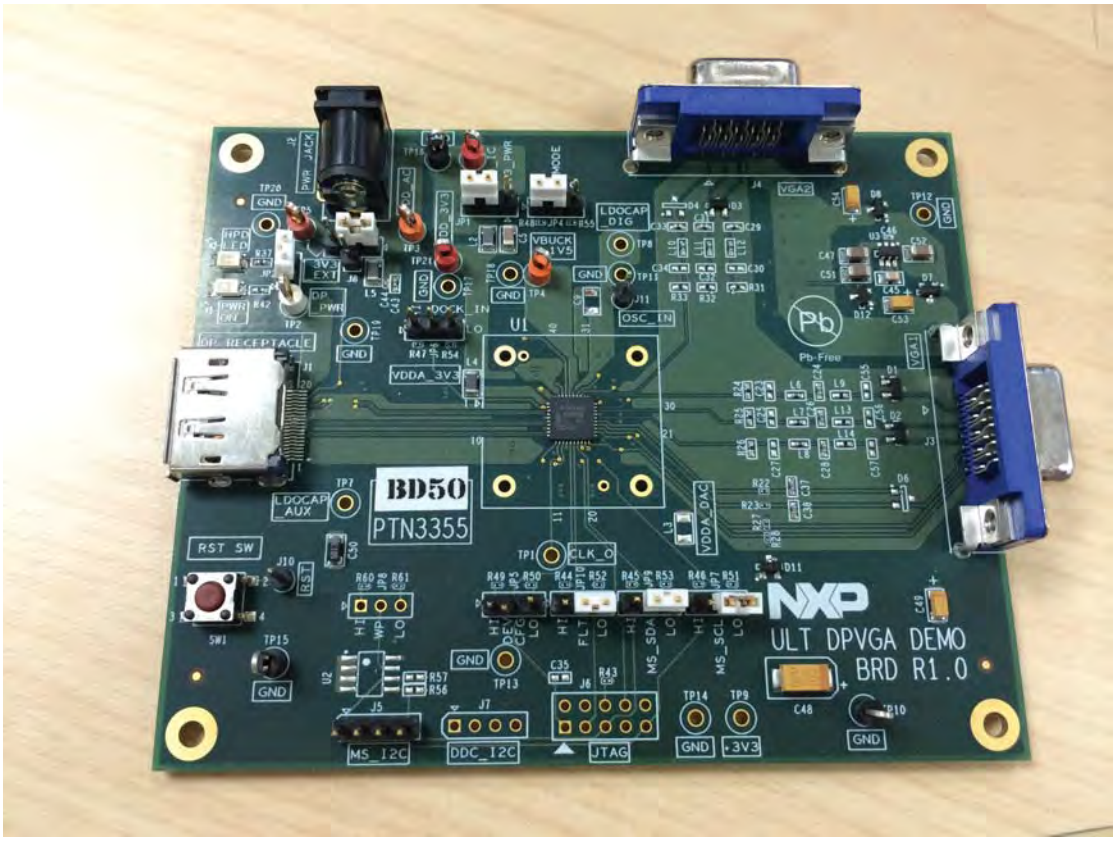

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Fig 3. PTN3355 application board

2.3 PTN3355 ULT DP-VGA application board features

- Stuff options for PT3393 or PTN3355.
- Groups of jumpers for pin configuration.
- Other jumpers for test options.
- One reset button.
- Power LED.
- HPD LED.
- One I2C header bringing out I2C pins (SCL, SDA, GND) to interface with a I^2C-Bird dongle to program (Flash over I2C) and debug.
- One I2C header for DDC control.
- One JTAG for FW download.
- One 3V3 power adapter jack.
- Test point for external power supplies 3.3 V (1A).
- Option to power from DP connector.
- Jumper to select between 3 power sources
- Two VGA connectors selectable by jumper setting.

3. Hardware requirements

- Item 1 - (e)DP sources of Intel, AMD, Apple
- Item 2 - VTG5225-DP or DPT-200, DP sources with DP 1.1 or DP1.0 cable
- Item 3 - DPA-400, AUX analyzer
- Item 4 - Different native resolution monitors
- Item 5 - FS2 with 2x5 JTAG connection for FW download
- Item 6 - I2C Bird with 1x4 header connection for s-EEPROM R/W

4. Board specifications

4.1 General description

- Layers: 4 layers expected - trace, ground, VCC, trace
- Size: 3.5" x 4.5"
- Material: FR4
- Thickness: 62 mil
- Impedance: 50 ohm single-end, 75 ohm single-end RGB, 100 ohm differential on DP and AUX signal pairs.

4.2 PCB stack ups

PCB Stack Up		Impedance			
Thickness (mil)					
e solder mask	0.50 mils	Single		DIFF	
copper+plating	0.70 mils	9.45 mils , 50Ω±10% 3.55 mils , 75Ω±10%	53.09 Ω	5.9/5.5/5.9 mils , 100Ω±10%	101.26 Ω
Prepreg	4.70 mils				
copper	1.40 mils				
core	47.20 mils				
copper	1.40 mils				
Prepreg	4.70 mils				
copper+plating	0.70 mils	9.45 mils , 50Ω±10% 3.55 mils , 75Ω±10%	53.09 Ω	5.9/5.5/5.9 mils , 100Ω±10%	101.26 Ω
ide solder mask	0.50 mils				
TOTAL	61.80 mils 1.57 mm				

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Fig 4. ULT DP-VGA Application Board PCB Stack Up example

4.3 Top assembly drawings of the PTN3355 Application Board

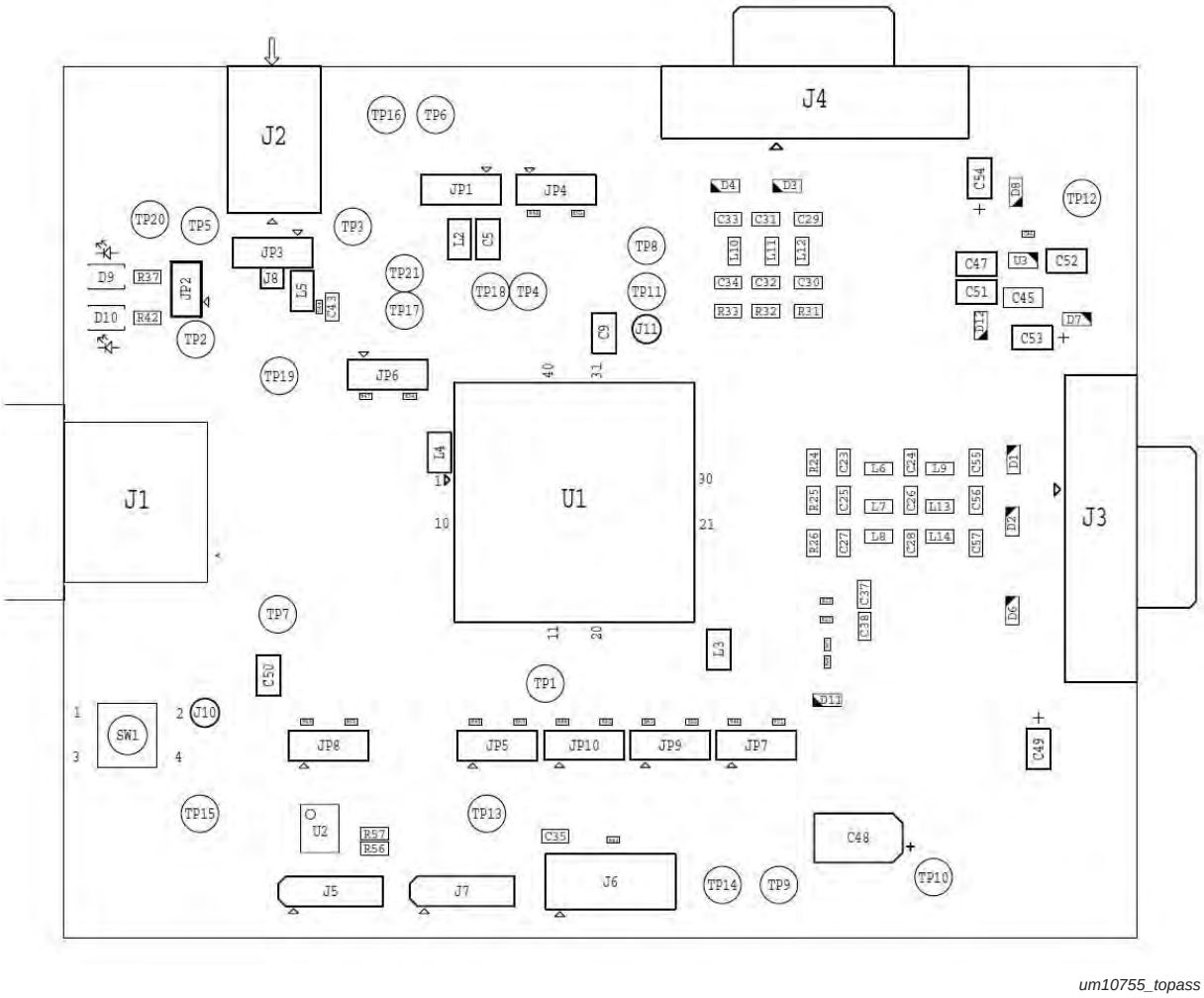

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Fig 5. PTN3355 application board top assembly drawings

4.4 Bottom assembly drawings of the PTN3355 Application Board

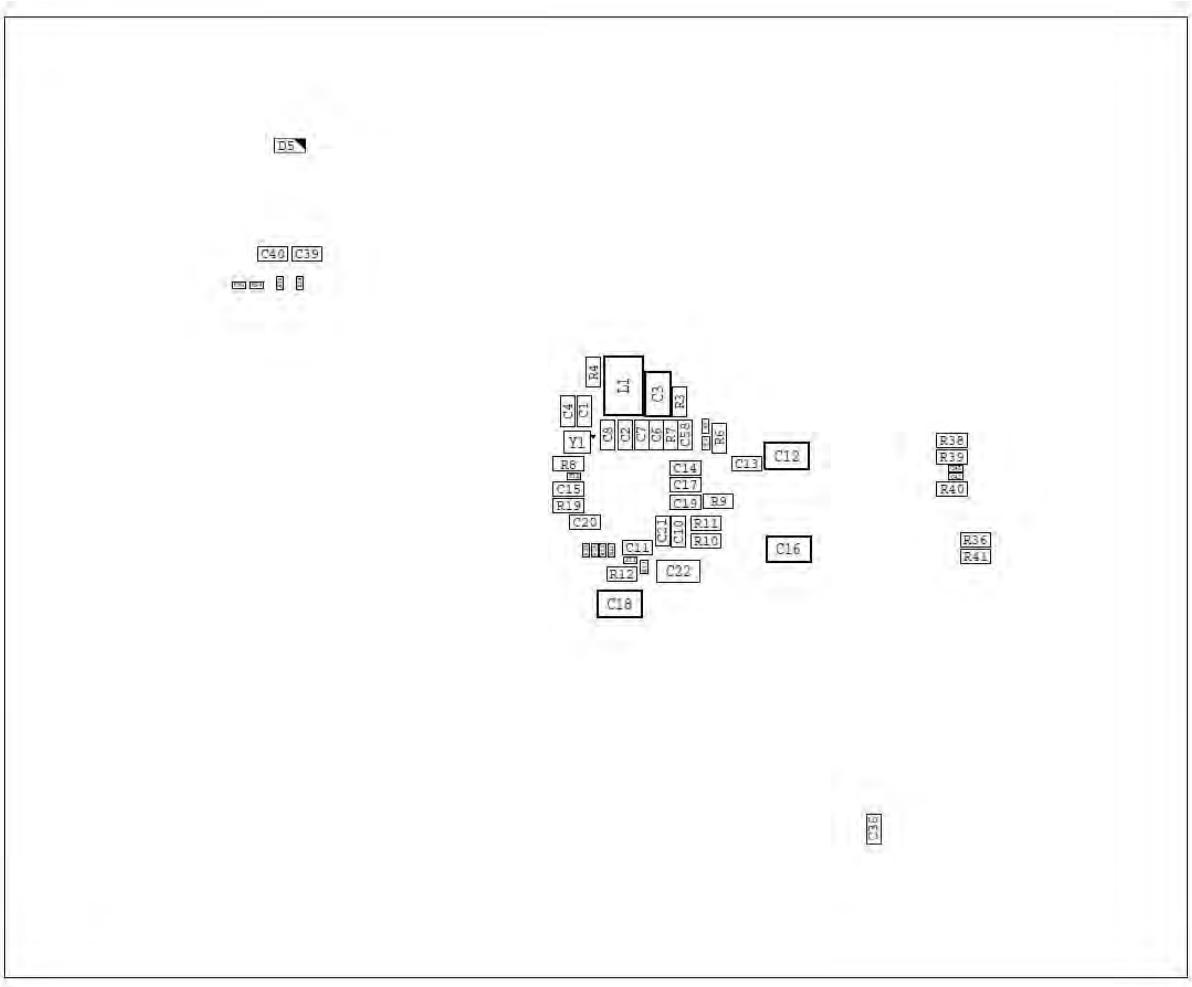

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Fig 6. PTN3355 application board bottom assembly drawings

5. Connector specifications

5.1 Connectors and jumpers

Table 1. Connectors and jumpers

Jumper number	Jumper name	Connector name	Manufacturer	Part number
J1	DP CONN SINK	DP RCPT 20 POS	Molex	47272-0001
J2	POWER JACK	CONN JACK POWER 2.1MM PC	CUI	PJ-102A
J3,J4	VGA_CONN	CONN D-SUB RCPT 15POS HD R/A	EDAC	634-015-274-992
J5,J7	HEADER 4	CONN HEADER .100 SINGL STR 4POS	Sullins	PBC04SAAN

Table 1. Connectors and jumpers *…continued*

Jumper number	Jumper name	Connector name	Manufacturer	Part number
J6	HEADER, 2x5	CONN HEADER .100 DUAL STR 10POS	Sullins	PBC05DAAN
J8,J10,J11	CON1	CONN HEADER .100 SINGL STR 1POS	Sullins	PBC01SAAN
JP1,JP3,JP4,JP5,JP6, JP7,JP8,JP9,JP10	HEADER 3	CONN HEADER .100 SINGL STR 3POS	Sullins	PBC03SAAN
JP2	HEADER 2	CONN HEADER .100 SINGL STR 2POS	Sullins	PBC02SAAN

5.2 Cables

- DP 1.0 cable to power the application board
- DP 1.1 cable for DP communication only
- VGA cable

5.3 Jumper settings

Table 2. Jumper settings

Jumper number	Signal Names	Jumper Settings	Default Setting
JP1	+3V3_IC	1-2, select external power to measure 2-3, select 3-1 power source	2-3
JP2	HPD_ON	1-2 Enable HPD LED OPEN: Disable HPD LED	1-2
JP3 + J8	+3V3_FB	1-2, Select 3V3 power adapter 2-3, Select external power supply JP3-2 to J8-1, Select DP power	1-2
JP4	TESTMODE	1-2 HIGH, CFG[5:1] = JTAG PINS 2-3 LOW, CFG[5:1] = CONFIG PINS. I2C = 40H OPEN, CFG[5:1] = CONFIG PINS. I2C = C0H	2-3
JP5	CFG5_TCK	1-2 HIGH, 33 MHZ XTAL is used OPEN, 27 MHZ XTAL is used 2-3 LOW, 25 MHZ XTAL is used	OPEN
JP6	DOCK_IN	1-2 HIGH, Select VGA2 2-3 LOW or OPEN, Select VGA1	OPEN
JP7	CFG1-MS_SCL/TDI	CFG1, CFG2: 11: Compliant HPD behavior, MS Bus is used 10: Non-compliant HPD behavior	2-3

Table 2. Jumper settings *...continued*

Jumper number	Signal Names	Jumper Settings	Default Setting
JP9	CFG2-MS_SDA/TMS	01: Non-compliant HPD behavior 00: Compliant HPD behavior, MS bus is not used	2-3
JP8	WP	1-2 HIGH, WP for S-EEPROM 2-3 LOW, No WP S-EEPROM	2-3
JP10	CFG3-FLT/TDO	1-2 HIGH, Support FLT 2-3 LOW or OPEN, No FLT support	2-3

6. Power options

PTN3355_3393 application board can be powered by three different methods.

6.1 DP 1.0 cable

Set JP3-2 to J8-1 to select DP power

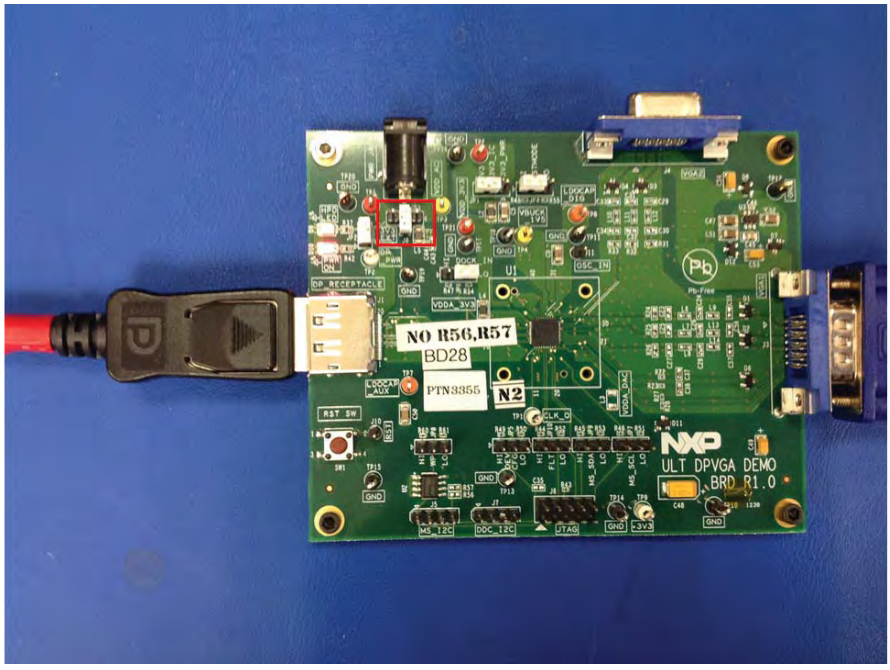

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Fig 7. Power by DP 1.0 cable

6.2 3.3 V power adapter

Set JP3 pin 2 to pin 1 to select 3V3 power adapter

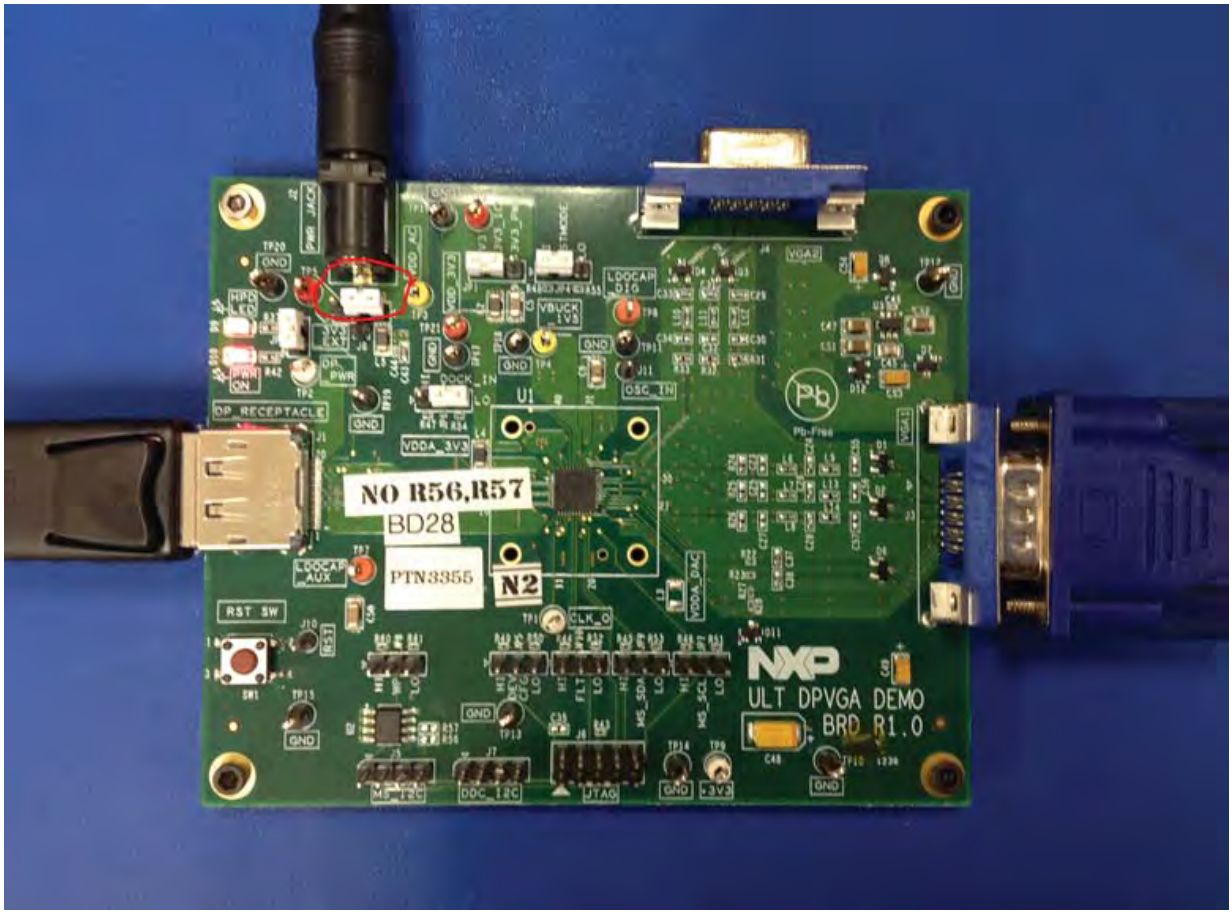

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Fig 8. Power by 3.3 V power adapter

6.3 External power source

Set JP3 pin 2 to pin 3 to select external 3.3V power supply.

Clip 3.3V power lead to TP5, and clip ground lead to GND test point.

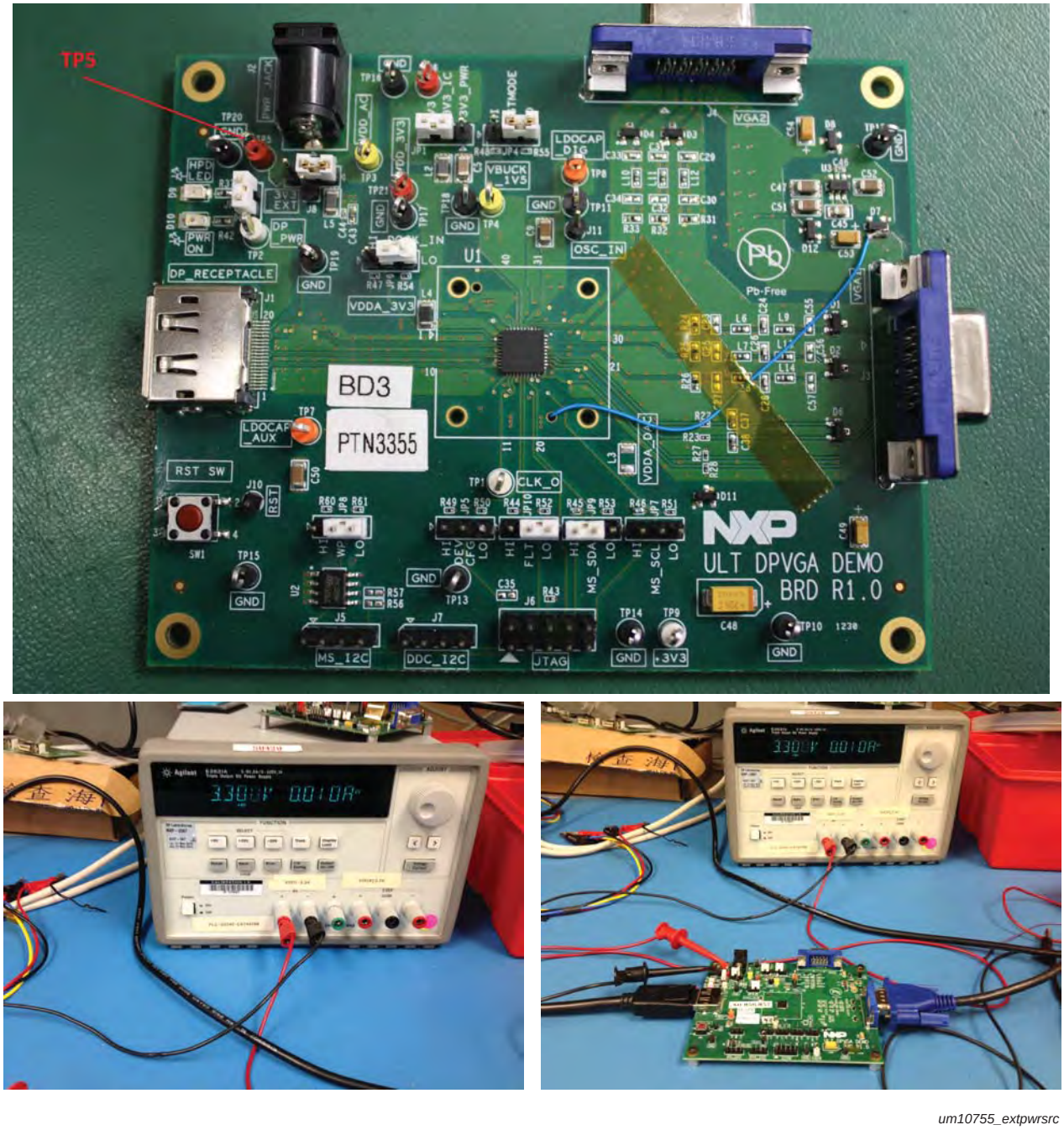

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Fig 9. Power by external 3.3 V power supply (1 of 2)

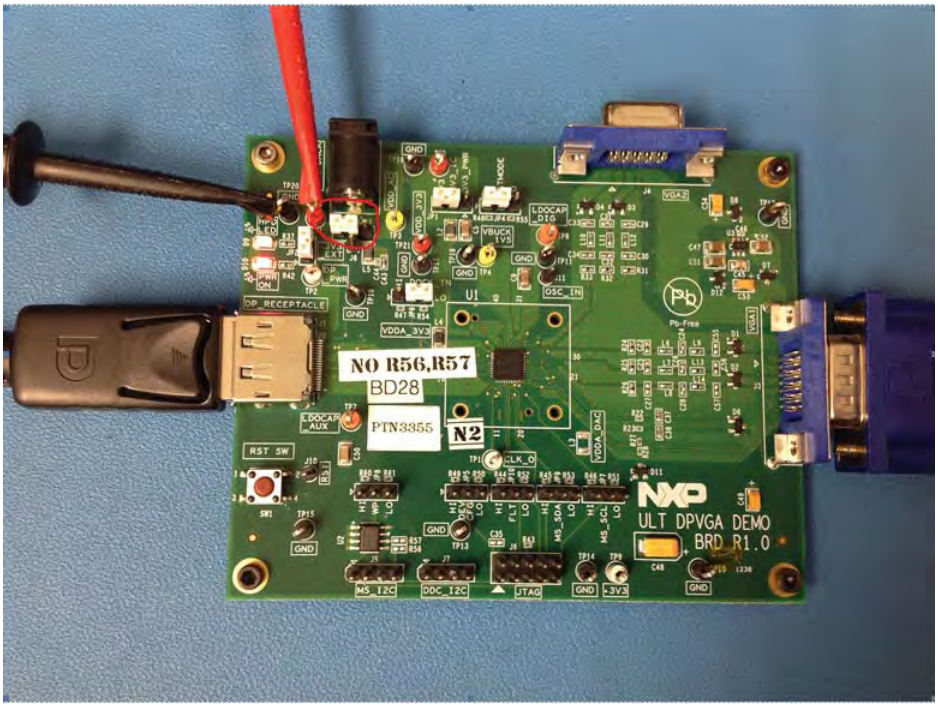

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Fig 10. Power by external 3.3 V power supply (2 of 2)

7. Stuffing options

7.1 PTN3393 stuffing

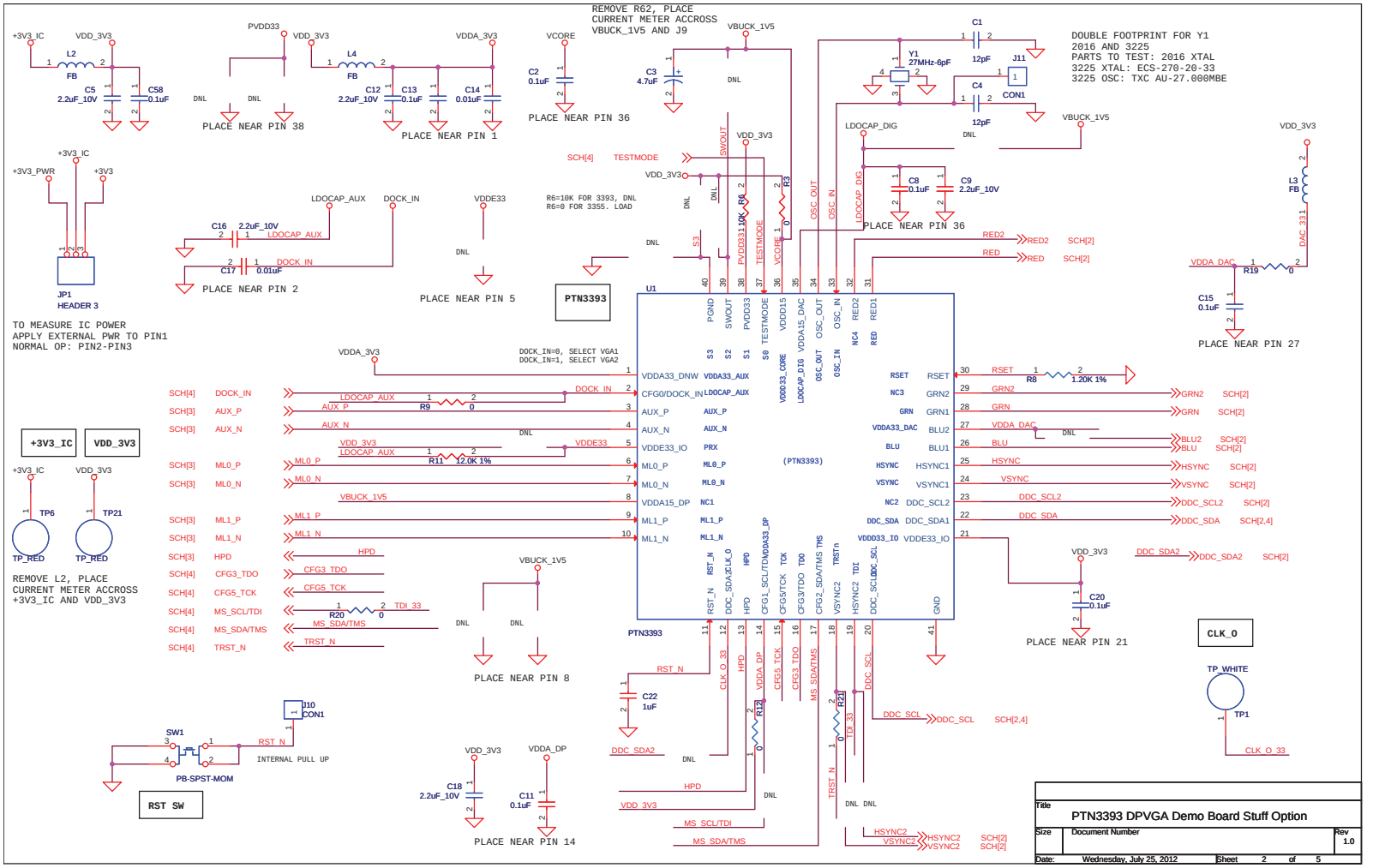
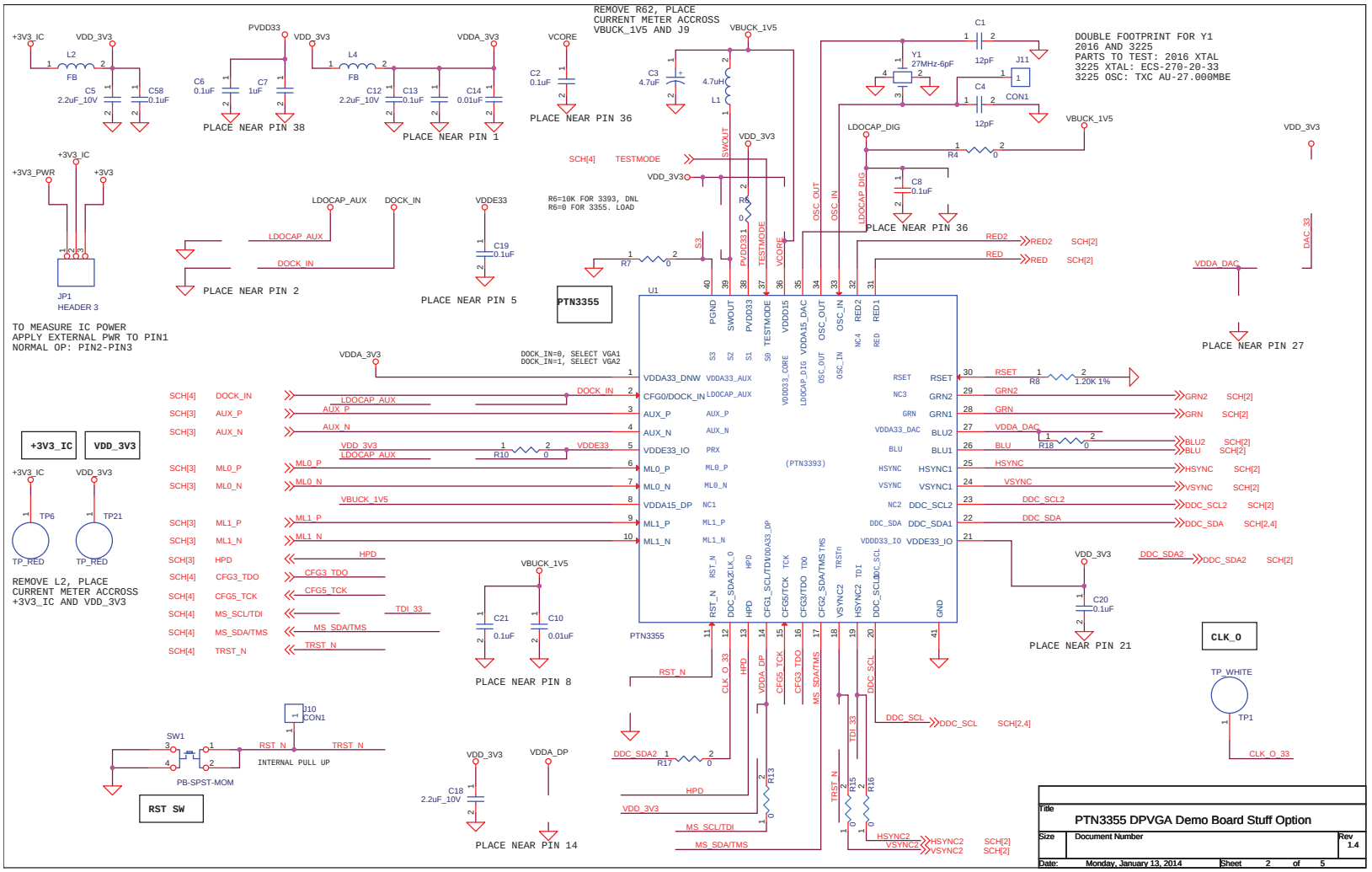


Fig 11. PTN3393 stuffing option design

7.2 PTN3355 stuffing



um10755_3355stuffing

Fig 12. PTN3355 stuffing option design

7.3 PTN3355_PTN3393 stuffing options table

Table 3. PTN3355_PTN3393 stuffing options table

Location	Function/Value	PTN3355	PTN3393
C6	0.1uF	Load	No Load
C7	1uF	Load	No Load
C16	2.2uF_10V	No Load	Load
C17	0.01uF	No Load	Load
C19	0.1uF	Load	No Load
R7	0 Ohm	Load	No Load
R9	0 Ohm	No Load	Load
R10	0 Ohm	Load	No Load
R11	12.0K 1%	No Load	Load
R1	10K	No Load	No Load
R5	10K	No Load	No Load
R6	0 Ohm for PTN3355 10K for PTN3393	Load	No Load
R3	0 Ohm	No Load	Load
L1	4.7uH	Load	No Load
C3	4.7uF	Load	No Load
R4	0 Ohm	Load	No Load
R17	0 Ohm	Load	No Load
C22	1uF	No Load	Load
R12	0 Ohm	No Load	Load
R13	0 Ohm	Load	No Load
R15	0 Ohm	Load	No Load
R16	0 Ohm	Load	No Load
R21	0 Ohm	No Load	Load
R18	0 Ohm	Load	No Load

8. References

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[2] Schematic, PTN3355_1.14_CONFIDENTIAL.pdf

[3] BOM, PTN3355_ONLY_REV14_BOM.xls

[4] AN11413-PTN3393-PTN3355 rev4.pdf

[5] AN11415-PTN3355 rev1.pdf

[6] Allegro layout, PTN3393 DEMO BOARD_REV1_305-PD12-0592_PCB_07-27-2012.brd

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Date of release: 19 January 2015
Document identifier: UM10755