# UM10741

## Fm+ development kit OM13320

Rev. 1 — 1 April 2014 User manual

### Document information

| Info | Content |
|---|---|
| **Keywords** | I2C-bus, Fm+, development tool, PCA9672, PCA9955 |
| **Abstract** | User manual for the Fm+ development board (OM13260) kit (OM13320). |

### Revision history

| Rev | Date | Description |
|---|---|---|
| 1.0 | 20140401 | User manual; initial release |

## Contact information

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# 1. Introduction

The Fm+ Development Kit (OM13320) is intended for several different tasks: from a hands-on introduction, understanding, and use of the I²C-bus (Inter-Integrated Circuit bus), to I²C device evaluation, and as a simple product demonstration platform (for trade shows and sales pitches).

The kit has a core Printed-Circuit Board (PCB) assembly, and three add-on PCBs. Other PCBs are available for advanced use or to support newly-released I²C-bus components as they are introduced to the market.

The Fm+ Development Kit (OM13320) is supported by a Graphics User Interface (GUI) software program that runs on a Personal Computer (PC) under the Microsoft Windows 7 Operation System. In some uses the GUI is not required, and the Fm+ Development Kit (OM13320) can be run as a standalone demonstration, requiring only an external power adapter (not included).

# 2. Key features

### I²C-bus masters

Self-contained PCB with two independent I²C buses

Bus 1: On-card I²C MCU master (NXP **LPC1343**)

Bus 2: NXP LPC Xpresso MCU module (not included), and NXP **PCA9665** bus controller

USB interface to on-card MCU (for connection to a PC running the GUI software)

### I²C-bus slaves

General Purpose Input/Output (GPIO): **PCA9672** (one each on Bus1 and Bus2)

LED driver, with 16 constant current outputs: **PCA9955** (with four RGB and four White LEDs on Bus1)

### Accessory sockets

Connectors for up to four daughter cards, each providing power, Bus1 and Bus2 I²C signals

Connector for the Bus Buffer Board **OM13398** (supplied) containing two **PCA9617A** bus buffers

Connector for a third-party I²C-bus logger or I²C-bus controller (Beagle and Aardvark, from Total Phase)

### I²C buses

I²C-bus voltage: jumper select 5 V (external) or 3.3 V (on-card 3.3 V regulator)

I²C-bus pull-up resistors: jumper select of ‘high’, ‘med’ or ‘low’ loading


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### Other features

SPI ports: One for on-card MCU, two more for LPC Xpresso

Serial Com Port: EIA232 with voltage level shifter and connection to the LPC Xpresso

LED blinker: NXP PCA9901 one-wire with on-card LED

INT (Interrupt) and RST (Reset) Bus signal monitor LEDs (buffered)

Logic probe: Utility LEDs (buffered) to monitor signals by user jumper wire connection

External DC input (6 V DC maximum)

Prototype area: Uncommitted 8 × 8 100 mil pitch tie points for end user component attachment

Test points and ground: for probe attachment to major signals

Connection of both $I^2C$ buses together (supplied 2-wire jumper)

# 3. Fm+ development kit quick tour

## 3.1 Kit contents

Before using the kit for the first time, please familiarize yourself with the various components listed in Table 1. See Figure 1.

**Remark:** Each PCB assembly is shipped in an anti-static bag. After the first use, these may be discarded to simplify future storage.


a. Top layer

b. Bottom layer

**Fig 1. Fm+ development kit**


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**Table 1. Fm+ development kit contents**

| Components |
|---|
| Fm+ development board (OM13260) |
| GPIO target board (OM13303) |
| PCA9617A bus buffer demo board (OM13398) |
| Bridge board (OM13399) |
| Cable, USB Type A to Type B |
| Ribbon cable, 10 position (bag of two) |
| Jumper wires with female terminals (bag of ten) |
| Shorting jumpers (bag of twenty) |
| Hardware (bag of M3 screws and standoffs) |

### 3.1.1 Box contents

The Fm+ Development Kit (OM13320) contains four PCB assemblies, cables, and loose hardware. These should be retained in the box for future access. Depending upon the desired use, some of the PCB assemblies may be attached to each other, either by plug connection or by ‘stacking’ the GPIO PCB assemblies above the Fm+ Development Board (OM13260), using the supplied ribbon cables and hardware.


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## 3.2 Supplied PCB assemblies

There are four PCB assemblies in the kit. Each has a specific function and not all of them are used at the same time.

### 3.2.1 Fm+ Development Board (OM13260)

The large PCB, Figure 2, contains two separate I²C-bus structures, together with supporting circuitry. Each bus has a bus master, one or more bus slaves, and user options to change the bus voltage and bus pull-up resistors. Adjusting these changes the operation of the buses to suit various goals. In addition, the two buses may be linked together to operate a one I²C-bus structure. This can be done with a two-wire jumper (supplied) or the Bus Buffer Board OM133998 (supplied). See figure 3.5. Four identical ports provide access for add-on boards that contain additional I²C-bus devices.

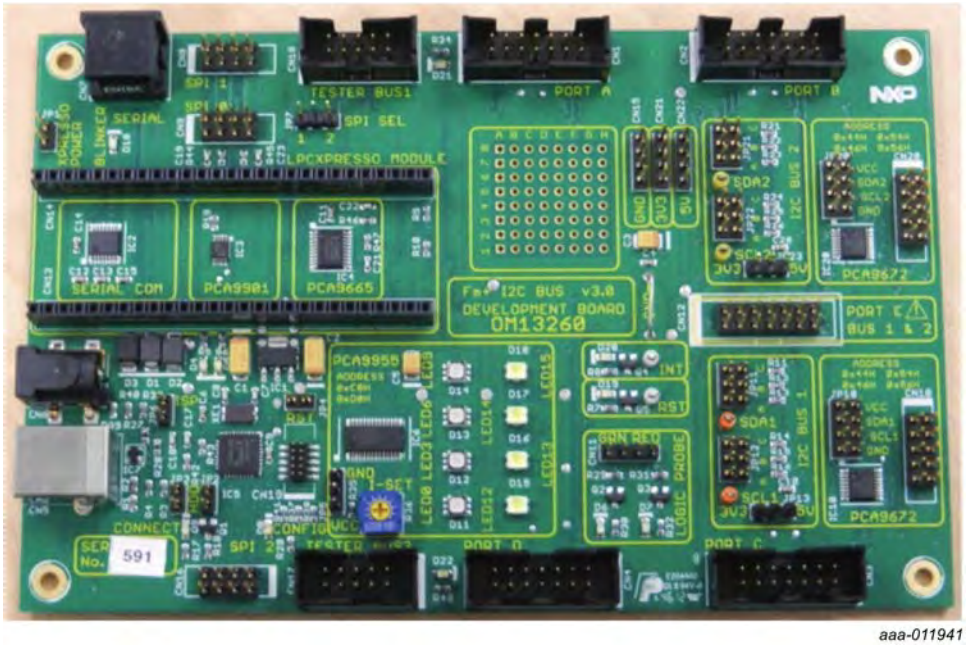


**Fig 2. OM13260 Fm+ development board PCB assembly**


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### 3.2.2 GPIO target board (OM13303)

Outputs from the GPIO devices on the Fm+ Development Board (OM13260), and those when using GPIO daughter cards (not supplied in the kit), require the GPIO Target Board (OM13303). Each one has eight channels of LED indicator and push-button switches for user input. See Figure 3.


**Fig 3. OM13303 GPIO target board PCB assembly**

### 3.2.3 PCA9617A bus buffer demo board (OM13398)

Bus buffers bridge two $I^2C$-bus segments, which are provided on the Fm+ Development Board (OM13260) by Bus1 and Bus2. Bus buffer daughter cards, such as the PCA9617A Bus Buffer Demo Board (OM13398) (supplied in the kit) can be installed directly on Port E (CN12). See Figure 4.


**Fig 4. OM13260 bus buffer PCB assembly**


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### 3.2.4 Bridge board (OM13398)

Some existing Demo Boards used a single row connector with nine pins. To use these with the Fm+ Development Kit requires the Bridge Board (OM13399, supplied in the kit). See Figure 5.


**Fig 5. OM13399 bridge board PCB assembly**

### 3.2.5 Daughter cards (not supplied in the kit)

These are not in the OM13230 kit, and should be obtained separately. Daughter cards hedge against obsolescence so that the Fm+ Development Kit (OM13320) can be used with future devices by adding newly released daughter cards as they become available. An example daughter card is shown in Figure 6.


**Fig 6. Example daughter card PCB assembly**


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# 4. First time setup: Fm+ development board kit (OM13320)

## 4.1 Before you begin

To use the Fm+ Development Kit (OM13320) for the first time requires some hardware setup and installation of both firmware (on the Fm+ Development Board OM13260) and software on the attached computer.

The following three steps must be completed:

1. Install Jumpers on the Fm+ Development Board (OM13260) (see Section 4.3).
2. Install Firmware on the Fm+ Development Board (OM13260) (see Section 4.6).
3. Install the NXP GUI Software on the computer to be used with the kit (see Section 4.7).

## 4.2 First time setup of the Fm+ development board (OM13260)

Several jumpers must be installed before using the Fm+ Development Board (OM13260) PCB. The on-board microcontroller (MCU) must contain the appropriate firmware.

To install the firmware requires the connection to a Personal Computer (PC) running Microsoft Windows 7/64 Operating System and a USB port.

## 4.3 OM132680 jumpers

The jumpers and their function are shown in Table 2. Using Figure 7 and the table data, install the jumpers.

**Table 2. OM13260 jumpers**

| Jumper | Label | Function | First time |
|---|---|---|---|
| JP1 | XPRESSO POWER | | Close |
| JP2 | HDD | | Open |
| JP3 | CONNECT | | Close |
| JP4 | RST | | Open |
| JP5 | | PCA9955 address | GND |
| JP6 | ISP | | Open |
| JP7 | SPI SEL | | 1 |
| JP10 | | PCA9672 address | GND |
| JP11 | | SDA1 pull-up | A |
| JP12 | | SCL1 pull-up | A |
| JP13 | | Bus1 bus voltage | 3V3 |
| JP20 | | PCA9672 address | GND |
| JP21 | | SDA2 pull-up | A |
| JP22 | | SCL2 pull-up | A |
| JP23 | | Bus2 bus voltage | 3V3 |


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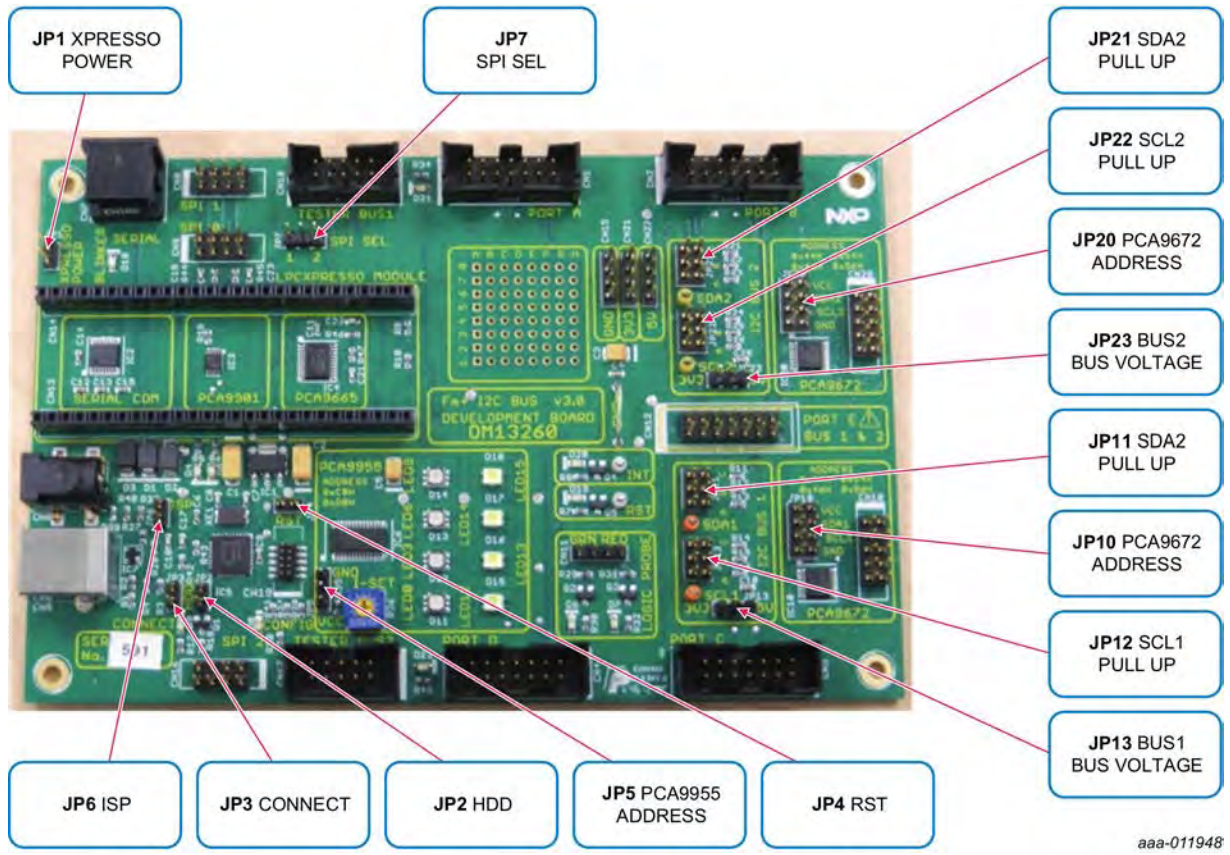


**Fig 7. OM13260 test point locations**

## 4.4 OM13260 Port E bypass

Depending up the intended operation of the Fm+ Development Board (OM13260), Port E (CN12) should be left open, or linked with a jumper wire, or for the attachment of a Bus Buffer Board. The PCA9617A Bus Buffer Demo Board (OM13398) is supplied in the kit.

For the purpose of this quick setup section, install the two-wire jumper (supplied) as shown in Figure 8.

**Remark:** The two-wire jumper requires a twist, as shown. The diagonally opposite pins are linked.


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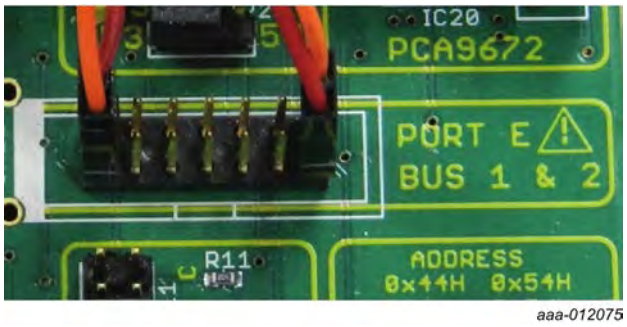


**Fig 8. OM13260 Port E jumper**

## 4.5 OM13260 mounting hardware

To prevent damage to the table surface, it is recommended that metal hardware (supplied in the kit) is installed in the four mounting holes. This raises the PCB assembly about 6 mm. See Figure 9.

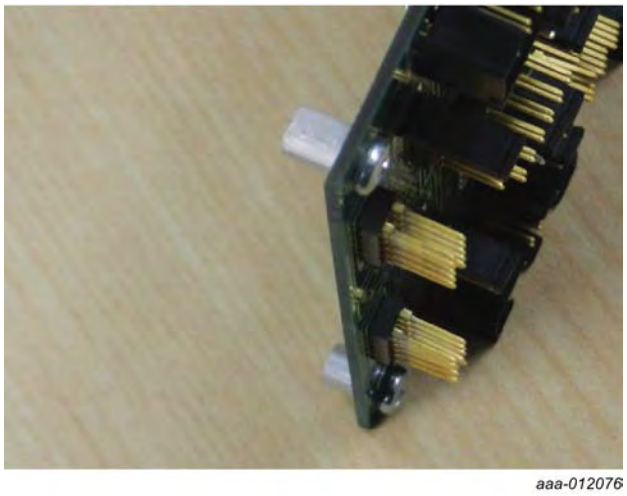


**Fig 9. OM13260 mounting hardware**

**Remark:** Save the completed Fm+ Development Board, now install the NXP USB Driver.


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## 4.6 NXP firmware installation

The micro on the Fm+ Development Board needs firmware running on it to interface with the GUI running on a Windows 7 PC over USB. The board is shipped with a blank microprocessor, so user action is necessary for proper operation.

An installation user manual UM10785 (Ref. 1) is available at for a complete explanation of the process. A quick overview is presented here.

1. Download **NXP_Fm+_Eval_Board_V1_0_firmware.zip** from www.nxp.com/demoboard/OM13320.html#documentation
2. Connect a USB cable from the PC USB port to CN5.
3. Install the Connect (JP3) jumper to connect the USB communications.
4. Install the ISP (JP6) jumper to put the MCU into In-System Programming mode.
5. Install and then remove RST (JP4) jumper to reset the MCU.
6. The MCU will enumerate on the PC as a disk drive called CRP_DISABLD.
7. Delete the file on the MCU (size may vary — up to 32 kB).
8. Copy the new firmware file **NXP_Fm_Eval_Board_V1_0.bin**, extracted from the zip file to the MCU.
9. Remove the ISP (JP6) jumper.
10. Install and then remove RST (JP4) jumper to reset the MCU.

## 4.7 NXP GUI installation

A Graphical User Interface (GUI) is provided which allows easy manipulation of the devices included on the Fm+ Development Board and many others that can be connected to the board via daughter cards.

An installation user manual UM10785 (Ref. 1) is available for a complete explanation of the process. A quick overview is presented here.

1. Download **NXP_Fm_Board_V1_0_Installation.zip** from www.nxp.com/demoboard/OM13320.html#documentation
2. Extract **NXP Fm+ Board V1.0 Installation.exe** and run.
3. Follow the instruction prompts. Select the default answers.

This GUI uses a USB Human Interface Driver (HID), so no driver installation is required.

If the firmware and GUI installs are successful, an Fm+ Development Board block diagram is displayed when the GUI executes (Figure 10).


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# 5. Fm+ development board (OM13260)

The Fm+ Development Board (OM13260) PCB assembly is self-contained, requiring only DC power to operate. Depending upon the firmware installed on the Fm+ Development Board (OM13260), it can also operate with a connected Personal Computer (PC) via a USB cable.

The modular design of the kit and this board in particular allows accessory boards to be easily connected.

## 5.1 Theory of operation

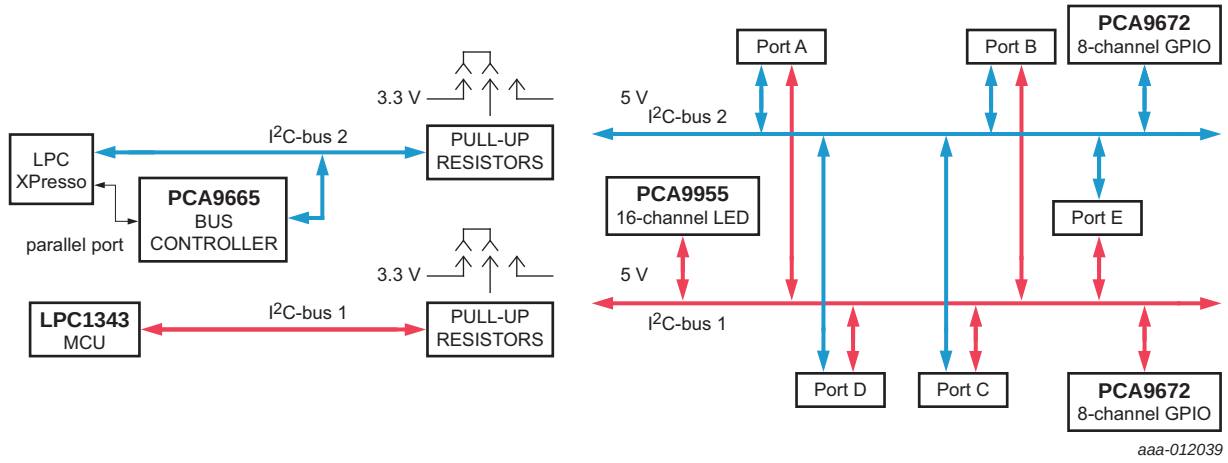


**Fig 10. Fm+ development board bus structure**

An I²C-bus requires a Master and one or more Slaves. The two bus signals, clock SCL and data SDA, are wired-OR and require pull-ups to a DC power supply. Two similar but separate I²C buses each support one Master and at least one Slave device on the board. The two buses may be linked by either a Bus Buffer Board (OM13398 supplied in the kit) or a wire jumper, at the Port E connector (CN12).

The signals from both buses are available simultaneously at each of four connectors, Port A through Port D (CN1 through CN4, respectively). These are intended for attachment of accessory daughter cards, which will be made available as future I²C-bus devices are released.

The size of the pull-up resistors can be changed by moving shorting jumpers (JP1, JP2, JP11, and JP12), providing selection of ‘Low’ ‘Med’ and ‘High’ resistor values scaled to the Fm+ I²C-bus drive strength. When both buses are joined by a jumper wire, the pull-ups are effectively in parallel, and have one-half the stated resistance values.

Operating voltage of the I²C-bus depends upon the shorting jumpers (JP13 and JP23) that select either 3.3 V or 5 V connected to the pull-up resistors. Compliant I²C-bus devices can tolerate 5.5 V (maximum), regardless of the device operating voltage.


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Each bus has a GPIO 8-bit Slave device (PCA9672, IC10 and IC20), and Bus 1 also has an LED Driver 16-channel device (PCA9955, IC6). All sixteen outputs are connected to LEDs, for visual indication. The 8-bit GPIOs require connection of GPIO Target Boards (OM13303, supplied in the kit) to both indicate the output using eight LEDs and allow user input from eight push switches.

An NXP LPC1343 Microcontroller (MCU) serves as both the Bus 1 Master, and the USB link. The firmware on the MCU can be replaced by the In-System Programming (ISP) mode, with data sent over the USB link (CN5).

Bus 2 has a Parallel to $I^2C$-bus Controller device (PCA9665, IC6), which is to be driven by an optional NXP LPC Xpresso module (not supplied). That module is also an $I^2C$ Master and connected to Bus 2.

**Remark:** Although Bus 2 has more than one $I^2C$ Master, only one is active at any time.

The remaining circuitry is to support the $I^2C$ devices, and provide communications with the PC over a USB link.

The main operating voltage on the Fm+ Development Board (OM13260) is 3.3 V supplied from a linear regulator (IC1). Some circuits and the optional $I^2C$-bus pull-ups may run from 5 V derived either from the USB host (typically a PC) or an AC-DC power supply (not supplied in the kit). The actual voltage is seldom 5 V, due to cable losses, plus an additional drop in a series connected diode used to OR the two inputs. Whichever has the highest voltage has priority.

A shunt Zener diode (6.2 V) protects the board from reverse polarity and overvoltage at the DC Power connector (CN6).

To aid in understanding digital signal levels on the board, two ‘logic probe’ circuits are provided. These are buffered LEDs (Green, D6 and Red, D7), which light if their respective inputs (CN11) are grounded.

Two global digital signal nets, called INT (interrupt) and RST (reset) connect all $I^2C$-bus devices on the board and also the Port A – Port E Daughter Card connectors. These are also connected to the Master (MCU, IC5) on Bus 1, the Master (Bus Controller, IC4), and the LPC Xpresso module.

**Remark:** The $I^2C$ global Reset is not the same as the MCU Reset. Resetting the MCU will only reset the $I^2C$-bus if the MCU firmware is intended to create a global reset.

The test points provide monitoring of interrupts (usually generated by $I^2C$-bus Slaves) and software reset of Fm+ class $I^2C$-bus devices that have that feature.

Additional buffered LEDs are provided (D19, RST and D20, Interrupt) on the Fm+ Development Board (OM13260) for visual indication.

Various MCU and LPC Xpresso signals are made available through additional connectors. These include a serial Port (CN7) with EIA232 voltage level translation (IC2) and SPI Bus signals (SP0, CN9 and SP1, CN8) from the LPC Xpresso module, together with SPI Bus (SP2, CN16) from the MCU (IC5).

A prototyping area is provided for solder connection of components that may be required by an application circuit beyond this board’s design. Power supplies and other signals are readily available.


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On the Fm+ Development Board (OM13260) V3.0 there is an LED Blinker device (PCA9901, IC3) and LED indicator (D10), while not strictly an $I^2C$ device as it uses a one-wire protocol, it belongs to the NXP $I^2C$-bus product portfolio.

**Remark:** The PCA9901 will be made obsolete, and will not be present on future versions of the Fm+ Development Board (OM13260).

The operation of the Fm+ Development Board (OM13260) is greatly enhanced by third-party tools (not supplied in the kit) that may be attached to either $I^2C$-bus through dedicated connectors (Bus1, CN17 and Bus2, CN18), labeled 'TESTER'.

## 5.2 Circuit description

The schematic diagram has multiple sheets. For clarification, only fragments of the schematic are shown here. The full schematic should be downloaded if required. The following pages are divided in to several sections covering the power supply, USB interface, Bus1, Bus2, and support circuits.

### 5.2.1 Power supply

The Fm+ Development Board (OM13260) operates from DC, either from the USB Host connector (CN5) or an optional external AC-DC power adapter (not supplied in the kit) via connector (CN6). See Figure 11 and Figure 12. Selection of the power source is automatic, using ORing diodes (D1 and D2). The main power on the Fm+ Development Board (OM13260) is 3.3 V from a linear regulator (IC1), but some of the circuits are powered directly from the incoming supply, which is a nominal 5 V. Linear regulator (IC1) uses the PCB bottom layer copper as a heat sink. The Fm+ Development Board (OM13260) external DC input is protected against reverse polarity or overvoltage by Zener diode (D3). Both input sources are scaled by resistor dividers (R1, R2 and R39, R40) and fed to the MCU (IC5) Port1 ADC inputs for voltage level monitoring. The VBUS from the USB Host is fed to the MCU Port 0 so that the MCU can detect that a USB connection is available. Green LED (D4) confirms 5 V, and Green LED (D5) confirms 3.3 V.


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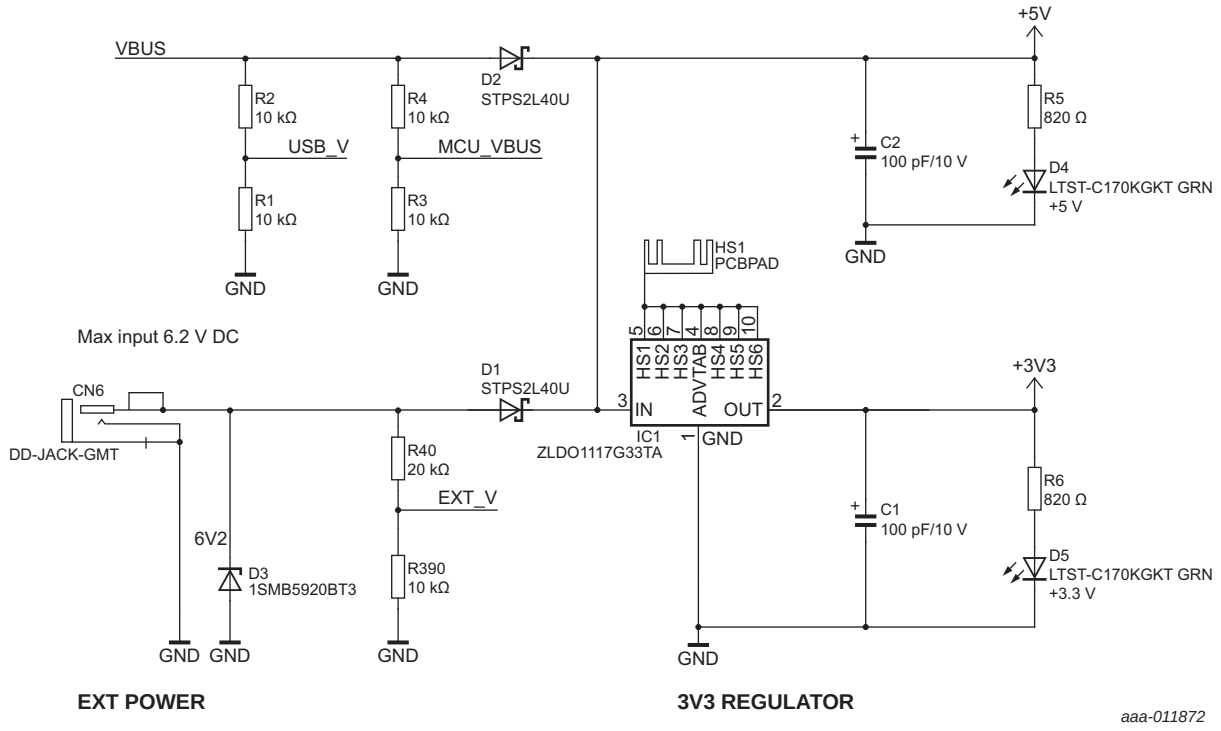


**Fig 11. Power supply**

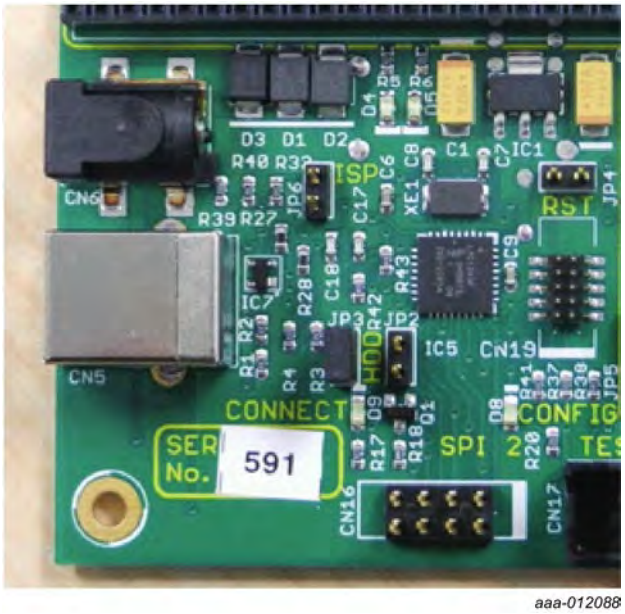


**Fig 12. Power supply and USB section**


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### 5.2.2 USB interface

The USB Host connector (CN5) provides DC power and USB connectivity using the MCU (IC5) hardware interface, see Figure 12 and Figure 13. USB data lines are terminated by resistors (R27 and R28) and protected by an ESD network (IC7). To signal to the host that the USB connection is required, the USB signal DP is pulled to 3.3 V via a resistor (R18) and a transistor (Q1). USB Connection is controlled by the MCU (IC5) via signal CON_EN and can be disabled by removing a jumper (JP3) 'CONNECT'. When the MCU requests a USB connection, and the jumper (JP3) is installed, the green LED (D9) is ON. MCU activity is displayed by the Heart Beat green LED (D8), which is set to blink at about one per second.

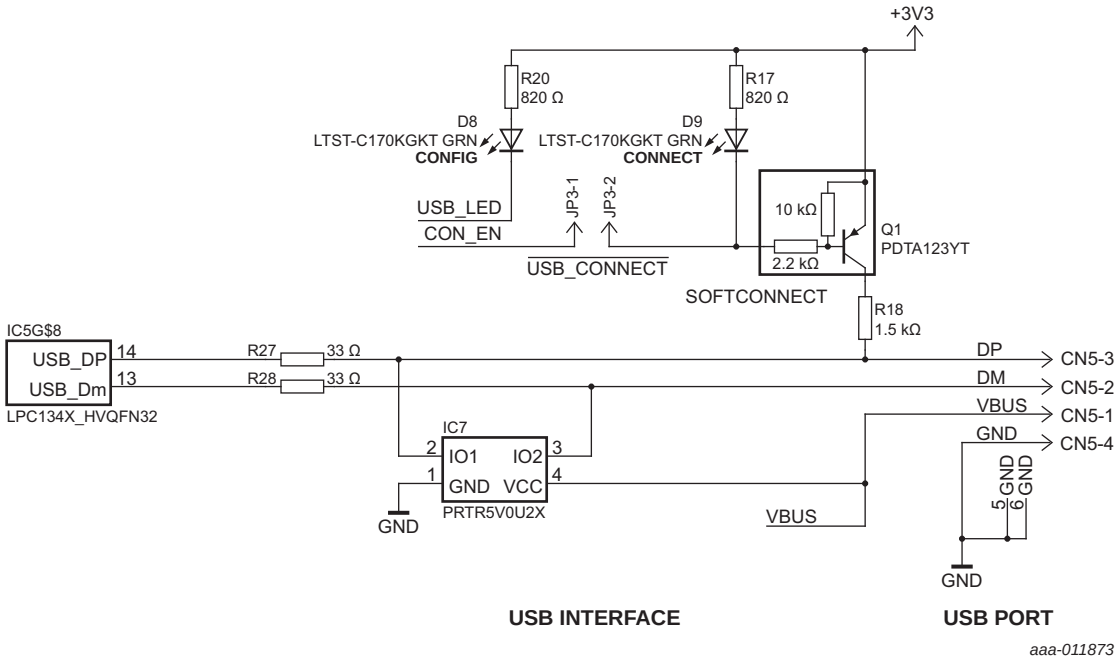


**Fig 13. USB interface**

## 5.3 Bus one (Bus1)

There are two almost identical $I^2C$ buses on the Fm+ Development Board (OM13260), called Bus1 and Bus2. These share a ground and power connection but may be operated independently.

**Remark:** The bus voltage for each $I^2C$ may be different (for example 3.3 V for one $I^2C$-bus, 5 V for the other $I^2C$-bus).

### 5.3.1 Bus1 master (MCU LPC1343)

Microcontroller (MCU) (LPC1343, IC5) serves as the Bus1 Master and the USB Bridge. Firmware installed on the Fm+ Development Board (OM13260) is stored in non-volatile memory, which has a limit of 32 kB. The MCU may be programmed through the USB port or the JTAG connector (CN 19), using Single Wire Debug (SWD), see Figure 14 and Figure 15.


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During programming or at other times it may be necessary to reset the MCU, by briefly shorting JP4 (see Figure 15).

**Remark:** An MCU Reset is not the same as an I²C Bus Reset. Resetting the MCU will not affect the I²C-bus, unless the MCU firmware is designed to issue an I²C Bus Reset when it is reset.

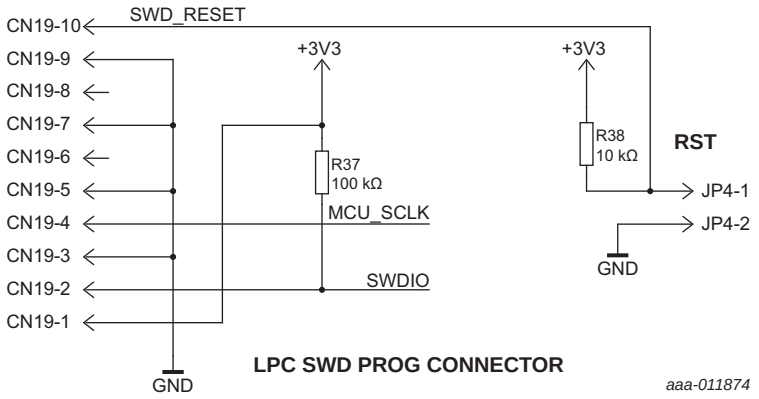


**Fig 14. MCU SWD interface**


**Fig 15. MCU SWD interface section**

MCU Port0 and Port1 provide most of the signals used by the Fm+ Development Board (OM13260), see Figure 16 and Figure 17. I²C Bus1 is connected to the MCU Port0 via RC edge rate control networks that provide bus fall time control (SCL1: R42 and C18; SDA1: R43 and C17).


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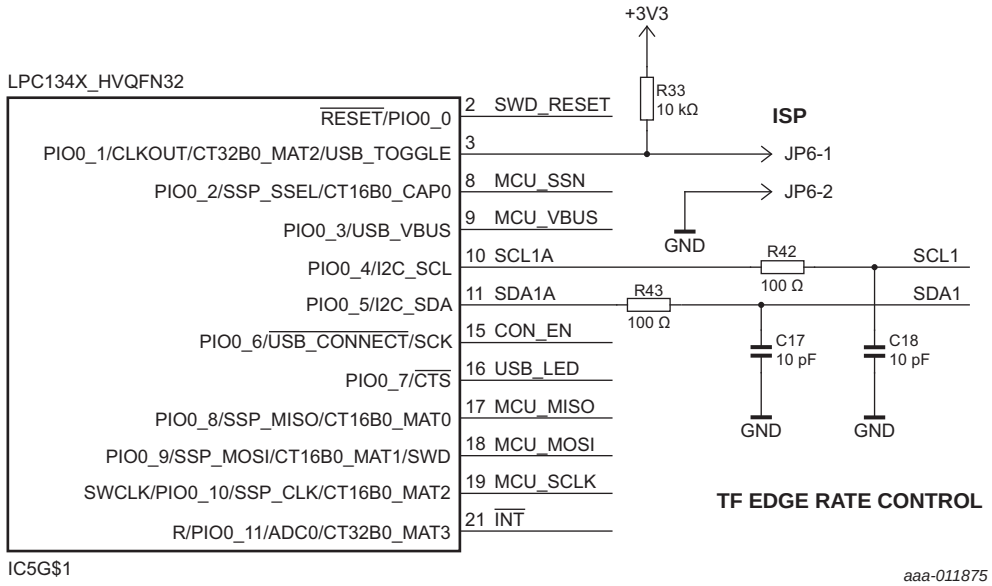


**Fig 16. IC5 MCU Port0**

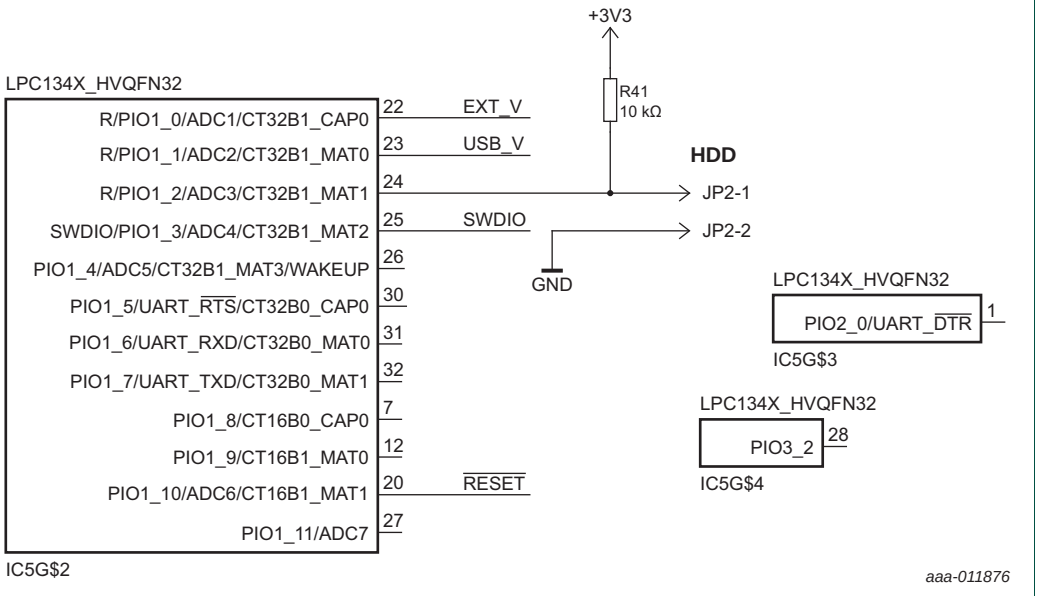


**Fig 17. IC5 MCU Port1**

The HVQN32 package has a thermal pad ground connection, and operates from the main 3.3 V supply. The MCU operates with a 12.00 MHz crystal controlled oscillator. The frequency value and accuracy is necessary for correct USB timing (see Figure 18).


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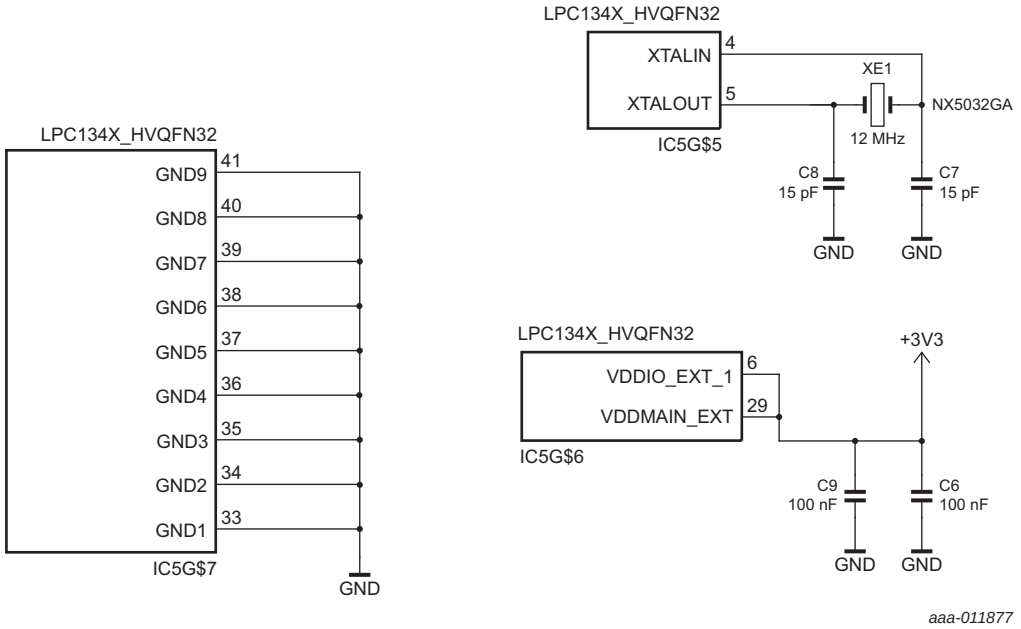


**Fig 18. IC5 MCU Port1, oscillator and power supply**

### 5.3.2 Bus1 pull-up resistors

The Bus1 is pulled up to either the 3.3 V or 5 V supplies via JP13. Three different value pull-up resistors are provided by jumper selection, JP11 and JP12. The values of the pull-up resistors are shown in Table 3. Separate pull-ups are provided for the SCL and SDA signal lines. Bus2 has a similar arrangement. See Figure 19 and Figure 20.

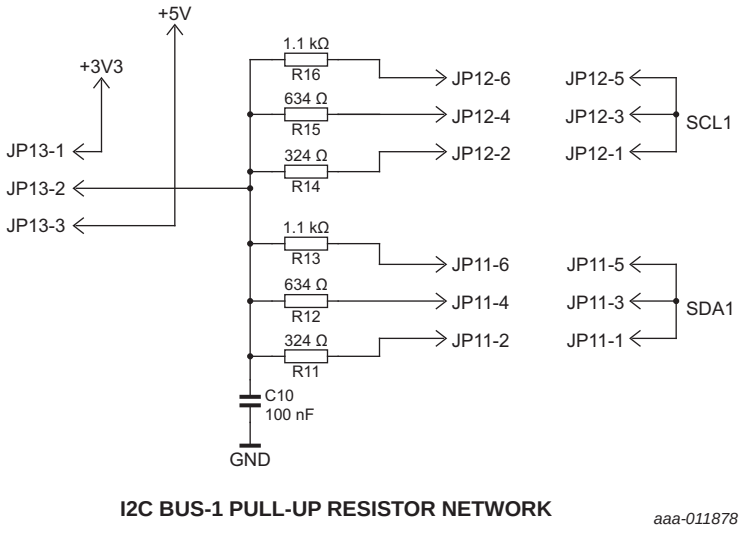


**Fig 19. Bus1 pull-ups and bus voltage selector**


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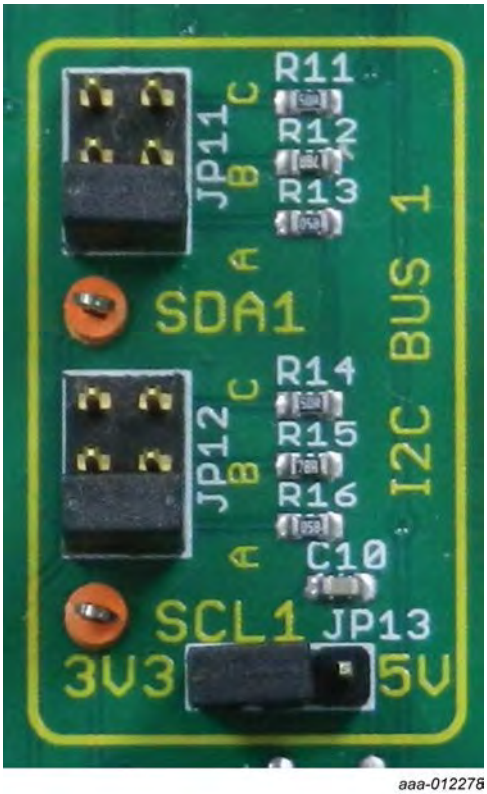


**Fig 20. Bus1 pull-ups section**

**Table 3. Bus pull-up resistors**

| Strength | Position | Value | Bus1 SCL | Bus1 SDA | Bus2 SCL | Bus2 SDA |
|---|---|---|---|---|---|---|
| LOW | A | 1.1 kΩ | R16 | R13 | R26 | R23 |
| MID | B | 634 Ω | R15 | R12 | R25 | R22 |
| HIGH | C | 324 Ω | R14 | R11 | R24 | R21 |

### 5.3.3 LED driver slave (PCA9955)

Bus1 is also used to control the LED Driver (PCA9955, IC6). The LED Driver has constant current outputs and is directly connected to the LEDs, without customary series resistors. The LEDs are powered directly from the 5 V supply, thus avoiding further power dissipation in the 3.3 V linear regulator, IC1. The sixteen channels drive eight LED clusters consisting of four White LEDs (LED12 – LED15) and four RGB LED clusters (LED0 – LED11). The maximum current available for each channel is set by R35 and the variable resistor R36. The LEDs use the PCB top metal for heat dissipation, the LED driver is in the HTSSOP28 package has a thermal pad ground connection, and operates from the main 3.3 V supply. See Figure 21 and Figure 22.


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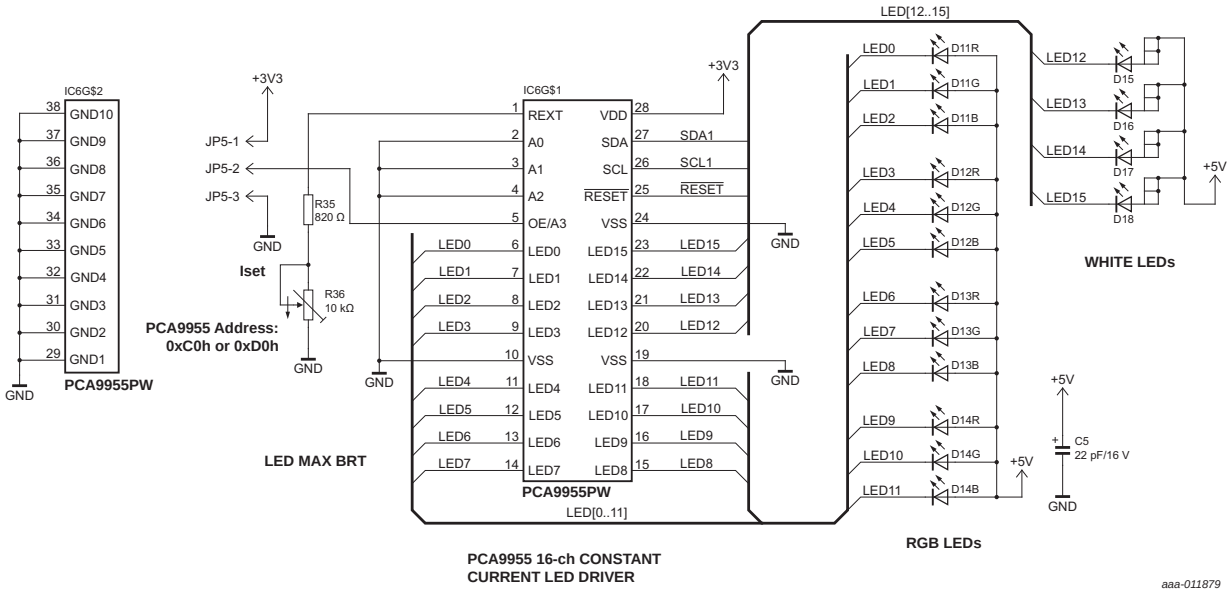


**Fig 21. Bus1 LED driver 16-channel**

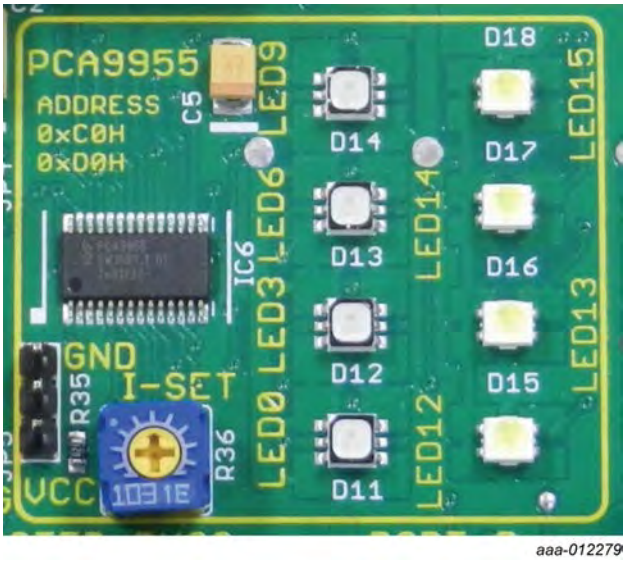


**Fig 22. Bus1 LED driver 16-channel section**

Operation of all sixteen LEDs at maximum current will overheat the LED driver, which is protected by an internal thermal limiter. The device will shut down and recover when the temperature has fallen.

When powered from the USB port (CN5) the USB Host is typically limited to 500 mA, and it will shut down before the LEDs reach maximum current. Operation from an external DC power supply connection (CN6) is required to drive the LEDs to the maximum current per channel of 57 mA, for a total of approximately 1 A.


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The recommended AC-DC adapter is Digikey PN: 62-1132-ND (not supplied). See Figure 23.


**Fig 23. AC-DC adapter, 6 V, 2 A**

The Slave address is set by JP5, summarized in Table 4.

**Remark:** The PCB is marked with hexadecimal (8-bit) address data, but data sheets and the NXP GUI use the 7-bit address values. See Table 4.

**Table 4. LED driver address selection**

| JP5 connected to | Hexadecimal 8-bit address | | | NXP 7-bit address | | |
|---|---|---|---|---|---|---|
| | Address | MSB | LSB | Address | MSB | LSB |
| GND | 0xC0 | 1100 | 0000 | 0x60 | 110 | 0000 |
| $V_{CC}$ | 0xD0 | 1101 | 0000 | 0x68 | 110 | 1000 |

### 5.3.4 GPIO slave (PCA9672)

The GPIO (PCA9672, IC10) is connected to Bus1, and provides eight input/output channels at CN10. Jumper JP10 sets the device address to one of four options, depending on whether the A0 pin is connected to GND, $V_{CC}$, SCL, or SDA. Bus2 has a similar arrangement for a second GPIO (PCA9672, IC20). See Figure 24 and Figure 25.

**Remark:** The PCB is marked with hexadecimal (8-bit) address data, but data sheets and the NXP GUI use the 7-bit address values. This is summarized in Table 5.


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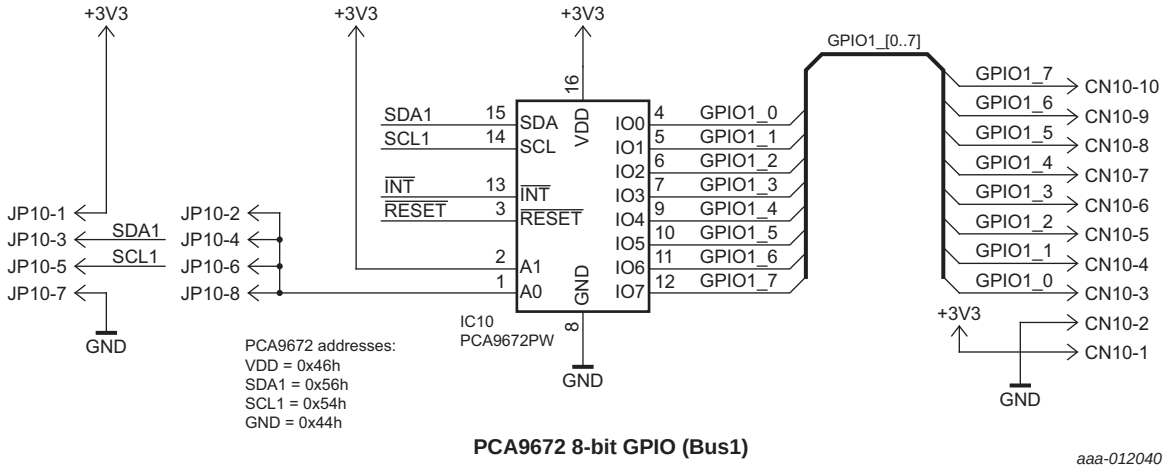


**Fig 24. Bus1 GPIO 8-bit**

**Table 5. LED driver address selection**

| A0 connected to | Hexadecimal 8-bit address | | | NXP 7-bit address | | |
|---|---|---|---|---|---|---|
| | Address | MSB | LSB | Address | MSB | LSB |
| GND | 0x44 | 0100 | 0100 | 0x22 | 010 | 0010 |
| $V_{CC}$ | 0x46 | 0100 | 0110 | 0x23 | 010 | 0011 |
| SCL | 0x54 | 0101 | 0100 | 0x2A | 010 | 1010 |
| SDA | 0x56 | 0101 | 0110 | 0x2B | 010 | 1011 |


**Fig 25. Bus1 GPIO 8-bit section**


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## 5.4 Bus two (Bus2)

The second I²C bus on the Fm+ Development Board (OM13260) requires the addition of an NXP LPC Xpresso Module (not included in the kit) to either be the Master, or drive the bus controller (PCA9665, IC4).

There are two almost identical I²C buses on the Fm+ Development Board (OM13260), called Bus1 and Bus2. These share a ground and power connection, but may be operated independently.

**Remark:** The bus voltage for each I²C maybe different (for example 3.3 V for one I²C bus, 5 V for the other I²C bus).

### 5.4.1 Bus2 master (LPC Xpresso — MCU LPC1343)

The LPC Xpresso Module contains an NXP LPC1343 MCU (similar to the one on Bus 1) and support circuits called LPC-Link. See Figure 26. The LPC Xpresso requires firmware that is loaded through either the LPC-Link and USB Bridge, or JTAG Single Wire Debug (SWD) connector.

**Remark:** The LPC Xpresso is not compatible with the NXP GUI, and requires the installation of an IDE for code development.

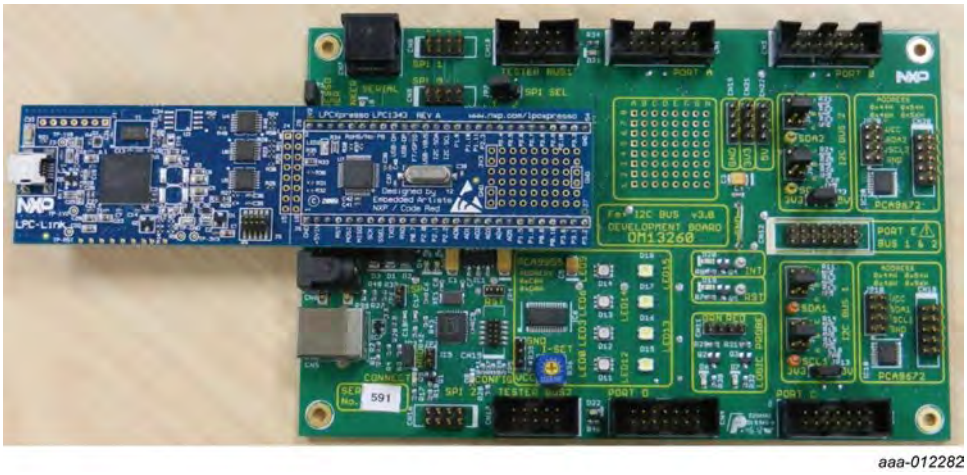


**Fig 26. Fm+ development board with LPC Xpresso installed**

The LPC-Link may be powered from the Fm+ Development Board (OM13260), or from a USB Host (connected to the LPC-Link port). There is a possible conflict that the LCP-Link 3.3 V supply will compete with the Fm+ Development Board (OM13260) 3.3 V supply. To avoid this issue the LPC Xpresso Module can provide its own 3.3 V power by removing jumper JP1 on the Fm+ Development Board (OM13260). See Figure 27.

I²C Bus2 is connected to the MCU Port0 via RC edge rate control networks that provide bus fall time control (SCL2: R45 and C23; SDA1: R44 and C19). See Figure 28.


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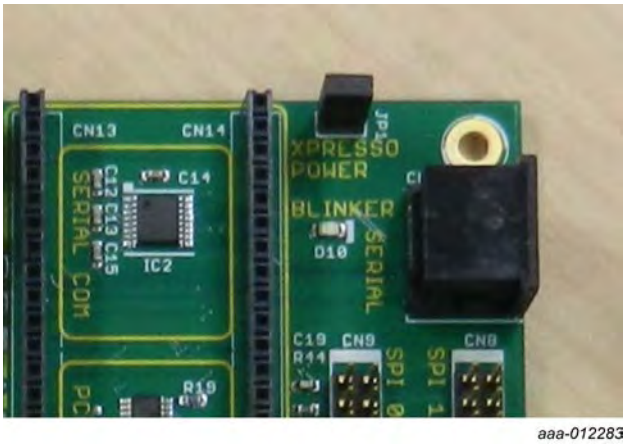


**Fig 27. LPC Xpresso power (JP1)**

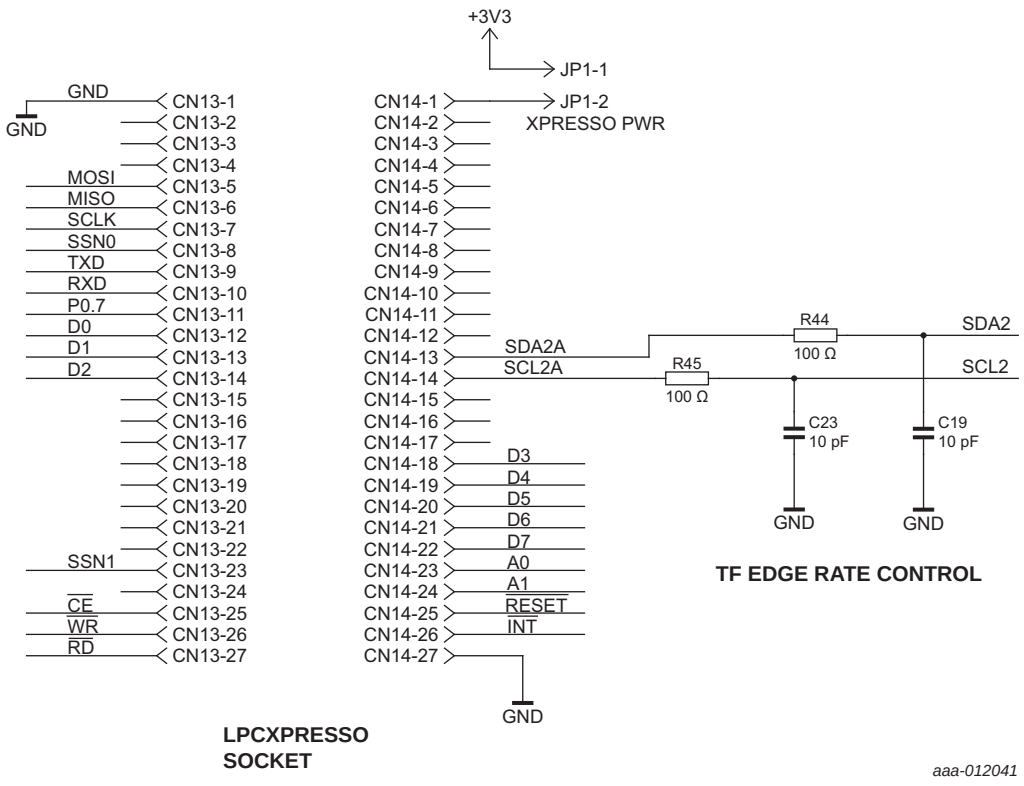


**Fig 28. Bus2 master (LPC Xpresso)**


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### 5.4.2 Bus2 bus master (PCA9665)

A second Bus Master is connected to Bus2 using a dedicated Bus Controller device (PCA9665 Fm+ parallel bus to I²C-bus controller) (IC4). The parallel port side is connected to the LPC Xpresso module (LPC1343 PIO2 and PIO3). The I²C side is connected via RC edge rate control networks that provide bus fall time control (SCL2: R47 and C21; SDA2: R46 and C22). See Figure 29 and Figure 30. Note IC4 is physically underneath the LPC Xpresso module.

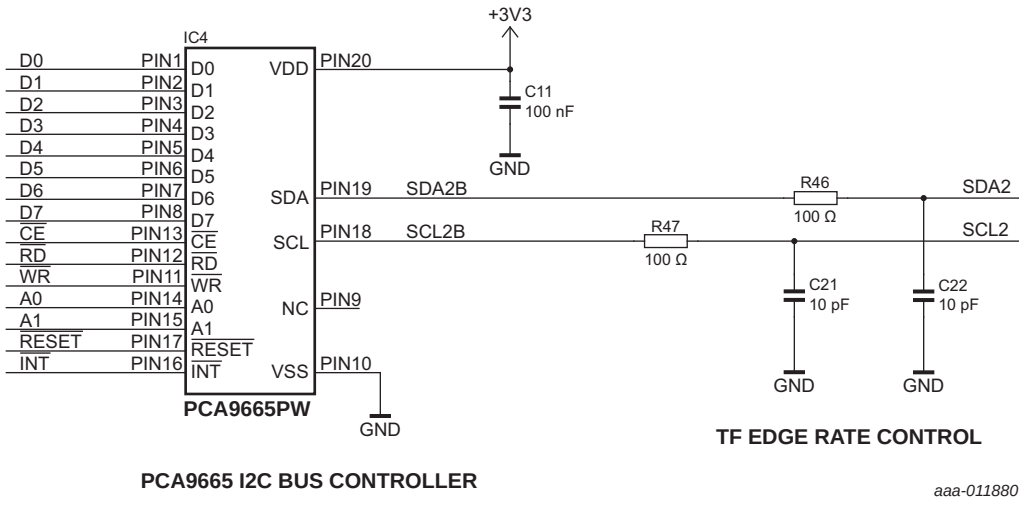


**Fig 29. Bus2 master (PCA9665)**


**Fig 30. Bus2 master (PCA9665) section**


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### 5.4.3 Bus2 pull-up resistors

The Bus2 is pulled up to either the 3.3 V or 5 V supplies, via JP23. Three different value pull-up resistors are provided by jumper selection, JP21 and JP22. The values of the pull-up resistors are shown in Table 6. Separate pull-ups are provided for the SCL and SDA signal lines. See Figure 31 and Figure 32. Bus1 has a similar arrangement (see Section 5.3.2).

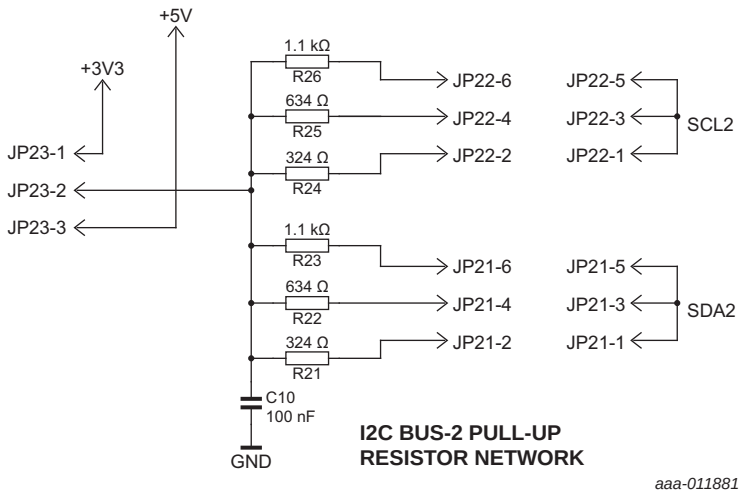


**Fig 31. Bus2 pull-ups and bus voltage selector**

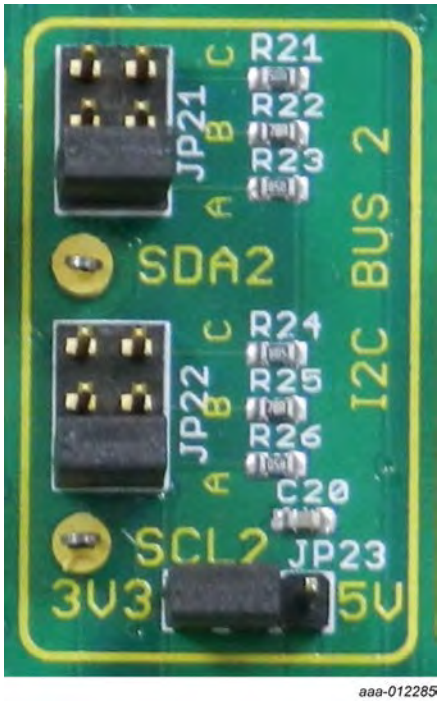


**Fig 32. Bus2 pull-ups section**


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**Table 6. Bus pull-up resistors**

| Strength | Position | Value | Bus1 SCL | Bus1 SDA | Bus2 SCL | Bus2 SDA |
|---|---|---|---|---|---|---|
| LOW | A | 1.1 kΩ | R16 | R13 | R26 | R23 |
| MID | B | 634 Ω | R15 | R12 | R25 | R22 |
| HIGH | C | 324 Ω | R14 | R11 | R24 | R21 |

## 5.5 Daughter card ports

Accessory circuit cards called Daughter Cards may be attached to any ports (Port A – Port D), connectors CN1 – CN4 respectively, see Figure 34. Each port carries the same signals, regardless of physical location. Daughter Cards have jumpers to select whether connection to Bus1 or Bus2 is required. Port A is shown in Figure 33; Port B – Port D are identical, and effectively in parallel.

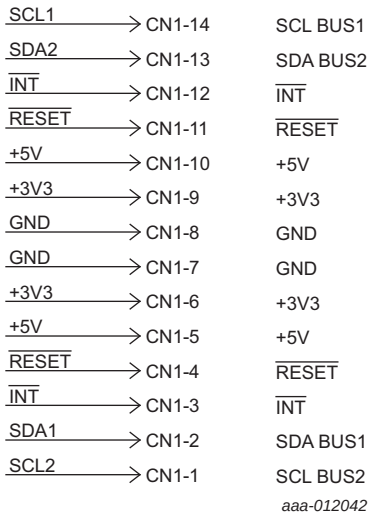


**Fig 33. Port A**

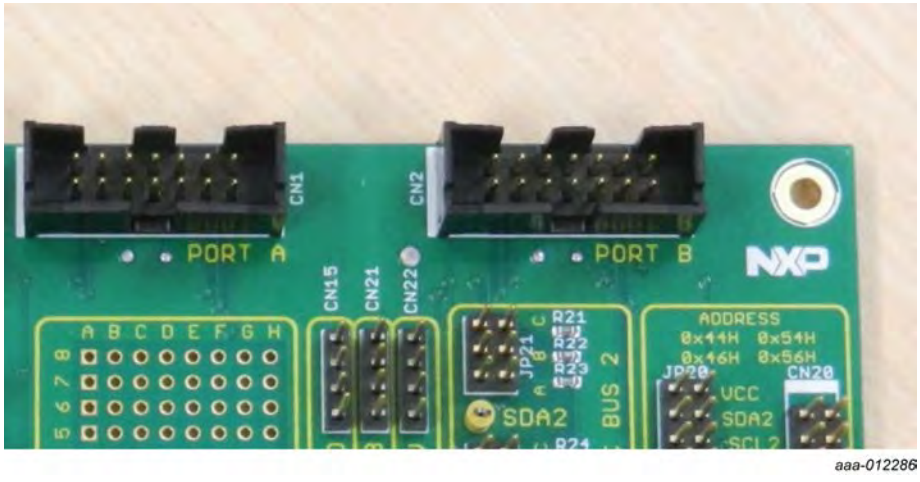


**Fig 34. Daughter card connectors (Port A and Port B shown)**


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## 5.6 Port E

The two independent $I^2C$ Buses (Bus1 and Bus2) can be joined electrically to create a single $I^2C$-bus. The link may be made by wire jumper or by an add-on board with an $I^2C$ Bus Buffer device installed. The PCA9617A Bus Buffer Demo Board (OM13398) (supplied in the kit) is an example. The Fm+ Development Board (OM13260) may also be operated with nothing connected to Port E (CN12).

The Port E signal pins are arranged to be symmetrical, permitting the card to be rotated 180°, effectively changing the direction of the signals through the card. See Figure 35 and Figure 36.

**Remark:** When linked together by wire jumper, the pull-up resistors on each bus are effectively in parallel. The resulting value is therefore one-half of the original value. Pull-up resistors of low value will overload the $I^2C$ drivers, and effectively stop the bus from operating.

### 5.6.1 Linking both buses together (with a jumper)

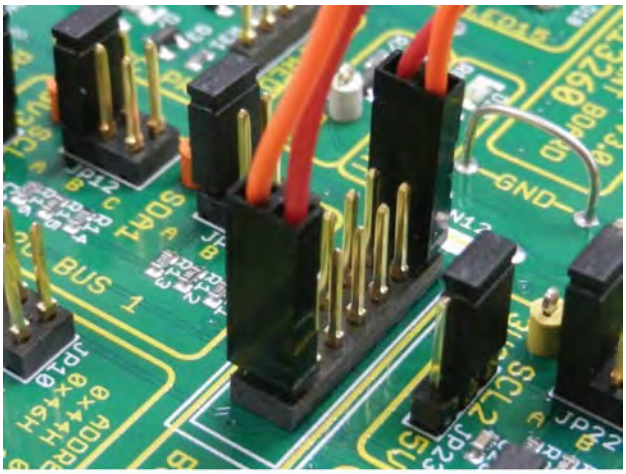


**Fig 35. Port E with wire jumper**


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### 5.6.2 Linking both buses together (with a bus buffer board)

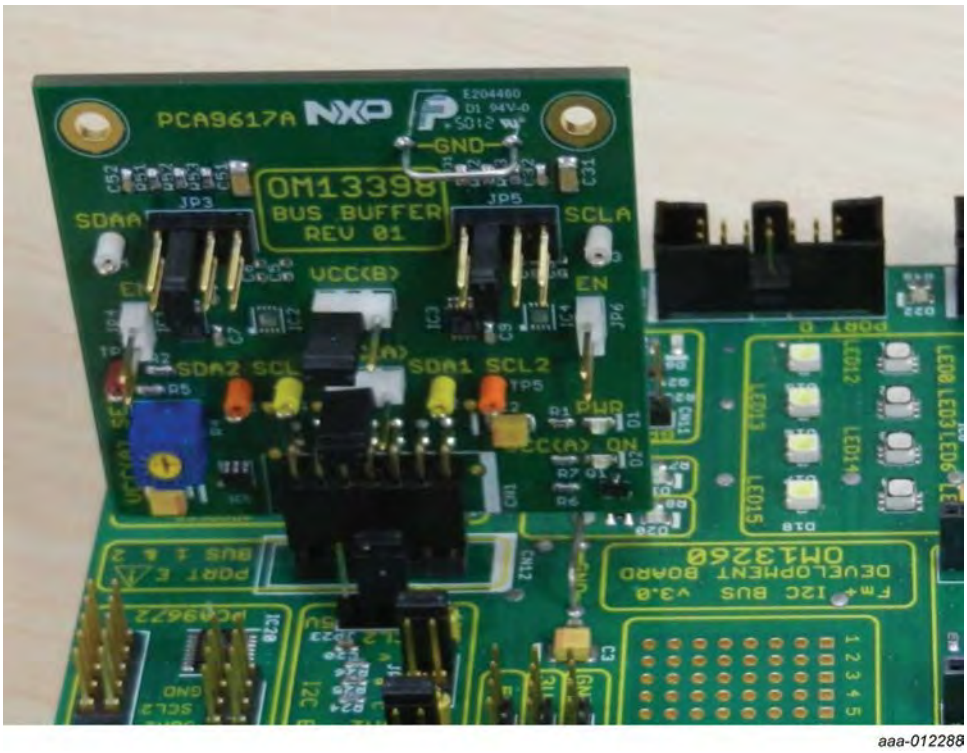


**Fig 36. Port E with bus buffer card (OM13398) installed**

## 5.7 Tester connectors (for third-party tools)

Bus1 may be connected to third-party test equipment via CN17. Bus2 has a similar and independent connection at CN18. See Figure 37, Figure 38 and Figure 39.

**Remark:** Refer to Section 9 “Third-party tools” of this user manual.

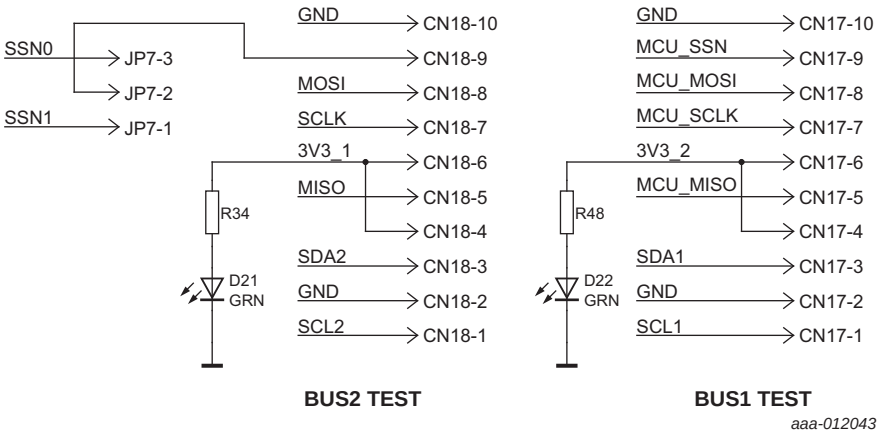


**Fig 37. Bus1 and Bus2 tester connectors**


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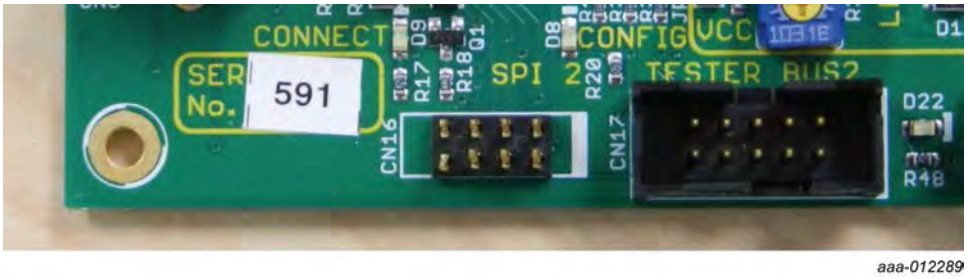


**Fig 38. Bus1 tester connectors**

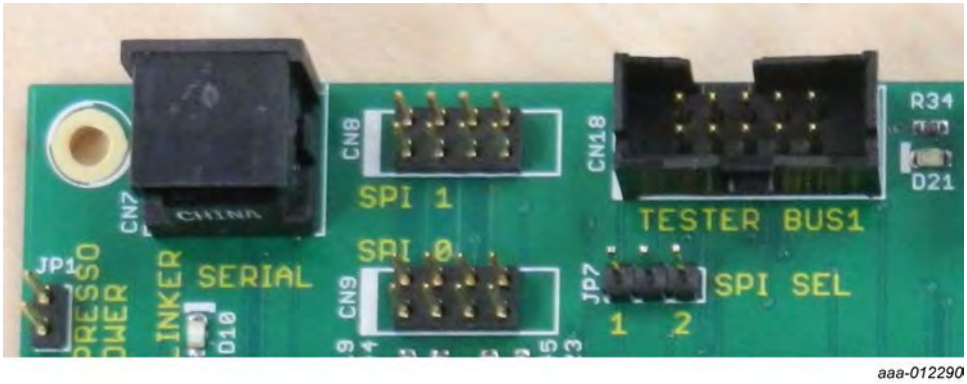


**Fig 39. Bus2 tester connectors**

## 5.8 Serial communication port

The LCP Xpresso module has a serial comms (communications) port, EIA232 standards compliant using IC2, a voltage level translator. See Figure 40. This is provided for connection to $I^2C$ Bridge devices that require Serial Communications.

To save space on the PCB, a small mini-DIN connector (CN7) replaces the standard 9-pin DE shell connector. For connection to standard serial comms cables an adapter is required, see Figure 41. The recommended Mini-DIN to DE-9 Adapter is Digikey PN: AE1393-ND (not supplied) See Figure 42.


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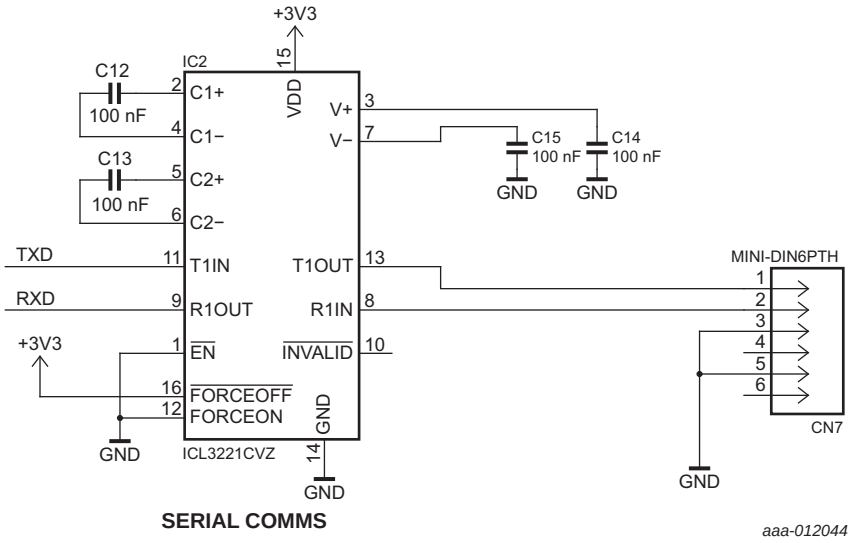


**Fig 40. Bus2 tester connectors**

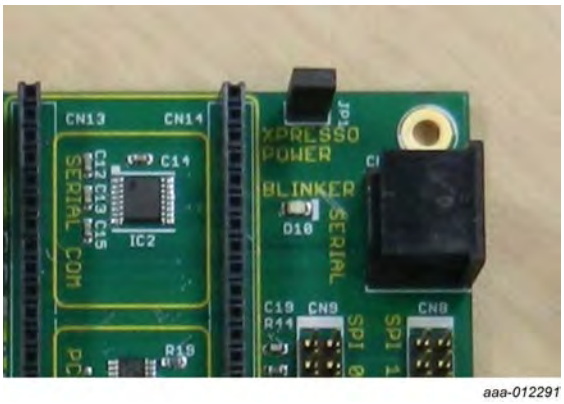


**Fig 41. Serial Com section**


**Fig 42. Serial Com dongle**


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## 5.9 SPI ports

Both the Bus1 Master MCU and the Bus2 Master LPC Xpresso Module support SPI communications. The Bus1 MCU has one SPI port (SPI2) (CN16) and the LPC Xpresso has two SPI ports (SPI0 and SPI1) (CN9 and CN8, respectively). See Figure 43, Figure 44 and Figure 45. Also refer to Section 9 of this user manual for details on using the tester connector (for third-party tools) with the SPI ports.

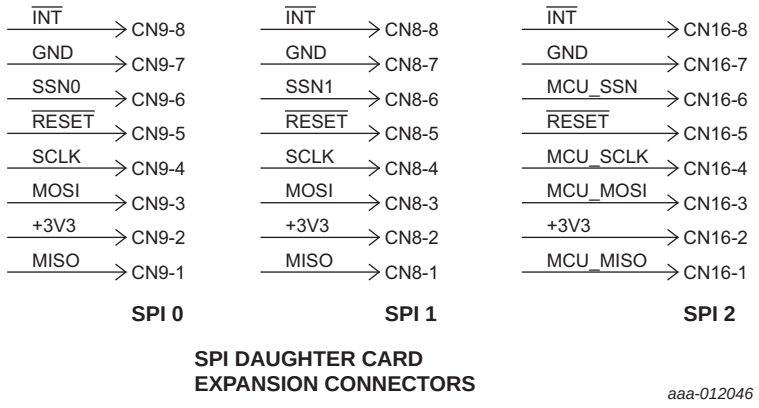


**Fig 43. SPI connectors**


**Fig 44. SPI 2 (Bus1 MCU) connector**

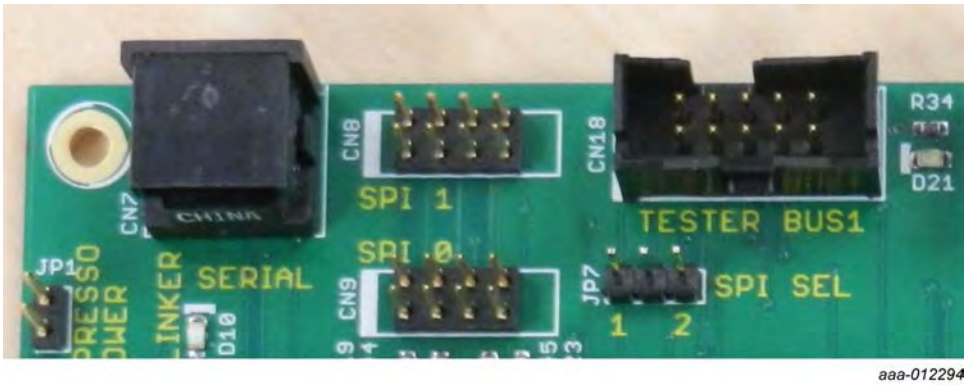


**Fig 45. SPI 0 and SPI 1 (Bus2 LPC Xpresso) connectors**


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## 5.10 Logic probe

Most of the I²C-bus slaves produce logic signals on their input/output ports. It is necessary to know a logic state. To facilitate this test there are two LEDs with buffers that may be used as a simple ‘logic probe’.

To prevent circuit loading the LEDs are buffered by FETs as shown in Figure 46. Green LED (D6) is driven by FET (Q2) when CN11-1 is at or near ground. When CN11-1 is open (or logic 1) the FET is non-conducting, and the LED is off. Red LED (D7) is driven by FET (Q3) when CN11-4 is at or near ground. When CN11-4 is open (or logic 1) the FET is non-conducting, and the LED is off. See Figure 47.

Note that the threshold voltage ($V_{th}$) of the FET is 2.5 V to 4.5 V to ensure it operates correctly on both 3.3 V and 5 V logic levels. The FET source is tied to 5 V, and the gate must therefore be at 2.5 V or lower relative to ground, to turn on the FET and light the LED.

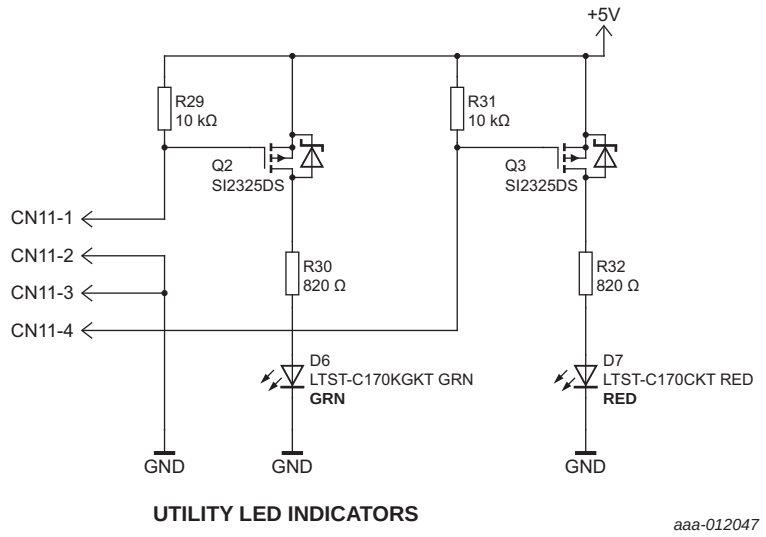


**Fig 46. Logic probe circuit**


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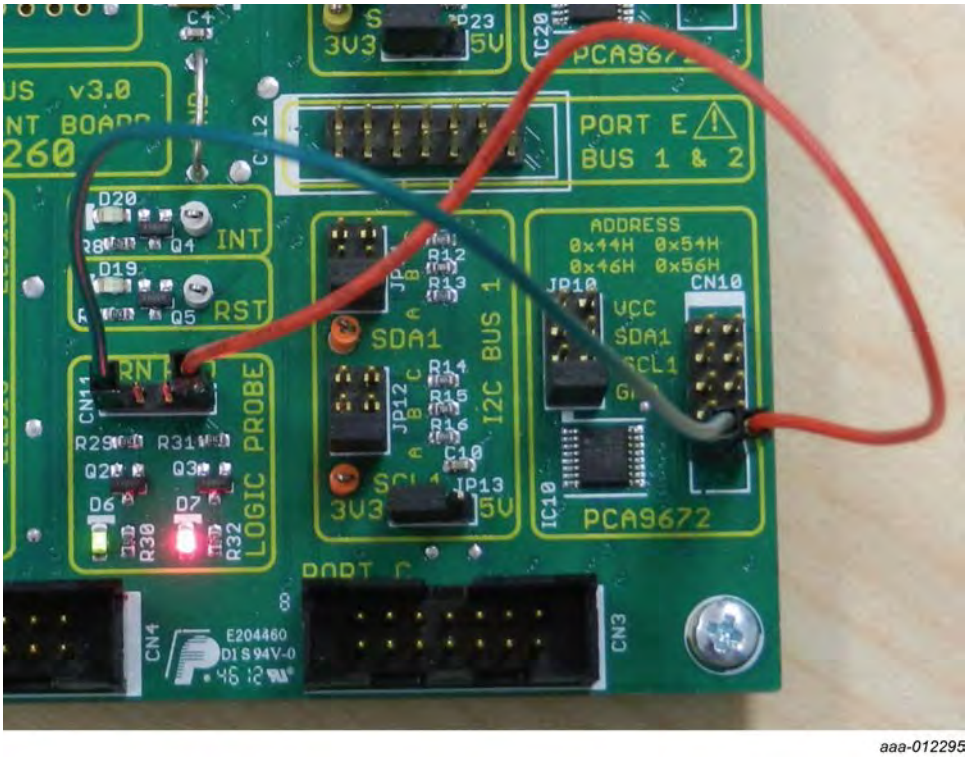


**Fig 47. Logic probe section (shown monitoring two GPIO channels from Bus1)**

## 5.11 INT and RST indicators

Two global digital signal nets, called INT (interrupt) and RST (reset), connect all I²C-bus devices on the board and also the Port A – Port E daughter card connectors. These are also connected to the Master (MCU, IC5) on Bus1, the Master (Bus Controller, IC4), and the LPC Xpresso module. See Figure 48 and Figure 49.

Additional buffered LEDs are provided (D19, RST and D20, Interrupt) on the Fm+ Development Board (OM13260) for visual indication. These buffered LEDs operate in the same fashion as the logic probe (see Section 5.10 “Logic probe”).

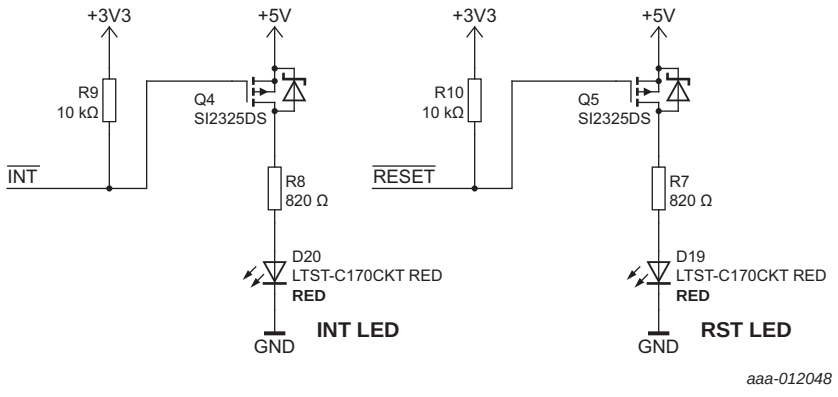


**Fig 48. INT and RST indicators circuit**


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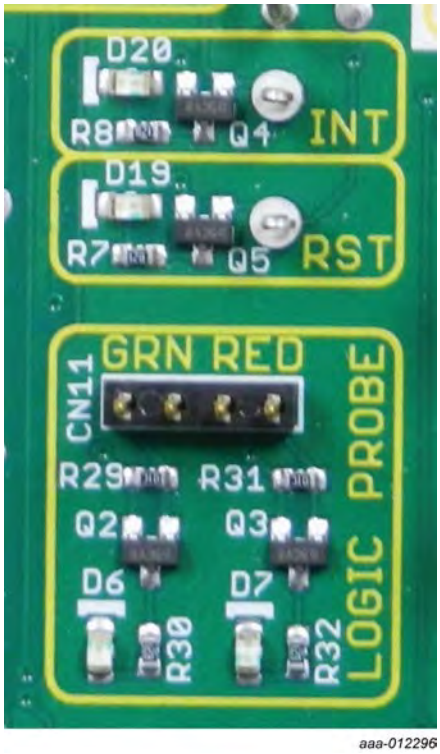


**Fig 49. INT and RST indicators section**

## 5.12 Prototype area

Additional circuits may be required to for an application beyond the intended scope of the Fm+ Development Board (OM13260). For example, using different value pull-up resistors than those supplied, or other circuit experiments.

The prototype area is available, and consists of pads and holes on a 100 mil (2.54 mm) grid. Power for these components is made available at several connector points (CN15 is ground, CN21 is +3.3 V, and CN22 is +5 V). See Figure 50 and Figure 51.


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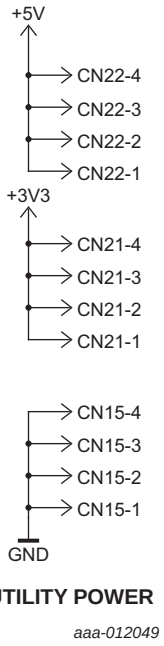


**Fig 50. Prototype area circuit**

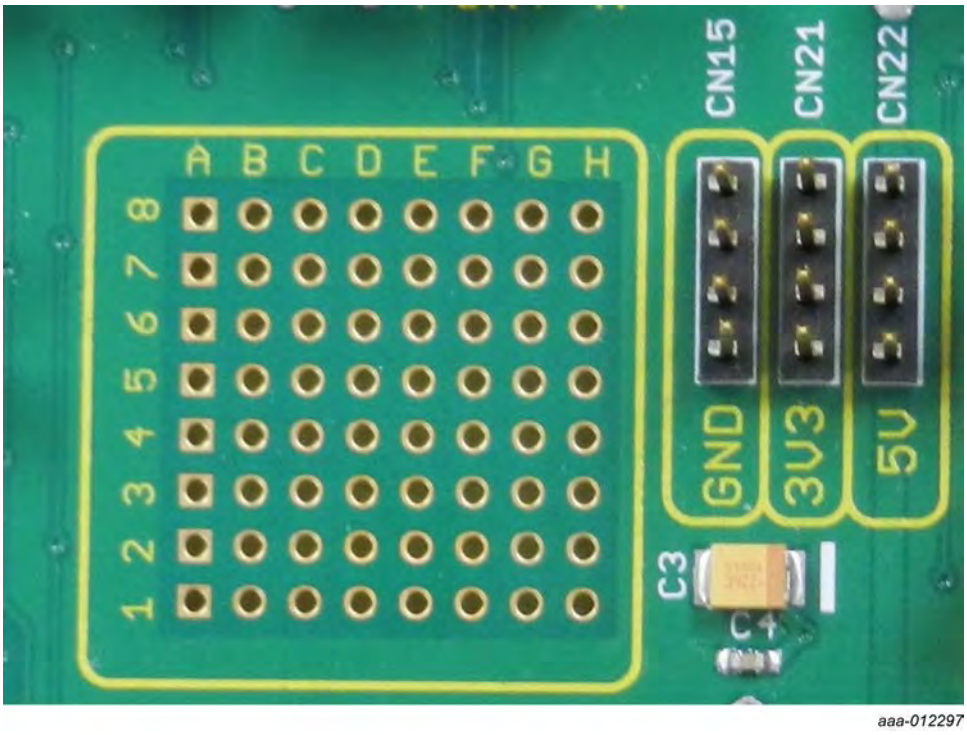


**Fig 51. Prototype area section**


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## 5.13 LED blinker (PCA9901)

On the Fm+ Development Board (OM13260) V3.0 there is an LED Blinker device (PCA9901, IC3) and LED indicator (D10). While not strictly an I²C-bus device, as it uses a one-wire protocol, it belongs to the NXP I²C-bus product portfolio.

**Remark:** The PCA9901 will be made obsolete, and will not be present on future versions of the Fm+ Development Board (OM13260).

Refer to the PCA9901 data sheet for details of this device. Note that it is not connected to either I²C Bus on the Fm+ Development Board (OM13260). It is connected to the LPC Xpresso module (PIO_0.7), and that module must be present (and programmed) to drive the PCA9901 device. See Figure 52 and Figure 53.

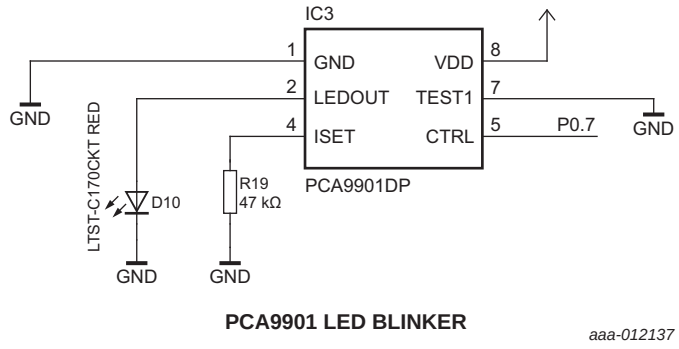


**Fig 52. LED blinker (PCA9901)**

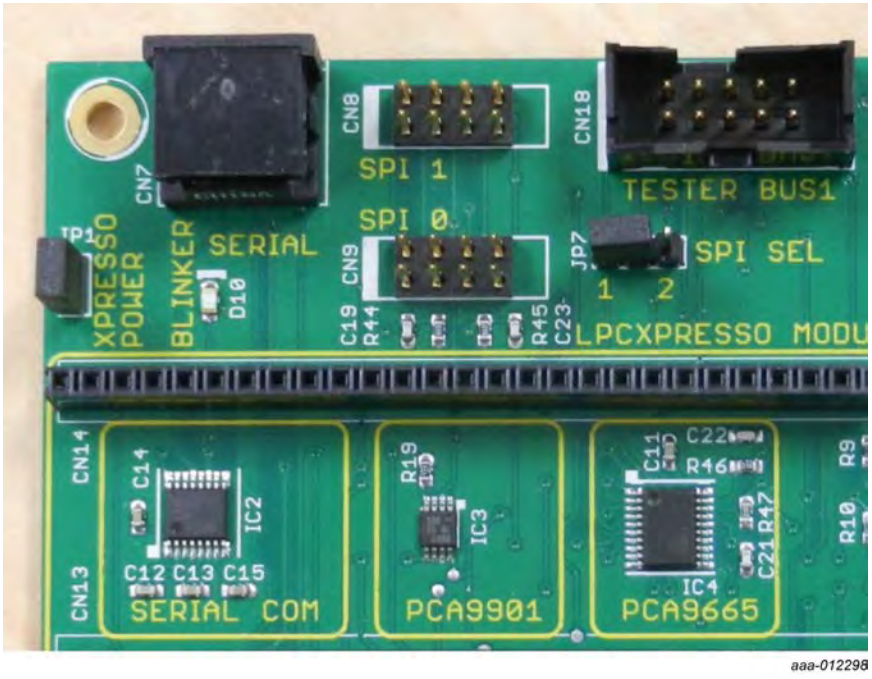


**Fig 53. LED blinker (PCA9901) section**


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# 6. GPIO target board (OM13303)

The GPIO Target Board (OM13303) is used to monitor the Input/Output (I/O) signals from a GPIO. The board has eight channels, each with a push switch and an LED indicator. See Figure 54.

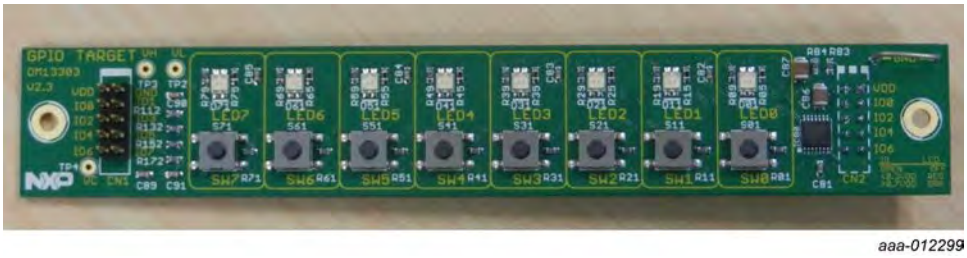


**Fig 54. OM13303 GPIO target board PCB assembly (front side)**

## 6.1 Theory of operation

Each of the eight channels operates independently and in the same way. The voltage applied to the input pin is compared in a Windows comparator, which in turn drives a dual color LED. The thresholds for the comparators are set to one-third (logic zero) and two-thirds (logic one) of the supply voltage. These values correspond to the $I^2C$-bus logic threshold voltages for the $I^2C$-bus specification.

When a push button is pressed, a logic zero is applied the channel, which can be read by the GPIO device to which the GPIO Target Board is attached. A $2 \times 5$ header is used to connect to the Fm+ Development Board (OM13260) or a GPIO daughter card with a flat ribbon cable (supplied in the kit).

Two connectors are installed, one on each end of the board, and on opposite sides of the PCB to aid in connection without the cables blocking the buttons or LEDs.

There are no option jumpers and no adjustments on the GPIO Target Board (OM13303).

Unlike other PCB assemblies in the Fm+ Development Kit (OM13320), the GPIO Target Board (OM13303) has components on both sides of the PCB. See Figure 55.

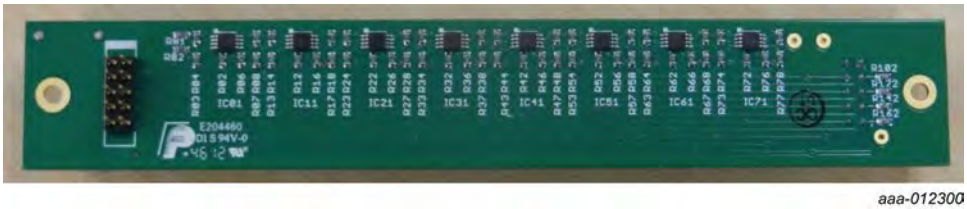


**Fig 55. OM13303 GPIO target board PCB assembly (back side)**


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## 6.2 Circuit description

The schematic diagram has multiple sheets. For clarification, only fragments of the schematic are shown here. The full schematic should be downloaded if required. The following pages are divided in to several sections covering the window comparator, push switches, bias circuit, and connectors.

### 6.2.1 Window comparator

Channel 0 is shown; channels 1 through 7 are identical. The input signal is applied to two comparators, (IC01A and IC01B).

If the input (IO0) is higher than the threshold set by $V_{IH}$ and resistor divider (R03 and R04), the output of the comparator (IC01A) switches to near ground. This turns on the green LED (D01). Resistor (R04) applies positive feedback hysteresis (about 150 mV) to the comparator, shifting the trip point to a slightly lower voltage, to stop the circuit from oscillation around the switch point.

The input (IO0) is attenuated slightly by a resistor divider (R07 and R08), if the resulting voltage is lower than the threshold set by $V_{IL}$, the output of the comparator (IC1B) switches to near ground. This turns on the red LED (D01). Resistor (R08) applies positive feedback hysteresis (about 125 mV) to the comparator, shifting the trip point to a slightly higher voltage, to stop the circuit from oscillation around the switch point.

LED current is limited by resistors R05 and R09, which are selected to give approximately equal brightness to the green and red LED elements. See Figure 56.

The operation of the window circuit is shown by applying a ramp waveform, see Figure 57 and Figure 58.

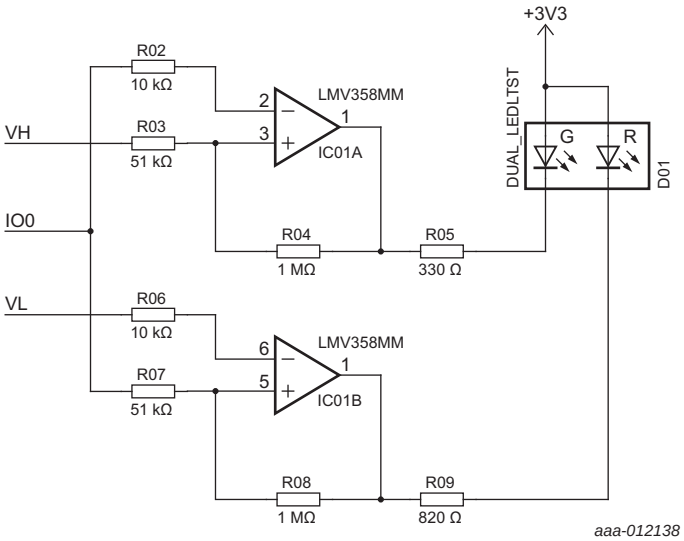


**Fig 56. Window comparator (Channel 0 shown)**


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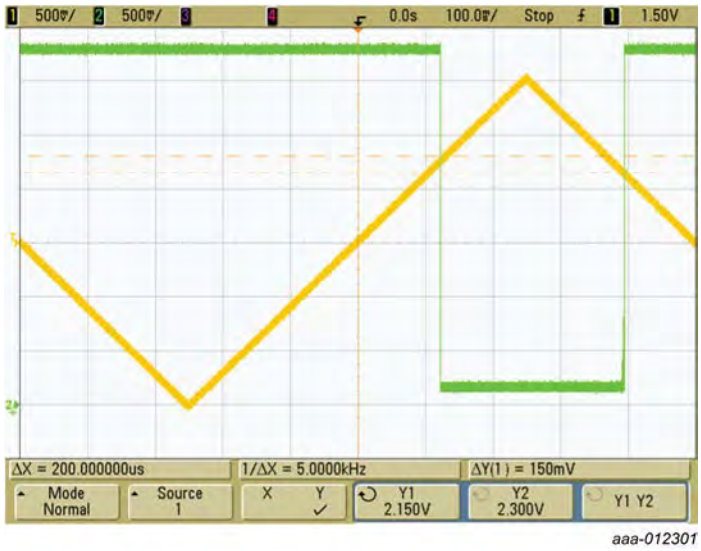


**Fig 57. Input ramp (yellow trace), green LED drive (green trace)**

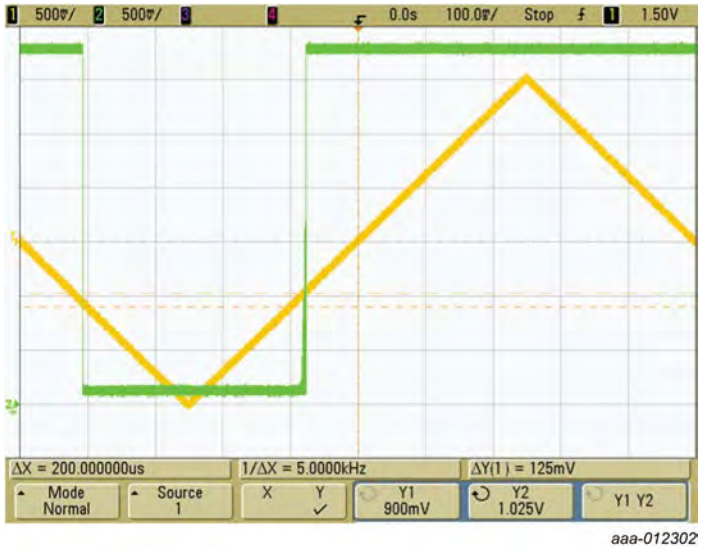


**Fig 58. Input ramp (yellow trace), red LED drive (green trace)**


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### 6.2.2 Push switches

Each channel has a push switch (S01 through S71) that connects the appropriate IO pin to ground when pressed. Series resistors (R01 through R71) limit the current, in the event that the IO pin is being driven HIGH (by the connected GPIO device) when the push switch is closed. Each input is biased to VC (one-half the supply voltage), in the event that the IO pin is left open. This extinguishes both the green and red LEDs of that channel, preventing false readings. See Figure 59.

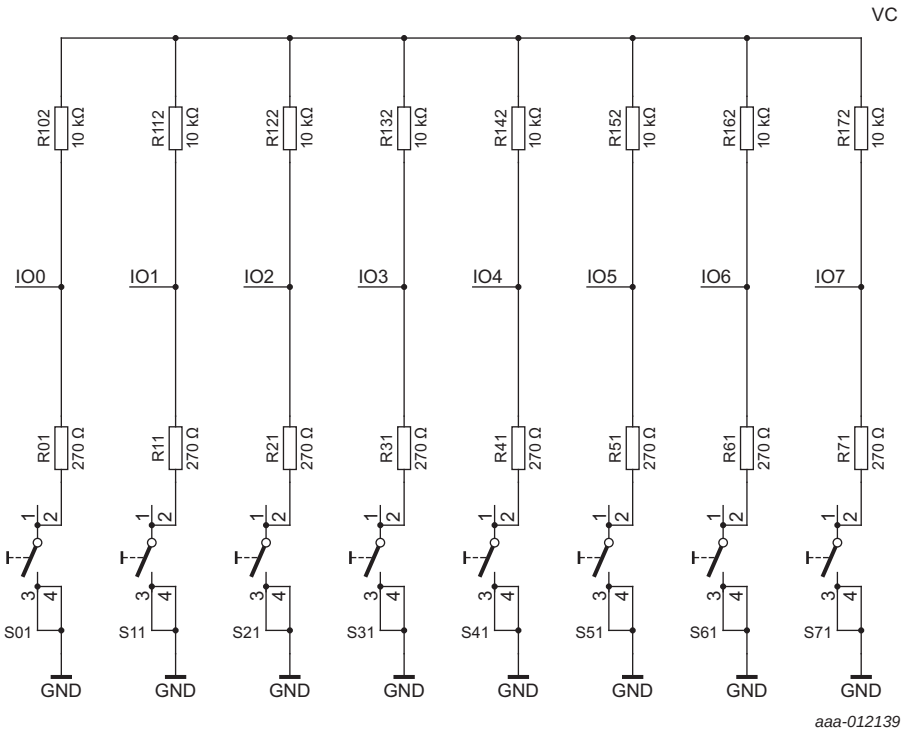


**Fig 59. Push switches**

### 6.2.3 Bias circuit

Each channel requires three reference voltages (VL, VC, and VH), from the bias circuit. A resistor divider chain (R01, R02, R03, and R04) divides the supply voltage to produce one-third (VL), one half (VC) and two-thirds (VH). Each value is buffered by an op amp (sections of IC80). Test points are provided as PCB pads for VH (high), VC (center), and VL (low). The fourth section of the quad op amp (IC80) is not used. Noise spikes on each bias supply are removed by capacitors (C89, C90, and C91), power supply variations are removed by capacitors (C86 and C87). See Figure 60.


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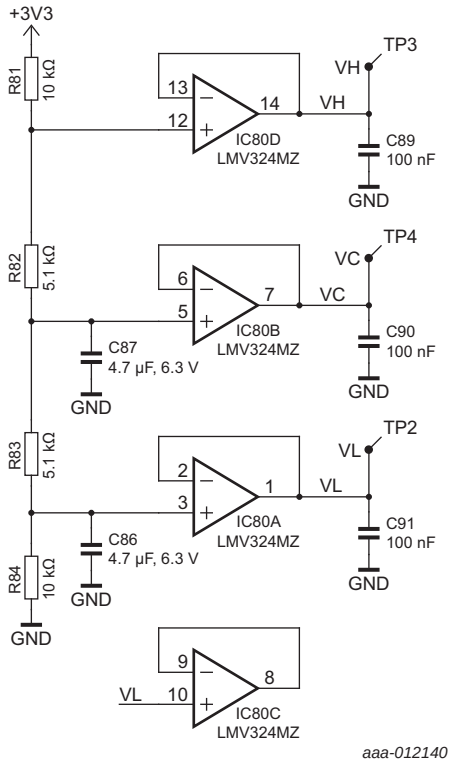


**Fig 60. Bias circuit**

### 6.2.4 Connectors

The GPIO Target Board (OM13303) is intended to be connected to the Fm+ Development Board (OM13260) (or other GPIO daughter cards) via a 10-pin ribbon cable. There are two identical connectors, one on each end of the GPIO Target Board to allow connection without blocking the push switches or the LEDs. See Figure 61, Figure 62 and Figure 63.

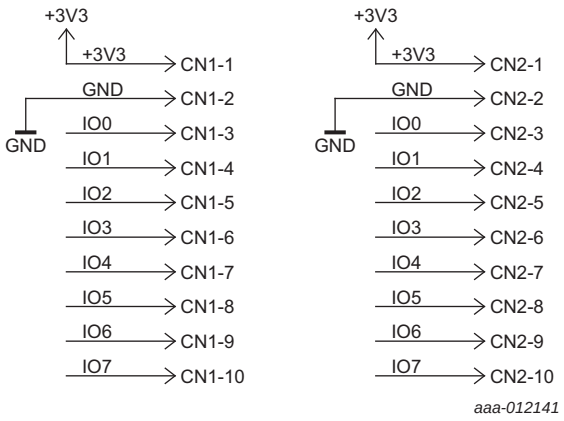


**Fig 61. Connectors**


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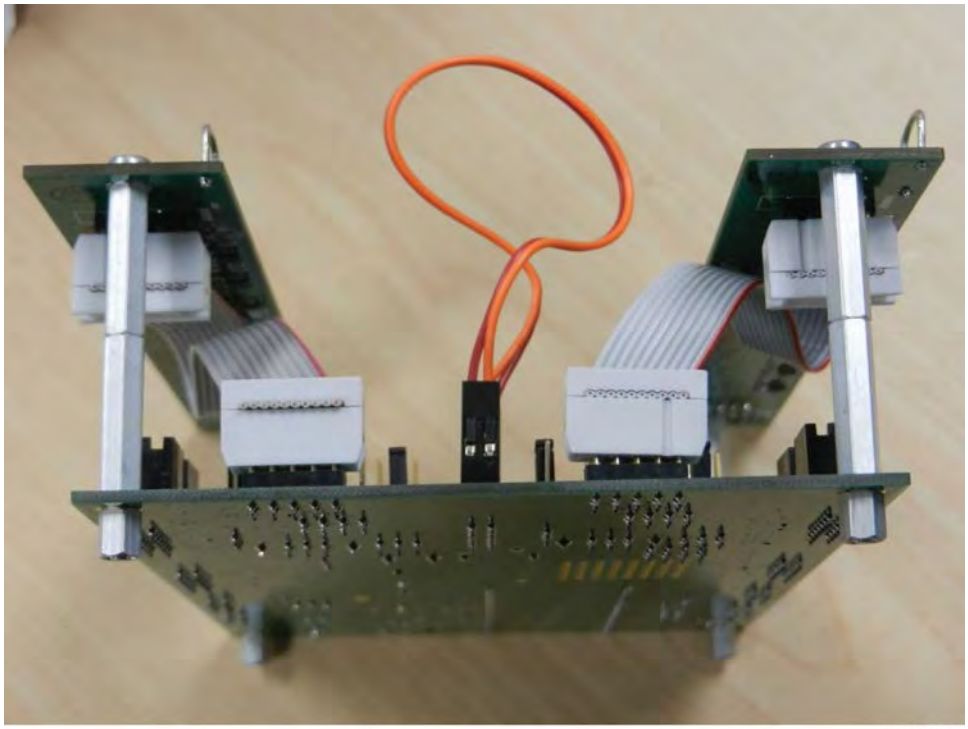
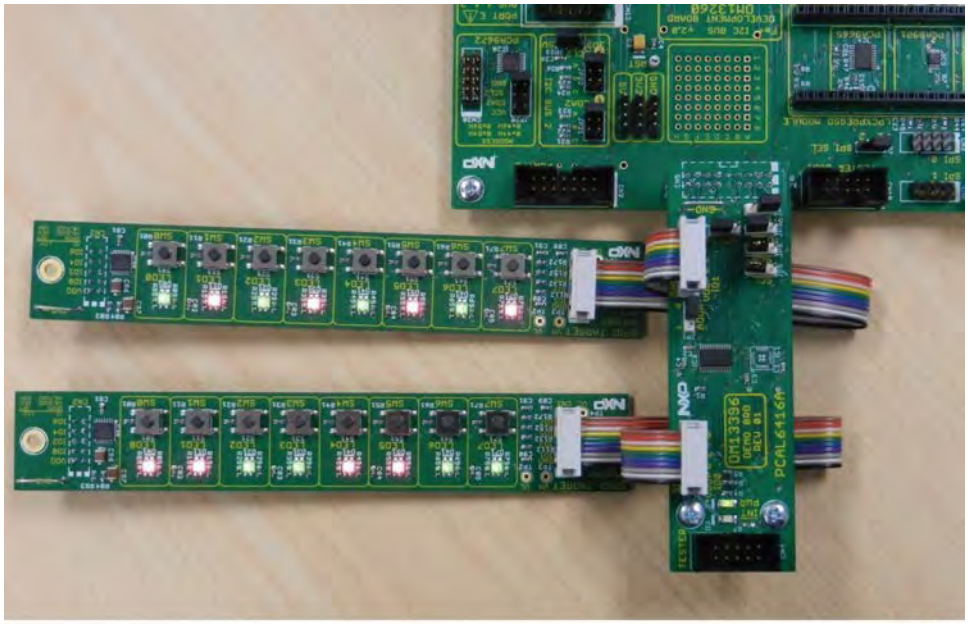


aaa-012303

**Fig 62. Ribbon cables attached to underside of the GPIO target board (OM13303)**



aaa-012304

**Fig 63. Ribbon cables attached to the topside of the GPIO target board (OM13303)**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# 7. Bus buffer demo board (OM13398)

The Bus Buffer Board (OM13398) (supplied in the kit) provides a method to link both the $I^2C$ buses on the Fm+ Development Board (OM13260) by attachment to Port E, in place of the wire jumper used earlier (see Section 5.6.1 “Linking both buses together (with a jumper)”. See Figure 64 and Figure 65.


**Fig 64. Bus buffer board (OM13398)**

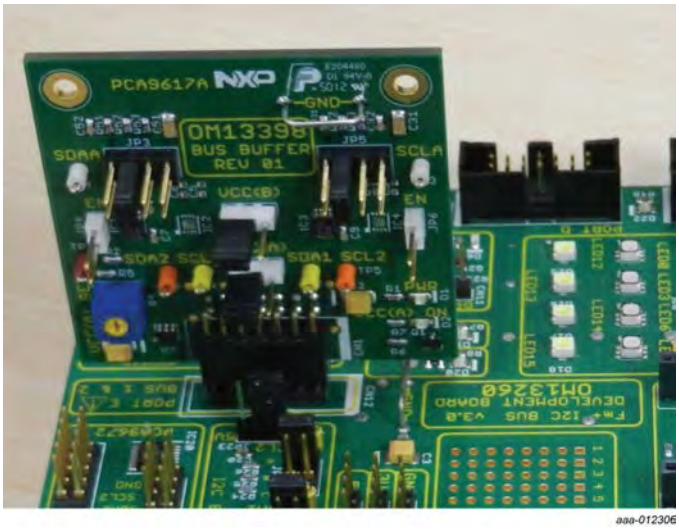


**Fig 65. Bus buffer board (OM13398) attached to the Fm+ development board (OM13260)**


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## 7.1 Theory of operation

Two identical bus buffer devices are connected in series between the Bus1 and Bus2 segments on the Fm+ Development Board (OM13260). Each Bus Buffer has two identical channels, one for $I^2C$ clock (SCL) and the second for $I^2C$ data (SDA). Only one channel will be described in detail.

Each PCA9617A bus buffer device has two power supply connections, $V_{CC(A)}$ and $V_{CC(B)}$, to allow voltage level shifting between one $I^2C$-bus segment and another $I^2C$-bus segment. Jumpers on the Bus Buffer Board (OM13398) select the voltage source of each of the two device power supplies. To demonstrate the voltage level translator ability the link between the two bus buffers is supplied from a variable voltage regulator, which in turn can be set by the user anywhere between 1.0 V and 3.2 V.

The pull-up resistor on the Low Voltage Bus section is selected by jumpers.

## 7.2 Circuit description

The schematic diagram has multiple sheets. For clarification, only fragments of the schematic are shown here. The full schematic should be downloaded if required. The following pages are divided in to several sections covering the Bus1 Bus Buffer, Bus2 Bus Buffer, Supply select jumpers, Adjustable Voltage Regulator, and Connectors. A block diagram will assist understanding. See Figure 66.

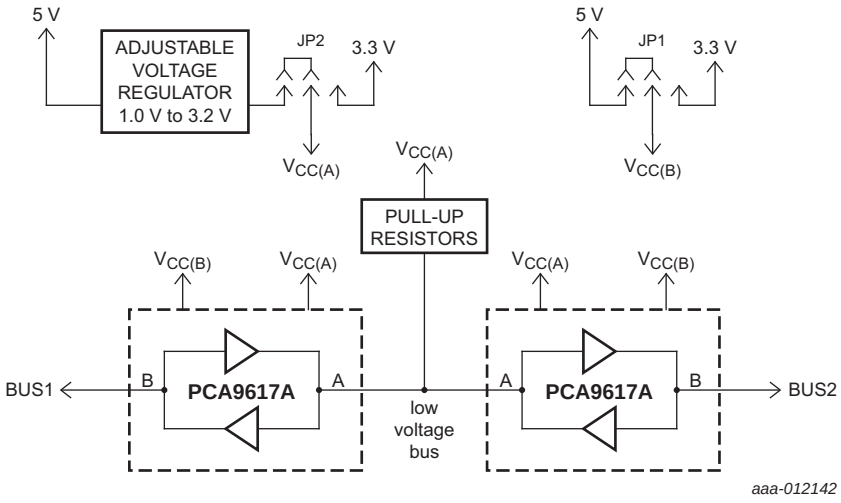


**Fig 66. Block diagram for the bus buffer board (OM13398)**


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### 7.2.1 Bus1 bus buffer (PCA9617A)

I²C-bus signals from the Fm+ Development Board (OM13260), called SCL1 and SDA1, are applied to the high voltage or 'B' Side of IC1 (PCA9617A). The required pull-up resistors on this section of Bus1 are on the Fm+ Development Board (OM13260).

Signals on the low voltage or 'A' Side of IC1 are connected to a selection of pull-up resistors selected by either JP5 (for SCL) or JP3 (for SDA), and the low voltage or 'A' Side of the second PCA9617A, IC3.

Loading capacitors, C31 for SCL and C51 SDA, can be placed on the low voltage section of the bus. To accommodate two different footprints IC1 (TSSOP8) and IC2 (HWSON8) are connected in parallel, but only one part is installed. Installing JP4 disables the Bus Buffer. See Figure 67.

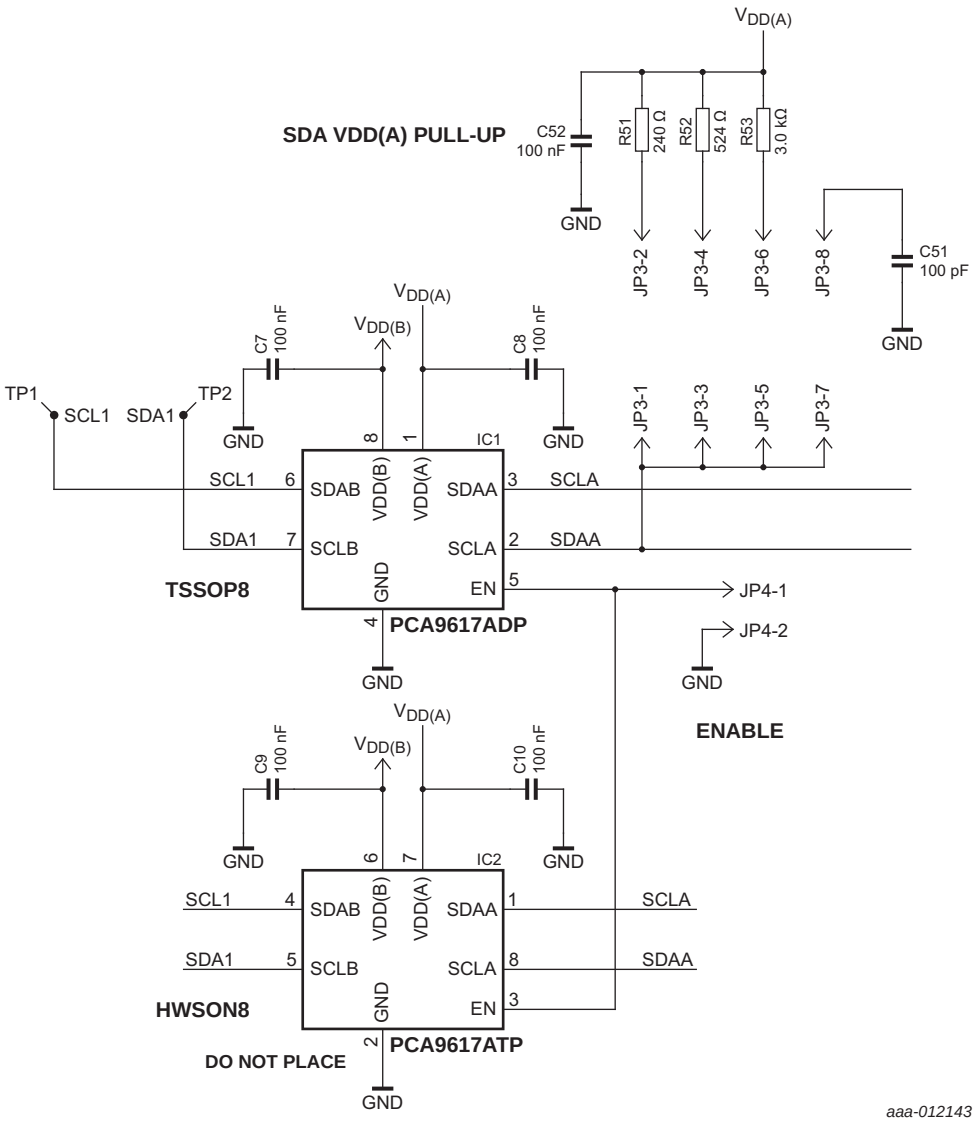


**Fig 67. Bus1 bus buffer**


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### 7.2.2 Bus2 bus buffer (PCA9617A)

I²C-bus signals on the low voltage bus are also connected to the A side of the second PCA9617A Bus Buffer device, IC3. To accommodate two different footprints, IC3 (TSSOP8) and IC4 (HWSON8) are connected in parallel, but only one device is installed. Installing JP6 disables the bus buffer. See Figure 68.

I²C-bus signals from the high voltage or 'B' side of IC3 (PCA9617A) are passed back to the Fm+ Development Board (OM13260). The required pull-up resistors on this section of Bus1 are on the Fm+ Development Board (OM13260).

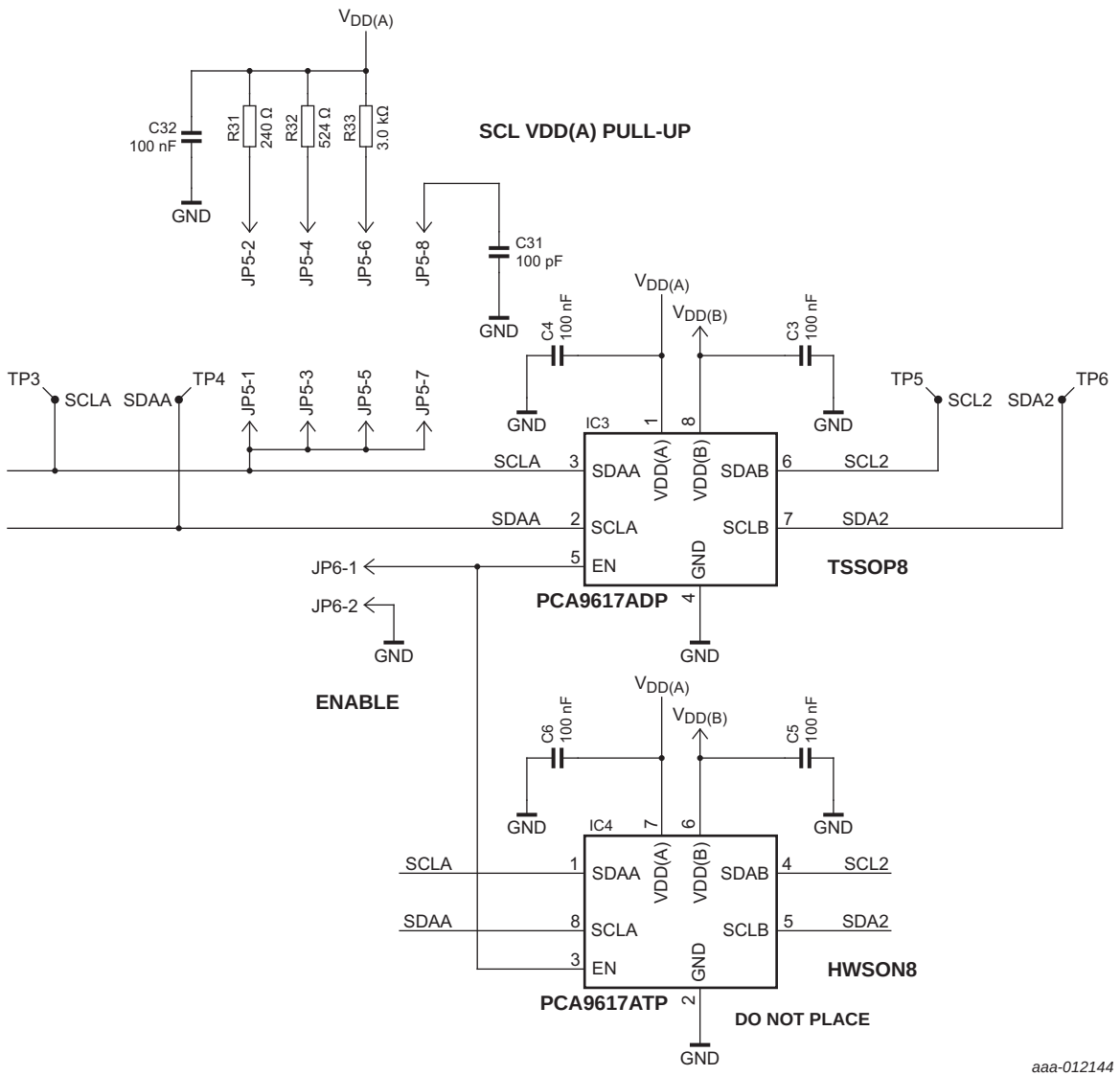


**Fig 68. Bus2 bus buffer**


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### 7.2.3 Supply select jumpers

The ‘B Side’ (high voltage side of the voltage level translator) of each PCA9617A can be either 3.3 V or 5 V as selected by JP1. The ‘A Side’ (low voltage side of the voltage level translator) of each PCA9617A can be either 3.3 V or a variable voltage between 1.0 V and 3.2 V as selected by JP2. See Figure 69.

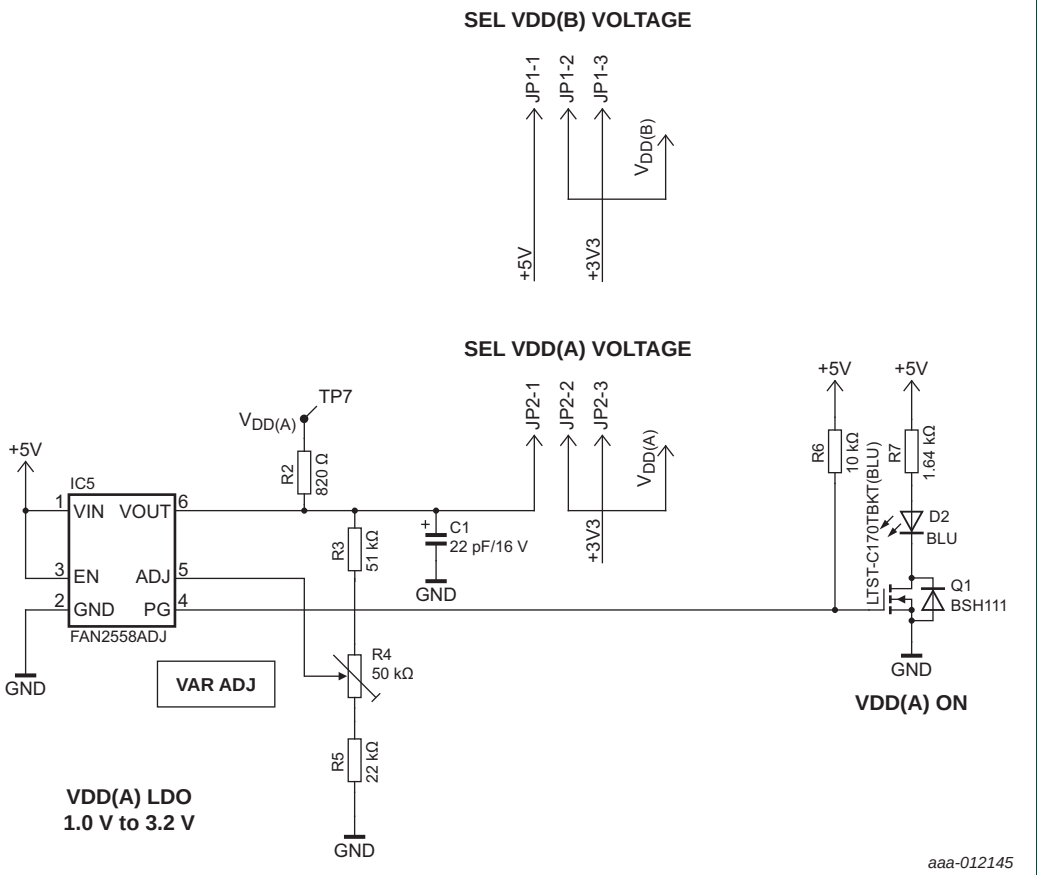


**Fig 69. Supply select jumpers**

### 7.2.4 Variable voltage regulator

The low voltage bus bias is generated by an LDO (Low Drop Out) voltage regulator, IC5. The output voltage is set by resistor divider R3, R4, and R5, and provides a range of 1.0 V to 3.2 V. The LDO provides a ‘Power Good’ signal, which is pulled HIGH by R6, and buffered by Q1. When the LDO is working correctly, the blue LED (D2) is turned ON. See Figure 69.


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### 7.2.5 Connector

The connector on the Bus Buffer Board (OM13398) matches the Port E connector on the Fm+ Development Board (OM13260). See Figure 70 and Figure 71.

The signals are arranged to be symmetrical so that the Bus Buffer Board (OM13398) can be rotated 180°, causing the signals from the Fm+ Development Board (OM13260) to flow in the opposite direction. For example, from Bus1 to Bus2, or from Bus2 to Bus1 when the Bus Buffer Board (OM13398) is rotated in the Port E connector. See Figure 71. The ability to reverse the signal flow is necessary when examining different $I^2C$ buffers, or comparing one NXP device to a non-NXP device.

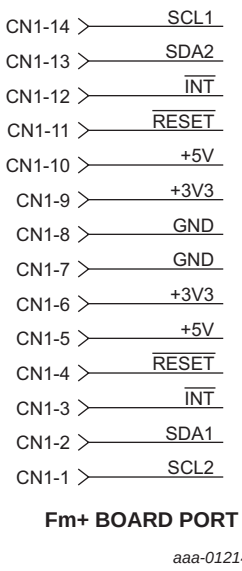


**Fig 70. Bus buffer board connector**

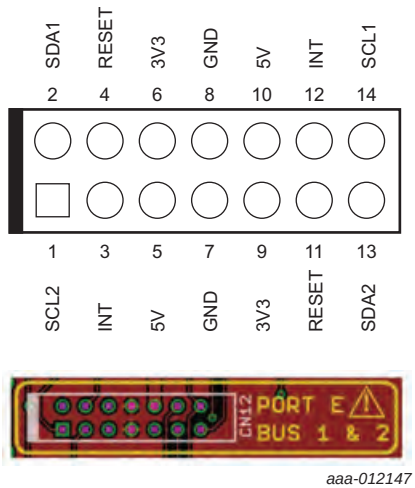


**Fig 71. Fm+ development board Port E connector**


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# 8. Bridge board (OM13399)

The Bridge Board (OM13399) (supplied in the kit) provides attachment of old style with a 9-pin, in-line, non-polarized connector NXP designed I²C demo boards to the Fm+ Development Board (OM13260). The Bridge Board (OM13399) can attach to any daughter card Port (A – D) inclusive. See Figure 72 and Figure 73.

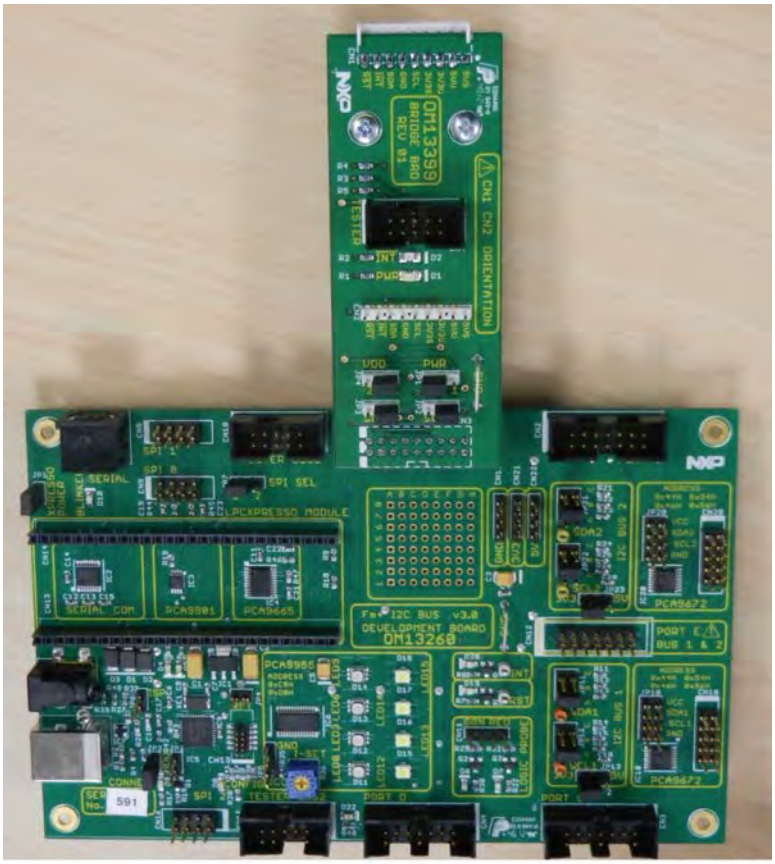


**Fig 72. Bridge board (OM13399 attached to the Fm+ development board (OM13260)**

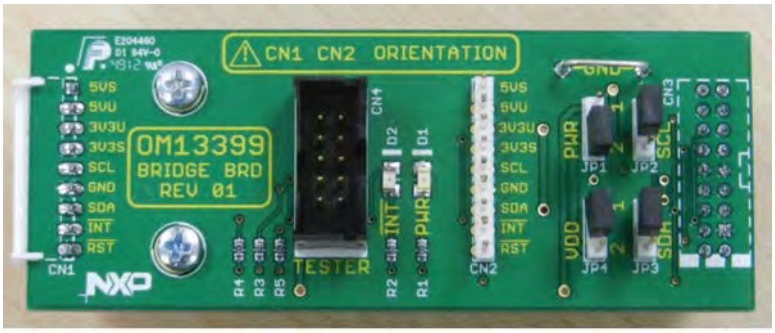


**Fig 73. Bridge board (OM13399)**


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## 8.1 Theory of operation

The Bridge Board is mostly a mechanical platform for the old style with a 9-pin, in-line, non-polarized connector of NXP designed I²C demo boards that use a non-polarized nine position connector. Previous NXP I²C demo boards were released with both vertical and horizontal mounting, and both male pins and female sockets. The Bridge Board (OM13399) therefore has both styles. There is also a 'Tester' connector that allows direct connection of the third-party tools (see Section 9). The old style with a 9-pin, in-line, non-polarized nine-circuit connector had only one I²C-bus, with SCL and SDA signals. The Fm+ Development Board Daughter Card ports have two I²C Buses (Bus1 and Bus2) signals. One or other I²C Bus can be selected by jumpers. The power source may also be selected by jumper.

## 8.2 Circuit description

The schematic diagram has a single sheet. For clarification, only fragments of the schematic are shown here. The full schematic should be downloaded if required. The circuit is simple.

### 8.2.1 Fm+ development board (OM13260) connector (CN3)

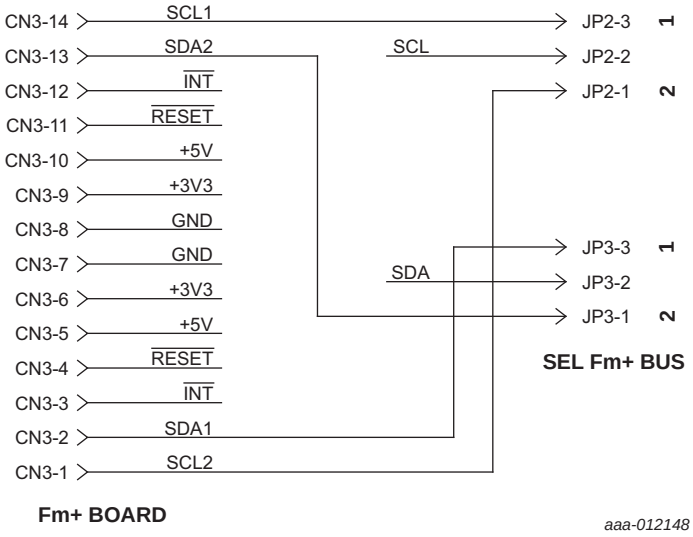


**Fig 74. Fm+ development board (OM13260) connector (CN3)**

The connector on the Bridge Board (OM13399) matches the Port connectors on the Fm+ Development Board (OM13260) See Figure 74. A Bridge Board (OM13399) can be attached to any Port A – Port D inclusive. It cannot be connected to Port E due to mechanical arrangement of the Port E connector.

The Fm+ Development Board has two separate I²C buses (Bus1 and Bus2) and one of these is selected by two jumpers, JP2 for SCL and JP3 for SDA.


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### 8.2.2 Power supply select (JP1 and JP4)

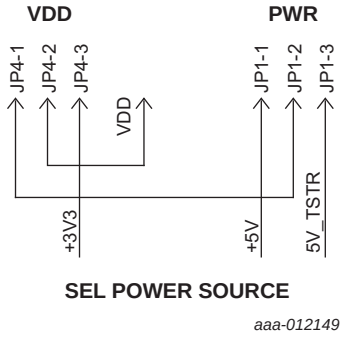


**Fig 75. Power supply selector**

There are two power sources available to the Bridge Board (OM13399) depending upon whether it is connected to the Fm+ Development Board (OM13260) or powered by a third-party tool (see Section 9).

The Tester socket provides 5 V and the Fm+ Development Board (OM13260) provides both 3.3 V or 5 V. Jumper JP1 selects the source of the 5 V power. JP4 selects either 3.3 V or 5 V as needed.

**Remark:** When the Bridge Board (OM13399) is not attached to the Fm+ Development Board and powered by the Tester, the only option is 5 V.

### 8.2.3 9-position connectors (CN1 and CN2)

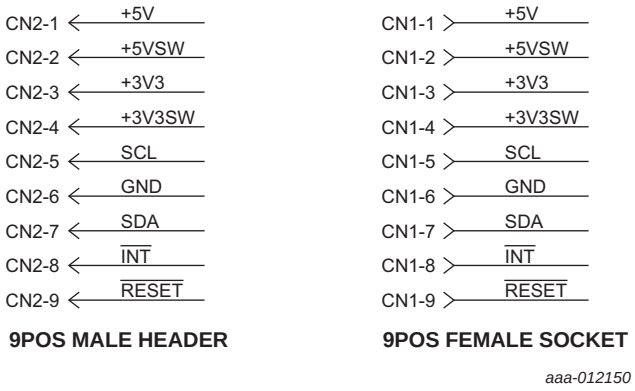


**Fig 76. 9-position connectors (CN1 and CN2)**

Two 9-position connectors are provided; both carry exactly the same signals. CN1 is female, CN2 is male.

**Remark:** These connectors are not polarized or keyed. Take care to make connection correctly.


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### 8.2.4 Tester connector (CN4)

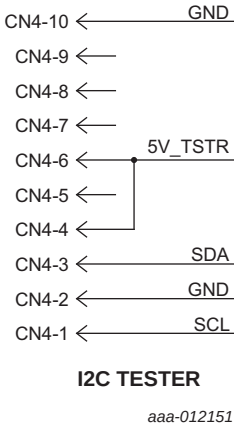


**Fig 77. Tester connection (CN4)**

The 10-position ($2 \times 5$) shrouded header connector (CN4) mates with third-party tools (see Section 9). Only I²C-bus signals and available 5 V power are connected.

**Remark:** The Tester's bus signals are connected to the two 9-position connectors and, depending upon the position of JP2 and JP3, to the Fm+ Development Board Bus1 or Bus2. Take care to avoid double termination of the I²C buses.

### 8.2.5 LED indicators and pull-ups

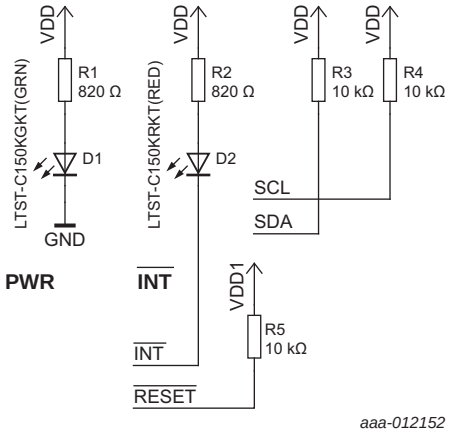


**Fig 78. LED indicators and pull-ups**

Two LEDs provide indication of power (D1, Green) and INT (interrupt) status (D2, Red). To prevent malfunction of the I²C-bus if the Bridge Board (OM13399) is used in manner that does not have pull-up on either SCL or SDA, there are weak pull-ups (R3, R4). These may be replaced with lower value resistors (or removed), as needed.


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## 8.3 Example using PCA9632 (OM13269)

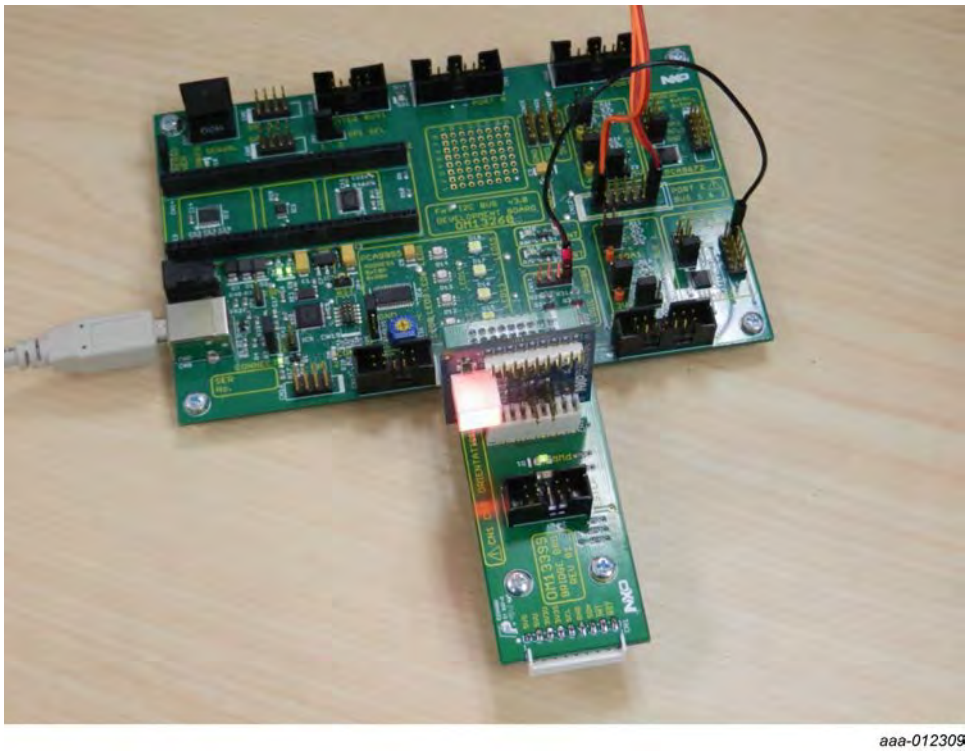


**Fig 79. Bridge board (OM13399) used to attach a PCA9632 (OM13269)**

The Bridge Board (OM13399) (supplied in the kit) provides attachment of old style with a 9-pin, in-line, non-polarized connector NXP designed $I^2C$ demo boards to the Fm+ Development Board (OM13260).


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# 9. Third-party tools

Generation, inspection and logging of $I^2C$-bus data is easily achieved with third-party development tools from a number of suppliers: SB Solutions, Inc. (www.i2ctools.com) and Total Phase (www.totalphase.com).

SB Solutions supplies a range of tools driven from USB and outputs to $I^2C$ and SPI. The user interface is very similar to the Fm+ Development Board GUI, and a DLL is provided for custom development. These tools are not supplied in the kit, and must be purchased directly from the vendor.

Total Phase supplies two tools called Aardvark (host adapter) and Beagle (bus logger) that connect directly to the Fm+ Development Board (OM13260). These tools are not supplied in the kit, and must be purchased directly from the vendor.

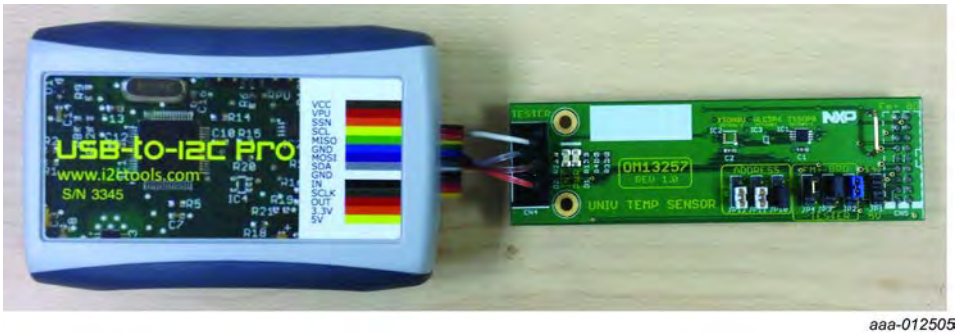


**Fig 80. SB Solutions USB-to-I2C Pro connected to an Fm+ Development Board daughter card**


**Fig 81. Aardvark Host Adapter connected to the Fm+ development board (OM13260)**


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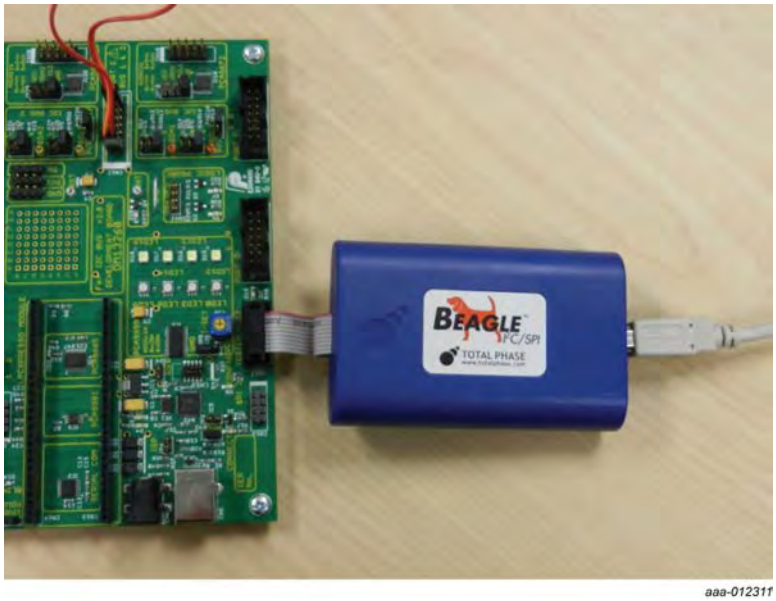


**Fig 82. Beagle Bus Logger connected to the Fm+ development board (OM13260)**


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# 10. Abbreviations

**Table 7. Abbreviations**

| Acronym | Description |
|---|---|
| DLL | Dynamic Link Library |
| EVM | Evaluation Module |
| FET | Field-Effect Transistor |
| Fm+ | Fast-mode Plus |
| GPIO | General Purpose Input/Output |
| GUI | Graphical User Interface |
| HID | Human Interface Driver |
| $I^2C$-bus | Inter-Integrated Circuit-bus |
| I/O | Input/Output |
| ISP | In-System Programmable |
| JTAG | Joint Test Action Group |
| LDO | Low Drop-Out |
| LED | Light-Emitting Diode |
| MCU | MicroController Unit |
| OS | Operating System |
| PC | Personal Computer |
| PCB | Printed-Circuit Board |
| RC | Resistor-Capacitor network |
| RGB | Red/Green/Blue |
| SPI | Serial Peripheral Interface |
| SWD | Single Wire Debug |
| USB | Universal Serial Port |

# 11. References

**[1]** **UM10785, *"Fm+ Demo Board Software Installation Guide"* —** NXP Semiconductors; 25 February 2014; www.nxp.com/documents/user_manual/UM10785.pdf



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