Freescale Semiconductor
Design Guide

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MPC5645S Hardware Design Guide

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1 Introduction

The MP5645S microcontroller provides a single-chip solution to complex vehicle cockpit applications. It is capable of controlling up to two TFT LCD panels and up to six stepper motors without any external drivers. Further functionality can be added through additional hardware connected to its sound generation, serial flash and SDRAM interfaces.

This level of integration brings challenges to the hardware and software designer using the MCU. To help address these challenges, this hardware design guide discusses hardware design techniques that can help avoid undesirable effects caused by fast clocks and I/O switching. This hardware design guide also reviews the primary peripheral connections from a schematic and layout design viewpoint and software configurations which can affect hardware performance.

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2 MPC5645S Application Overview

Table 1 summarizes the hardware interfaces present on the MPC5645S and how they are used in a typical application.

Table 1. MPC5645S Typical Functions

Function	Application	Typical Configuration
CPU	Software	125 MHz clock
GFX2D	OpenVG	125 MHz clock
DCU	Graphics panel	28 I/O, 8 – 32 MHz clock, 3.3 V
DCULite	Graphics pane	28 I/O, 8 – 32 MHz clock, 3.3 V
Stepper motor Controller	Gauges	24 I/O, PWM, 5 V
SDRAM Interface	DDR RAM	Up to 61 I/O, 125 MHz clock, 1.8 V, 0.9 V
SGM Interface	Sound output	Up to 4 I/O, 12 MHz clock, 3.3 V
CAN Communications	CAN bus	2 I/O, 500 kHz clock, 3.3V
LIN Communications	LIN bus	2 I/O, 20 kHz clock, 3.3V
QuadSPI	Serial flash	Up to 12 I/O, 80 MHz clock, 3.3V
VIU	Video input	9 I/O, 27 MHz clock, 3.3V
Nexus	Debugging	4 – 21 I/O, c. 8 MHz clock, 3.3 V
ADC	Analog input	Up to 20 pins, 5V
General I/O	Tell tales, switches	Available I/O, 3.3 V

As can be seen there are a large number of independent and energetic interfaces in use simultaneously in a typical application. The I/O includes up to four independent functions multiplexed on each pin and therefore I/O allocation must be carefully considered. In addition the application may require at least four separate power supplies:

- 5 V for ADC, stepper motors and possibly voltage regulator
- 3.3V for other I/O and possibly voltage regulator
- SDRAM supply of 1.8 V, 2.5 V or 3.3 V
- SDRAM reference/ODT supply of half the SDRAM voltage

The design of the MPC5645S hardware should take into account the power supply requirements of the device and its associated peripherals, the stability of its power supply and I/O as required, decoupling, allocation of I/O functions, configuration of I/O, signal routing and EMC considerations. This hardware design guide considers each of these areas in turn.

3 MPC5645S I/O Allocation

Before commencing schematic design it is important to allocate functions to specific pins on the MCU. This allows identification of any conflicts when functions are shared on a pin and identification of initial power supply requirements. Note that not all functions are available in all packages. For example the SDRAM option is only available in the 416 MAPBGA option. Similarly the 176 LQFP package only supports a single TFT panel.

The I/O allocation process is complex because there are a very large number of possible combinations, however, in most cases there are certain pins which are desirable to use for a particular function because they allocate adjacent pins to the same functional block. By choosing these first the number of options is reduced and it may be easier to resolve conflicts. Table 2 shows a particular combination that will be usable for many applications; however, the hardware designer should always consider other possibilities to see if there exists a better match to their needs. Note that the SDRAM interface has dedicated pins for the function.

Table 2. Possible I/O configuration

Function	Ports used	Conflicts when using these ports
DCU	Port A[0:15], Port G[0:11]	eMIOS0, I²C_1, I²C_2, I²C_3
DCULite	PN[0:15], PP[0:7], PJ0, PM12	TCON, LINFlex_2, LINFlex_3, eMIOS0, FlexCAN_2, SGM
Stepper motor Controller	Port D, Port E	eMIOS0, eMIOS1
SGM Interface	PB[7:9], PB11	DSPI_0, eMIOS1, FlexCAN_1
CAN Communications	PB[0:1]	LINFlex_0
LIN Communications	PB[12:13]	eMIOS1, DSPI_0
QuadSPI	Port F[10:15], PF[5:6], PJ[13:15], PK1	Nexus, eMIOS1, VIU
VIU	PJ3, PK[4:6], PL[4:8]	eMIOS0, eMIOS1, DCULite, DSPI_2, TCON
Nexus	PH[0:3]	No conflict but if full Nexus functionality is required the MAPBGA package provides this with no conflict where the LQFPs share this function on other ports
ADC	Port C[0:13], Port L[0:3]	FlexCAN_0, FlexCAN_1, DSPI_1
32 kHz crystal	Port C[14:15]	ADC

Bear in mind that in addition to the basic function some connected peripherals may require another configuration bus such as I²C or SPI. If some pins are required for interrupt purposes then further compromise may be required since only a subset of pins can be used in this way.

This hardware design guide uses the above port allocations when discussing I/O.

3.1 I/O configuration and software notes

The I/O pins on the MCU are configured using the SIUL module. Each pin has a PCR register which configures the function of the pin and some other features such as output and input buffer selection, drive strength, pull-ups and downs, and open drain options. Where the pin shares functions it may also have a PSMI register which determines which of the possible pins provides the input to the associated module. In this case the PSMI register is associated with the module function rather than the pin.

4 Peripheral Interfacing

This section discusses examples of connecting representative peripherals to the MPC5645S. The choice of peripherals influences the choice of I/O pin to use and also the power supply design for the board.

4.1 DCU and DCULite

The DCU and DCULite are specifically designed to allow direct connection between the MPC5645S and TFT panels which include a timing controller (TCON). The DCU has an option to allow connection of a panel without an embedded TCON, however this option is not discussed here.

In general connection from the MPC5645S to the panel is straightforward. Pins are connected such that the red, green and blue outputs connect to the same named pins on the panel. There are four other signals which may or may not all be required. These are pixel clock (normally required), data enable, horizontal sync (HSYNC) and vertical sync (VSYNC). Sometimes some other active signals are required to enable the panel or backlight at appropriate points in the power-on sequence and dimming control for the backlight. These additional signals must be provided by other I/O pins not associated with the DCU or DCULite.

The LCD panel may require three voltage supplies. These are typically 5 V, 3.3 V and a backlight voltage ranging from 3.3 V to 30 V. In most cases the 5 V and 3.3 V supplies to the MCU are suitable for use with the panel as well and so the current and stability requirements may be added to that of the rest of the board. The backlight may be explicitly generated to meet the requirements or a dedicated backlight driver may be chosen for the purpose. Freescale supplies backlight drivers suitable for use with many panels. The MC34845 is a 6 channel backlight driver that can be used for this purpose.

Depending on the operating environment it may also be important to consider the location and operating frequency of the panel. It is typical for the panel to be directly connected to the same board as the MPC5645S however if the panel must be at a greater distance then the drive strength of the MCU pins must be considered. Similarly, a fast clock rate for a panel may require a higher drive strength capability for the pins which may in turn cause impedance matching problems with the panel. The best way to examine the panel drive strength requirements is to simulate how the pin drive strength affects signal integrity. A high drive strength may create undesirable ringing and spurious edges on the signal. If this result is found then standard impedance matching techniques may be used. Flat Flexible Cables (FFC) are most commonly used to connect the panel to the board and these should also be considered when simulating behavior. At its simplest, the insertion of a resistor in series with the DCU signals may be

sufficient to address the problem. Based on Freescale simulations, values of 39 Ω or 79 Ω (when FFC in use) are good starting points for impedance matching resistors.

See Figure 1 for an example of how to connect the DCU pins to a generic TFT LCD panel.

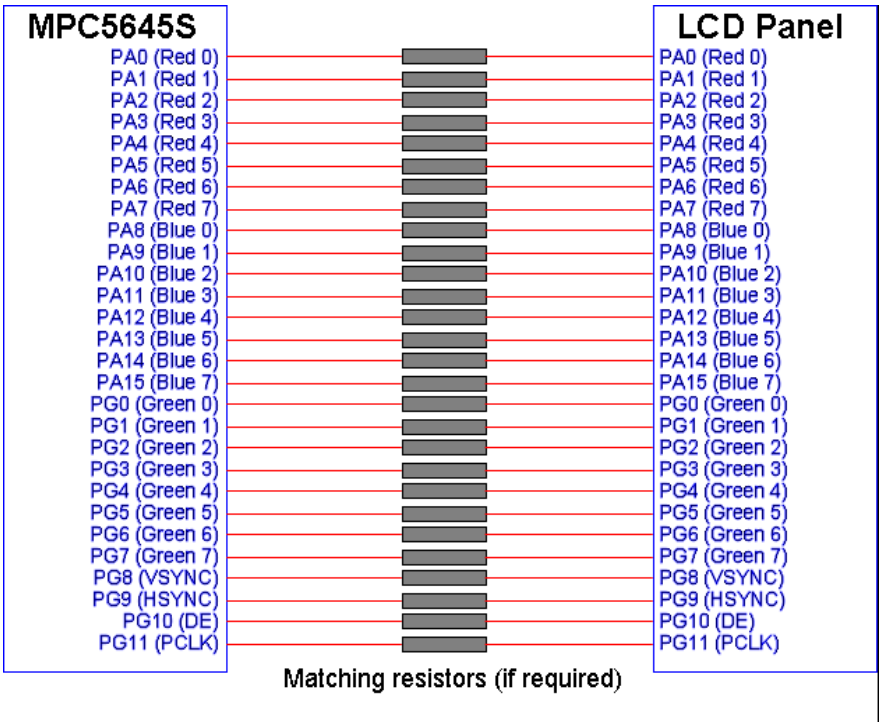

Figure 1. Connecting DCU to an LCD panel

4.2 Stepper motor controller and stall detection

The stepper motor controller shares its functions with the stepper stall detect module on all pins so no special wiring is required to switch between them. Once again the modules are intended to directly connect the MPC5645S to suitable low current stepper motors used to drive small gauges.

The SMC provides 6 x 4 pin interfaces to connect to the coils used on the stepper motor. All of the interfaces are identical and rely on PWMs of an appropriate polarity to drive each of the coils. By appropriately accelerating and decelerating the motor through the use of the PWMs it is possible to minimize system integrity issues. The exact drive approach will vary from motor to motor depending on the coil and gear specifications and the load created by the needle.

The stepper motor functions will typically be supplied at 5 V and since power is being switched across coils there is the potential of spikes being induced back onto this power supply. Therefore it is prudent to take care when routing these signals and when connecting the power supply to avoid undesirable effects on sensitive signals.

Figure 2 illustrates a typical connection schematic.

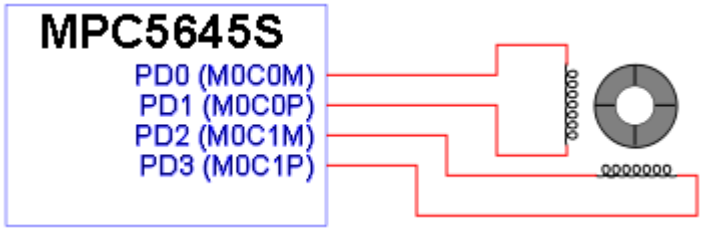

Figure 2. Connecting a stepper motor

4.3 SGM Interfacing

There are two options available when using the SGM:

- PWM output
- I²S

The PWM output consists of a single pin outputting a PWM whose duty cycle is varying at the sample rate of the audio data. The I²S option is a 4 pin interface used to send stereo 16-bit sample data to an external sound D to A converter. The second option can achieve CD quality sound while the first can achieve perhaps AM radio quality.

The hardware connections are therefore different for the two solutions. The PWM solution normally looks like Figure 3 where the PWM output is filtered and has the dc offset removed before amplifying.

We need to calculate the PWM and sample rates before we can define the filter. As a rough guide to the filter characteristics consider the following calculation:

Eqn. 1

$$f_{PWM} = 2^{sample\_depth} * f_{sample\ rate}$$

Where f_{PWM} is the (carrier) frequency of the audio signal

sample_depth is the number of bits in each audio sample

$f_{sample\ rate}$ is the audio sample rate

This formula assumes exactly one sample per PWM period.

In an ideal world we will produce CD quality output using this approach but it is not possible because the PWM operating clock will be too large as shown in Equation 2.

Eqn. 2

$$f_{PWM} = 2^{16} * 44100 = 2{,}890{,}137{,}600\ Hz$$

Therefore a practical output has to sacrifice sample depth or sample rate or both. In practice the sounds required by typical applications in the vehicle cockpit space are not high bandwidth and therefore it tends to be more satisfactory to reduce the sample rate and keep the sample depth at 10-bit or above. A suggested

compromise would be a sample depth of 10 and a sample rate of 11025 kHz which respects the 44.1 kHz reference point. This requires a PWM as given in Equation 3.

Eqn. 3

$$f_{PWM} = 2^{10} * 11025 = 11{,}289{,}600\ Hz$$

The SGM operates from a clock which is one half of the system clock and so is typically 62.5 MHz. This is approximately 5.5 times the calculated clock and so it is possible to achieve by operating the PWM at a slightly higher rate than calculated but keeping the sample rate the same. This will result in there being slightly more than one sample per PWM duty period.

NOTE

If the 44.1 kHz reference is abandoned it is possible to operate at a higher sample rate but this in turn leads to a faster clock being driven from the MCU with all the attendant concerns over signal integrity and EMC.

With this calculation complete we can design a filter to remove the unwanted PWM “carrier wave”.

The sample rate is 11 kHz and therefore the maximum frequency usable without aliasing is 5.5 kHz. Depending on the audio content it may be better to have a filter cut off at a lower frequency and have a less sharp roll-off than a cut off at 5.5 kHz which may require multiple orders of filtering to achieve a satisfactory sound. In practice the final sound amplifier will likely have additional filtering so the filter should be designed with this in mind as well. Figure 3 shows a typical filtering system for the PWM output.

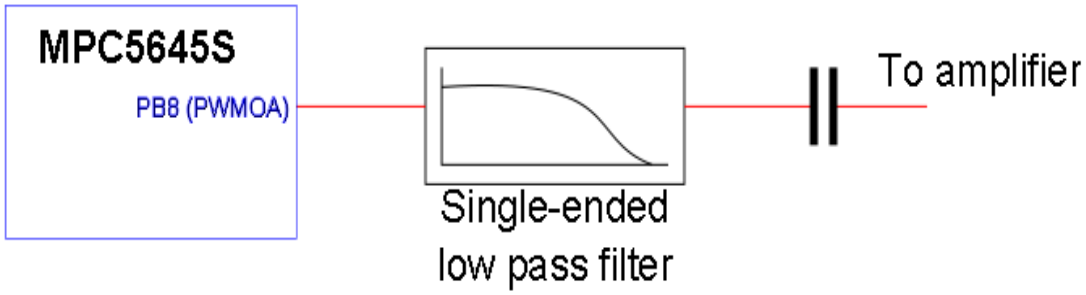

Figure 3. SGM PWM filtering system

The I²S option uses the industry standard 4-pin output-only interface to send digital audio data to a hardware decoder/D to A converter. These often come with an integrated headphone and line-level amplifier. Freescale has such a device (SGTL5000) and Figure 4 illustrates how this is connected to the MPC5645S. The MCLK is an over-clocked sample rate clock of 256x or 512x the sample rate and therefore will typically operate at 11.3 MHz and so care must be taken when choosing the port drive strength and layout for this signal. The DO pin is a serial bus which transmit samples at 32 x 44100 = 1.5 MHz.

Note that the SGTL5000 also requires an I²C bus for configuration as shown in the figure.

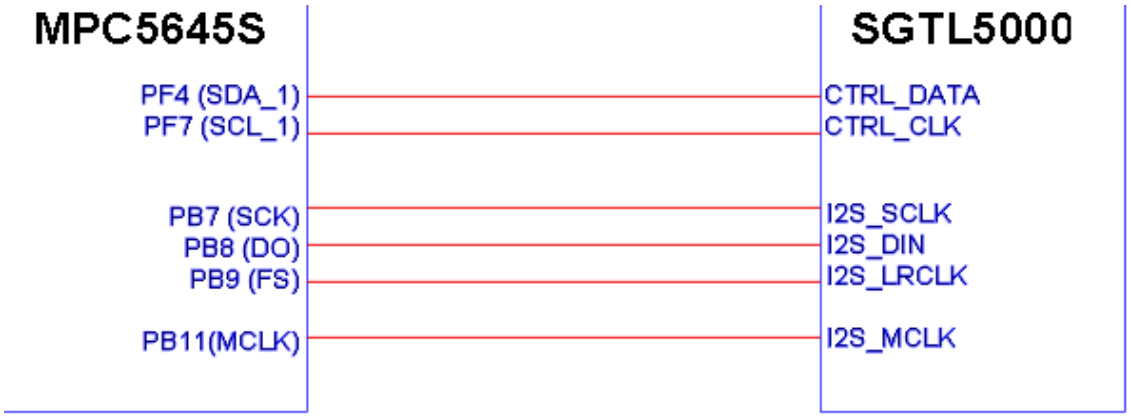

Figure 4. SGM I^2S Interface

4.4 CAN and LIN communications

The CAN and LIN interfaces on the MC5645S are straightforward to connect to physical interfaces that allow the connection of the MPC5645S onto the associated communication busses.

The CANL and CANH signals connect to the physical interface functions of the same function. There may be other configuration signals required to configure the port depending on the physical interface IC selected.

The LIN Rx and Tx pins connect to the physical interface functions of the same function. There may be other configuration signals required to configure the port depending on the physical interface IC selected. Note that the LINFlex module also functions as a buffered UART if required.

4.5 Serial Flash

The QuadSPI interface provides a high-speed dual-quad interface to external serial flash devices. The interface can be operated as a single quad I/O interface if the higher dual-quad bandwidth is not required. This interface provides two clocks – one to each serial flash – operating at up to 80 MHz and therefore care needs to be taken when placing and routing the serial component.

Freescale recommends that simulation is undertaken when laying out the serial flash interface to see if the high drive strength is required and if impedance matching is suitable to avoid undesirable signal issues.

Figure 5 shows the connections required to two standard serial flash devices from Spansion.

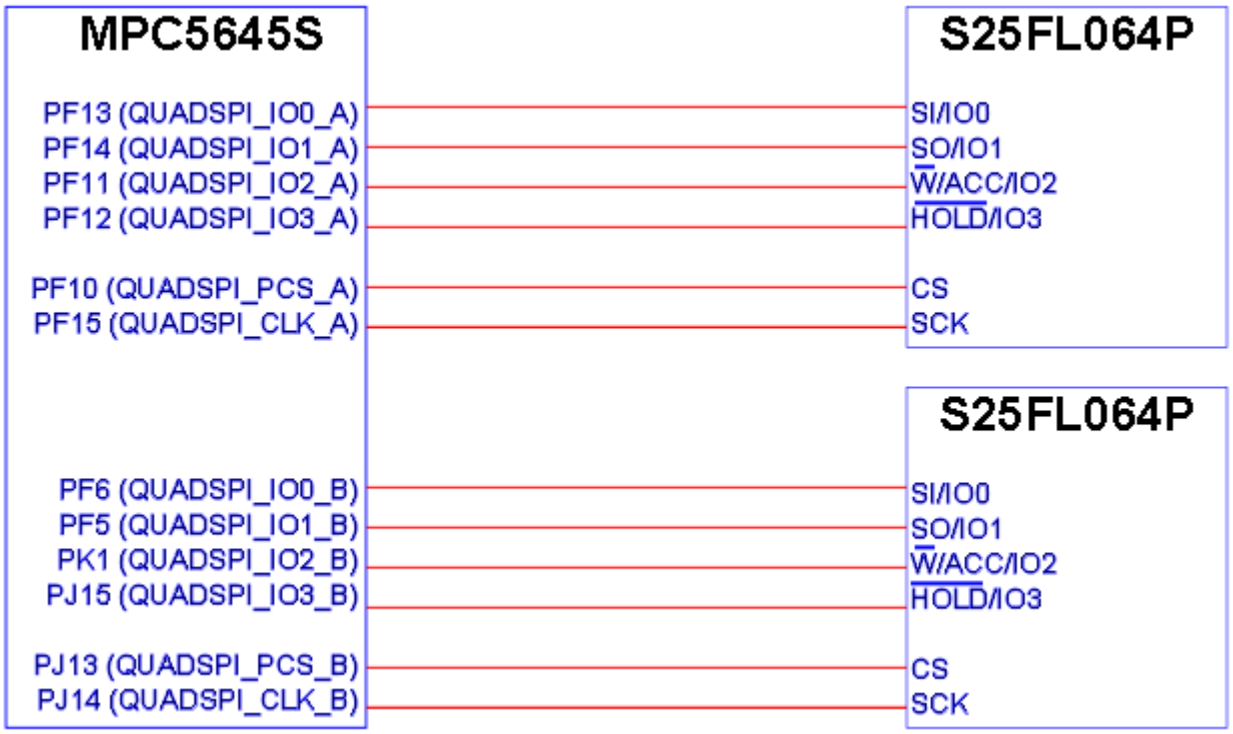

Figure 5. Serial Flash interface

4.6 SDRAM Interface

The nature of the SDRAM interface means that this is the most complex peripheral to connect in the application. The SDRAM interface is only available in the 416 MAPBGA package and provides a 32-bit data interface, up to 19 address and bank address lines, four each of data strobe and mask signals for each of the byte lanes, differential clock at up to 125 MHz (250 MHz DDR), column and row selects, one chip select, write strobe, four ODT supply pins and a reference voltage pin. The interface supports DDR1 and DDR2, SDR and LPDDR and thus can operate at 3.3 V, 2.5 V or 1.8 V.

The characteristics of the SDRAM interface are fast signals with associated fast transient currents, a sensitive external reference voltage for data detection and many signals to connect. All of these present a challenge to an embedded system which also includes fast, high current switching on other ports in the same package.

Both the SDRAM and the MCU have software options for optimizing the drive strength used by the output drivers. This can help to reduce undesirable signal integrity problems. For the MCU the configuration is performed in the SIUL_PCR[202:268]. For the SDRAM the configuration is done as part of its initialization process. If DDR2 is used then the memory also has options for different ODT resistor values. On the MCU the ODT pulls are fixed at a nominal 150 Ω.

The schematic connection of the external SDRAM is fairly straightforward but care needs to be taken with the layout of the circuit. Figure 6 shows the connections required for a DDR2-based system with a single 16-bit interface. Figure 7 shows the connection with two 16-bit interfaces in use.

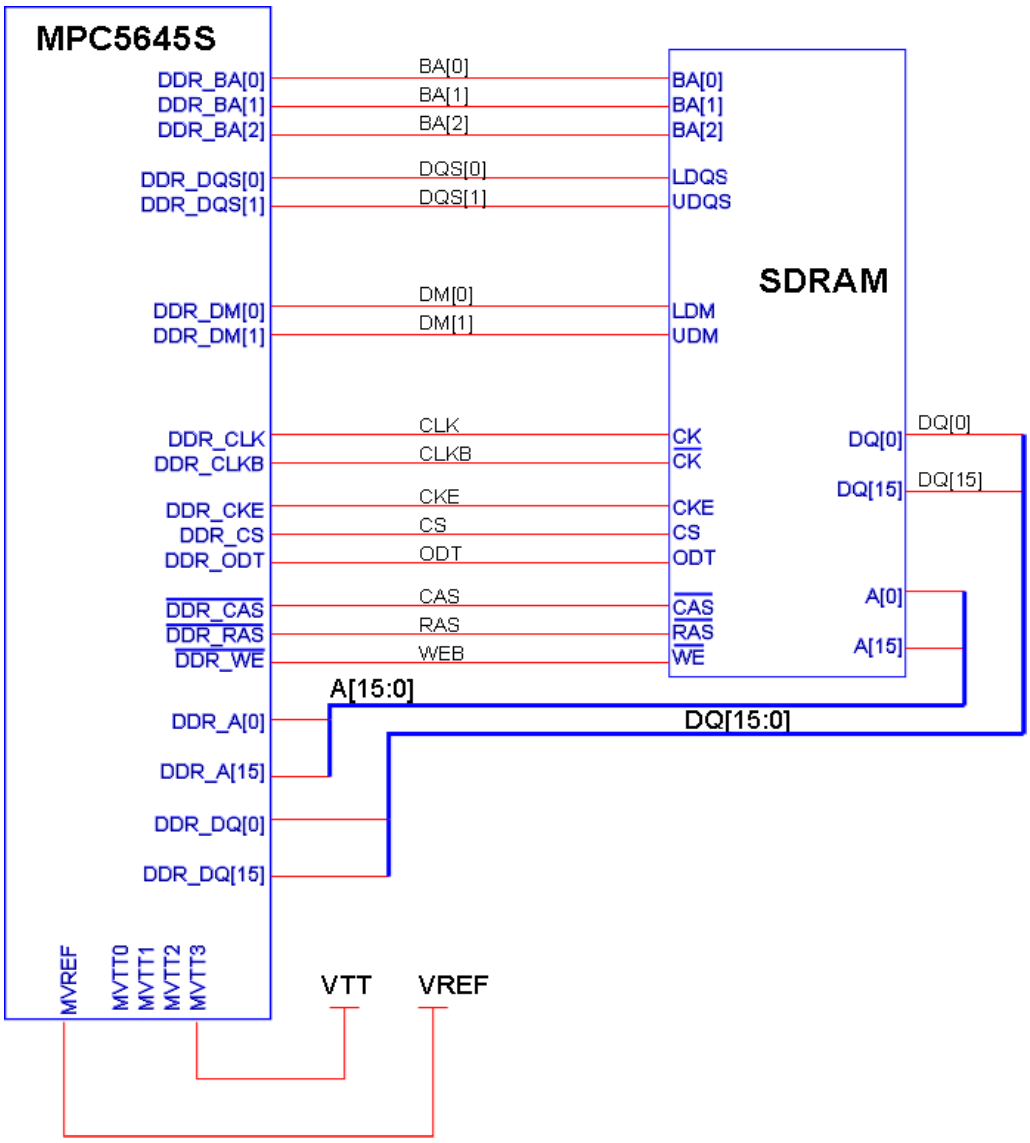

Figure 6. 16-bit DDR2 interface using a single memory

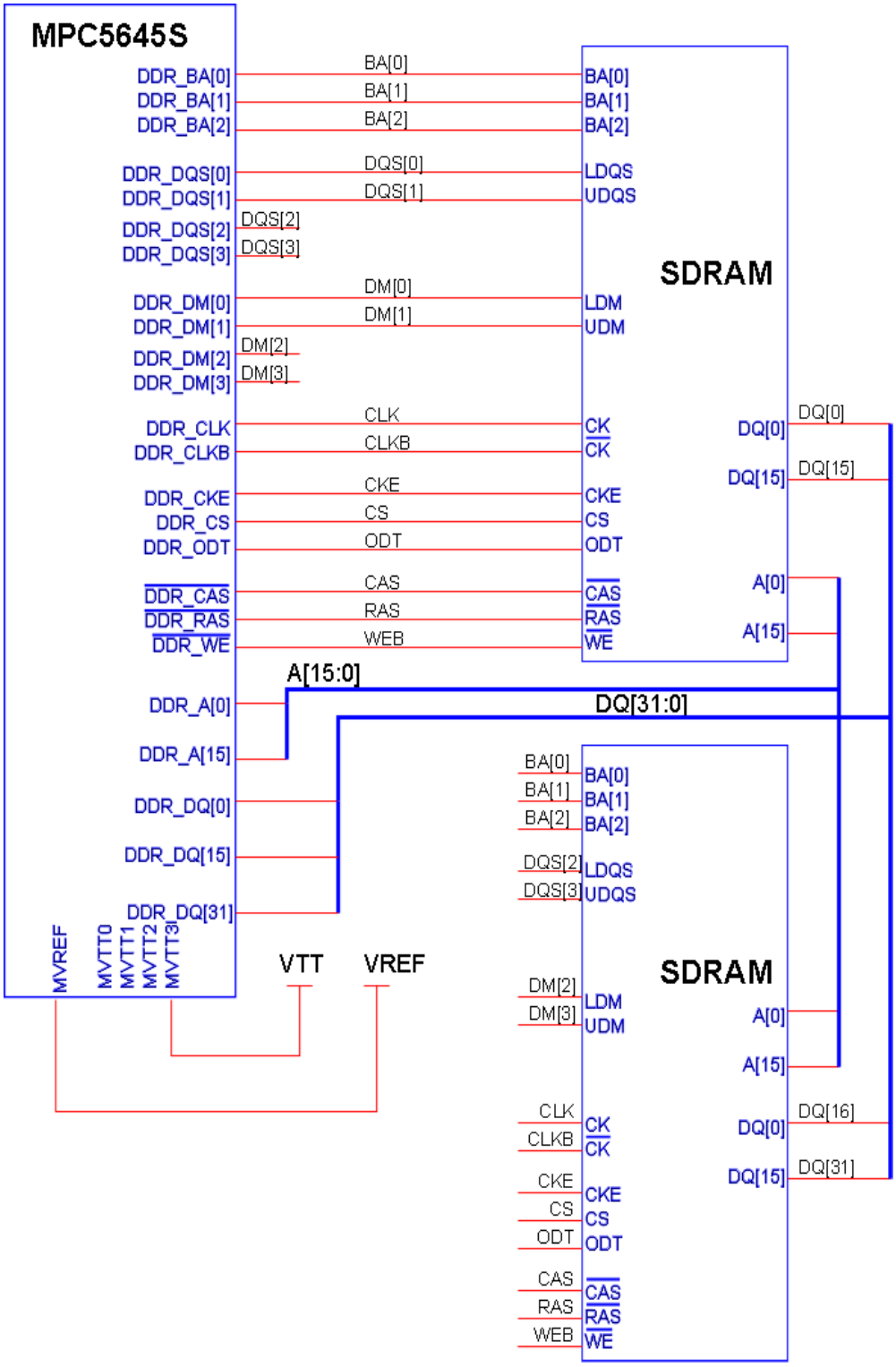

Figure 7. 32-bit DDR2 interface using two memories

It is important to note the following pin functions:

- VDD_DR is the operating voltage supply for the SDRAM pins and must be at the same voltage as the supply for the memories.
- VDD33_DR is a dedicated supply for the internal functionality of the MCU's SDRAM pins. While the I/O of the pin operates at VDD_DR its internal functions are powered by this supply.
- VREF is a 0.9V supply which is used to determine if the data from the memory is 0 or 1. It must be stable to within a few 10 MV.
- MVTT is the supply voltage for the On Die Termination (ODT) feature of the DDR2 interface. It must supply 0.9 V to all the pull resistors for each data line on the part. This means potentially high currents during switching and a stable supply is required if ODT is active. See Figure 8 as given below:

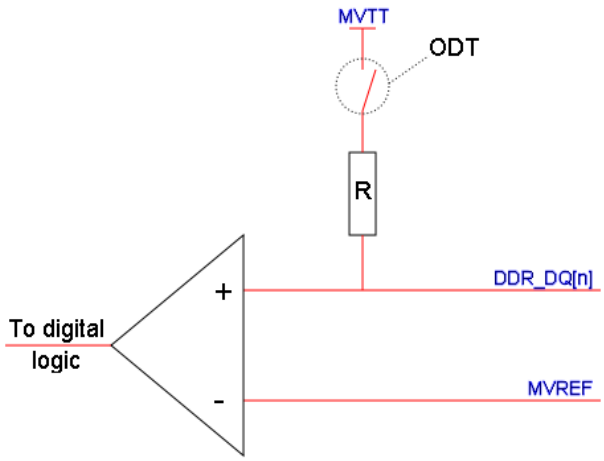

Figure 8. On Die Termination Arrangement

The SDRAM pins have special configuration options in their associated SIUL_PCRs which allow the configuration of the pin to the type of memory in use. There are also options for reduced drive strength. Refer to the MPC5645S Reference Manual guidance for PCRs 202-268 for details.

There are extensive guidelines available for connecting DRAM memories from the memory manufacturers and their advice should be used in conjunction with this hardware design guide.

In general, the best way to ensure operation of the SDRAM interface is to simulate the layout. As a result of simulations of boards and measurements on manufactured boards Freescale provides the following recommendations:

- Provide a stable reference for MVREF which also tracks the SDRAM supply voltage. In many cases acceptable performance may be achieved by using a simple resistor divider arrangement if the resistors are well matched. The addition of bypass capacitors may be required if the DDR supply voltage is noisy. Alternatively use a custom voltage reference IC. Figure 9 shows a MVREF reference circuit.

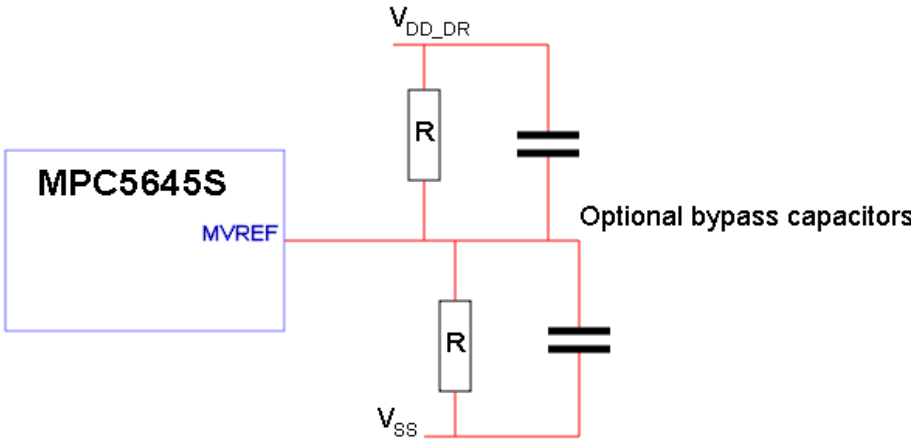

Figure 9. Simple MVREF reference circuit

- Size the MVTT supply appropriately for the size of the data bus in use and the termination resistors on-chip. The ODT resistors are fixed at a nominal 150 ohm on the MPC5645S. This means that a peak current of 0.9/(32 parallel 150R) = 190 mA is possible for 32 data lines. There exist dedicated supply ICs designed for this purpose.
- It may be possible to avoid using ODT since the typical application will be a point-to-point system and the memory will be very close to the MCU. Simulate the system before committing to this option.
- Consider adding series resistors in the signal paths. The value can be adjusted to improve signal matching and they provide a convenient probe point on the hardware.

4.7 Configuring the SDRAM memory

SDRAM achieves its high performance by using a state machine to schedule memory access. This state machine requires to be configured before use. The steps to configure the device vary between memory architectures but in principle the steps all involve writing values into the memory configuration registers. This step should configured after enabling the MPC5645S memory controller and SIUL.

To place the SDRAM in configuration mode first raise the CKE pin, enable the SDRAM clock and enter command mode. These functions are performed by writing 0xF0000000 to the DRAMC_SCR register. From then the DRAM commands are written into the DRAMC_CMD register and these values then appear on associated pins of the MCU. See the MPC5645S Reference Manual for how the bits in DRAMC_CMD map to the physical pins on the MCU.

When all commands have been sent clear the CMD bit in the DRAMC_SCR register to enter normal operation.

There are very many configuration options for the DRAMC and Freescale has created an Excel spreadsheet which allows automatic calculation of these values for a given memory/board specification.

4.8 VIU Interface

The VIU interface takes an ITU-656 format signal, decodes it and stores the video data in memory. The input consists of eight data lines and a clock. Note that the VIU shares its functionality with the background video input of the DCU (PDI) and care should be taken when selecting the input pins to use. The MPC5645S Reference Manual includes guidance on the configuration of the video input pins. The pins identified in Table 2 offer the most flexibility.

The VIU input can either be driven directly from a digital camera or from a video ADC. In both cases it is likely that an I²C interface will exist to configure the peripheral. The video signals can be high frequency and are all input to the MPC5645S so refer to the manufacturers' specification for details of connection recommendations and impedance matching if required.

4.9 ADC Interface

The on-chip ADC module directly provides up to 20 channels at 10-bit resolution. It is possible to add a further seven channels by adding an external analog multiplexer. All of the ADC channels can be configured as digital I/O and the analog path must be enabled by setting the APC bit in the SIUL_PCR register of the appropriate pin. Other functions such as digital input and output and pull devices should be disabled when using the pin as an analog input.

Protect the analog input from noise by filtering as appropriate but avoid excessively high input impedance because this affects the accuracy of the sampling phase. The MPC5645S Data Sheet includes guidance on the impedance values that affect the accuracy of the result.

5 Oscillator and Power supply considerations

This section considers the MCU's power supplies and clocks.

5.1 Oscillator design

The MPC5645S can operate from a number of clocks but the source of the primary system clock is the FXOSC which is a 4-16 MHz crystal or resonator. This crystal connects to dedicated oscillator pins and the oscillator implements a loop-controlled Pierce configuration. This configuration automatically adjusts the oscillation drive to maximize stability and minimize current consumption.

The schematic connection to the crystal is straightforward – see Figure 10. The low power behavior of the oscillator means that it is not suited for overtone resonators and crystals.

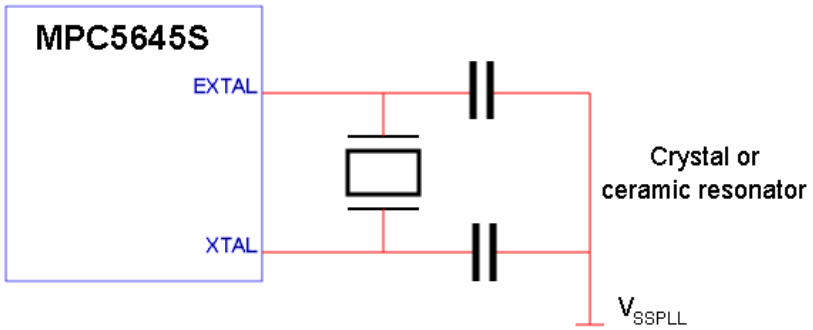

Figure 10. Crystal or Resonator connection

A second oscillator is provided called the SXOSC. This is optimized for a 32 kHz crystal and is intended for accurate time keeping even in low power modes. The connection of this crystal is as shown in Figure 11.

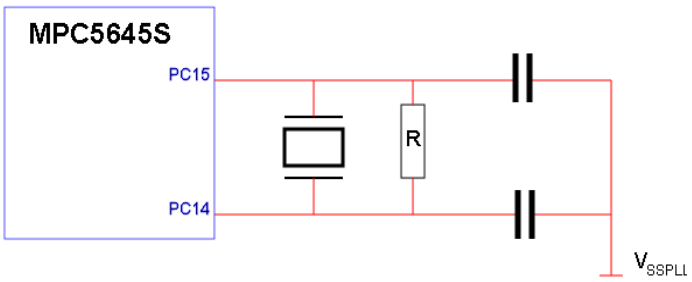

Figure 11. SXOSC connection

5.2 Power supply design

Since there are a number of different power supplies required in a typical application the sequencing of them becomes important. The MPC5645S Data Sheet includes guidance on the required sequence and this should be followed to ensure correct operation.

The MPC5645S requires a 1.2 V supply for its internal logic and this is always supplied by the on-chip regulator using an external ballast transistor and stabilizing capacitance. The suitable transistors to use are documented in the MPC5645S Data Sheet. See Figure 12 for a connection example.

When sizing the power supplies it is important to include all I/O activity as well as functional requirements. There are four independent banks that may operate at different voltages and therefore must be summed independently. Include the current consumed by the 1.2 V supply in the VDDR supply (either 3.3 V or 5 V).

If possible isolate power supplies that share the same voltage supplies. In particular the VDD33_DR supply for the SDRAM pins shares the same supply as the general I/O VDDE_B supply and both benefit from isolation from each other. Consider the addition of ferrite beads and capacitors to isolate noise from each reaching the other.

5.3 Decoupling capacitance

The basic guidance for the decoupling requirements is for 100 nF between each VDD/VSS pair and a stabilizing 10 µF capacitor between VDDR and VSS. Improved stability on the power supplies may be achieved by placing a pair of capacitors at each pin pair but the best results are achieved by optimizing the location of the capacitance as a priority.

Provide 100 nF capacitors for every pair of data lines at the relevant MVTT pin.

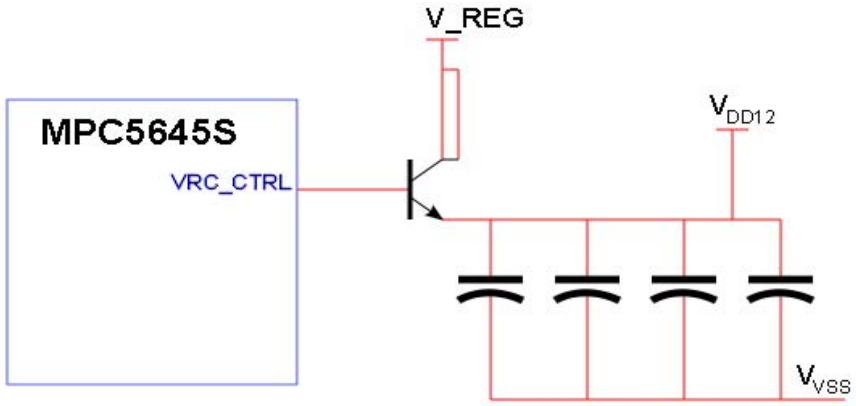

Figure 12. On-chip VREG Ballast example

6 Board Layout Considerations

The layout considerations given in this section are primarily based on the 416 MAPBGA package which is the most complex example.

6.1 Board Stack up

Most of the examples given here use a board stack-up of 6 layers as shown in Figure 13. There are two power planes and the VDD supplies share part of this plane. It is possible to use fewer layers with the smaller LQFP packages but with MAPBGA it is hard to access all of the signals without the additional signal layers.

Table 3. Board Stack Up

Layer	Name
1	Top Signal
2	Ground Plane
3	Internal Signal 1
4	Internal Signal 2
5	VDD Power plane
6	Bottom Signal

6.2 General board guidance

Much of the following guidance is taken from Section 7, “Further Reading item [4] and applies to the board in general.

There are many active signals sharing ground planes in the application so consideration should be given to the addition of ground return/transfer vias as discussed in Section 7, “Further Reading item [4].

Maintain at least 1w spacing between all signals - “the higher the spacing the better”. If a ground trace is closer than any other signal the EMC field will be smaller and disturbance will be reduced or eliminated.

6.3 Power supply layout

As far as possible keep the power supplies as close to the MCU as possible. If the supplies need to be some distance away then consider additional bulk capacitance close to the MCU to support rapid turn-on of functions (especially SDRAM) or minimize track inductance.

6.4 Decoupling

Place all decoupling as close as possible the supply pins. For MAPBGA this means on the opposite side of the board. In Figure 14 we can see the 0402 capacitors tightly packed into the area immediately under the MAPBGA pins.

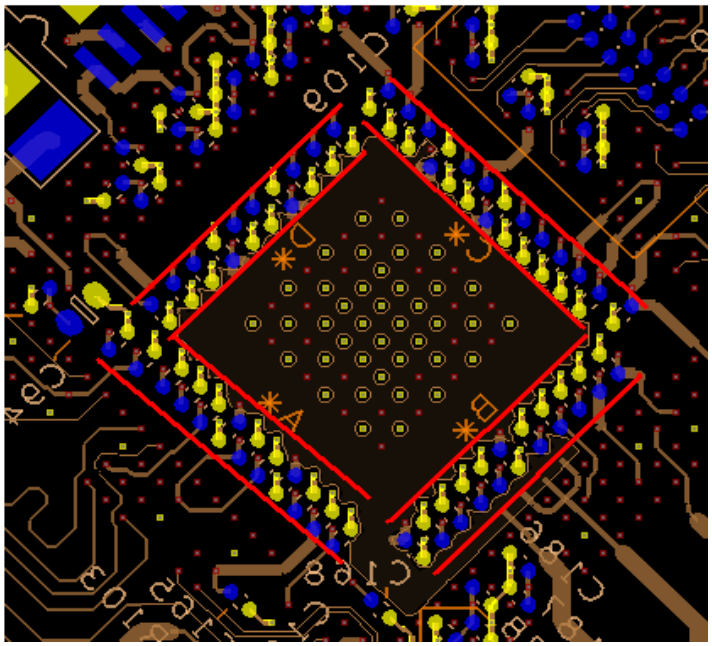

Figure 13. Example of decoupling capacitors in MAPBGA layout

6.5 Oscillator layout

On the 208 LQFP and 176 LQFP devices the oscillator layout is straightforward. See Figure 15 where Y1 is the crystal footprint.

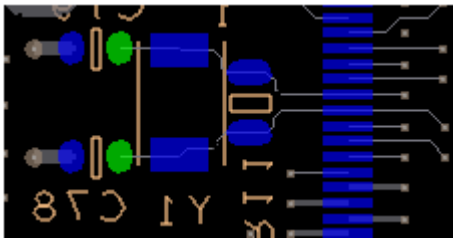

Figure 14. Example oscillator layout in LQFP

In MAPBGA the layout is similar because the oscillator pins are conveniently at the edge of the package. See Figure 16 where Y2 is the crystal footprint. Note that it is on the same side of the PCB as the MCU.

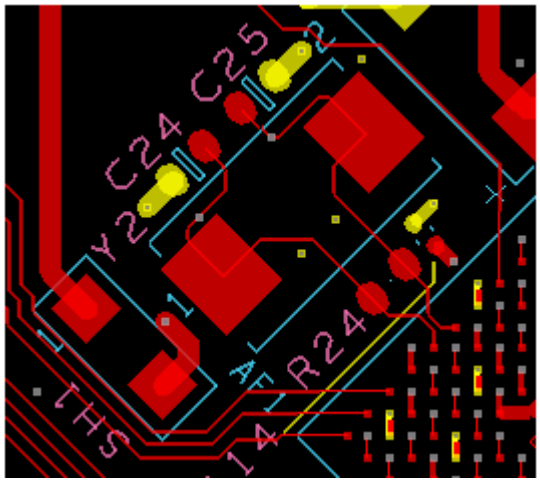

Figure 15. Example oscillator layout in MAPBGA

6.6 SDRAM Layout

The SDRAM layout follows guidelines provided by the memory manufacturer. In this example two 16-bit LPDDR memory devices are placed close to the MCU with both mounted on the top side of the board. This allows the signal tracks to be kept to the shortest length possible and simplifies power supply routing. See Figure 17 for a device placement.

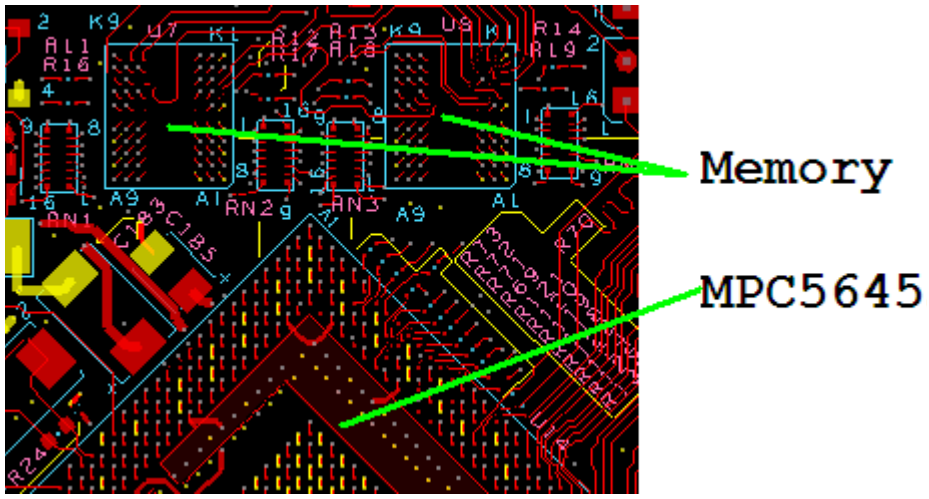

Figure 16. Memory placement

For the power supply a sub-portion of the power plane is created by a cut-out and this is then used to optimize the source impedance of the (in this case) 1.8V supply need as given in Figure 18.

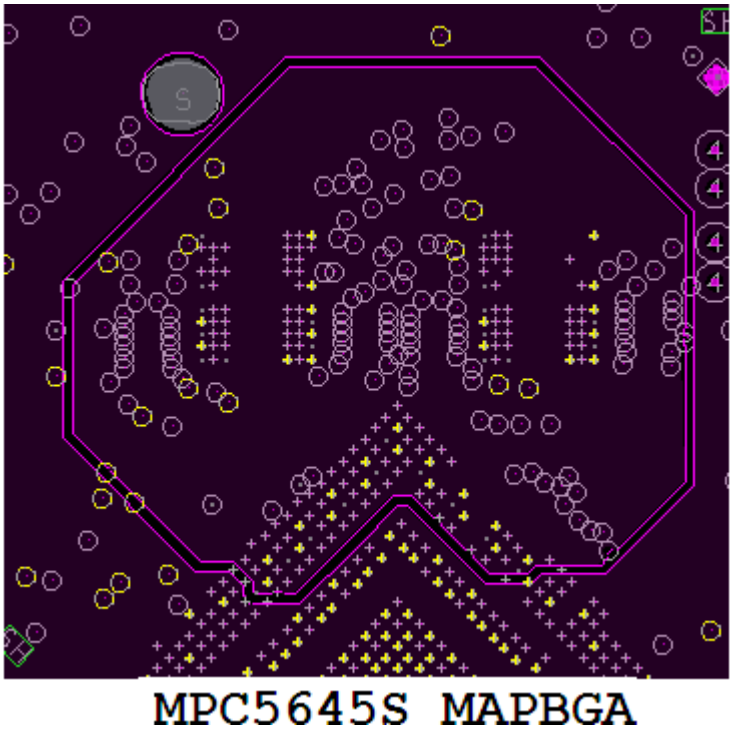

Figure 17. Example of cutout in power plane for SDRAM supply

Since the memories are so close to the MCU there is a conflict between trace-length matching which allows all the signals to be synchronous and excessive serpentine being used. The disadvantage of serpentine traces is that they reduce the area available to separate the traces and create different transfer paths for different frequencies as given in Figure 18. In this design the memory is operating at the low end of its frequency range and therefore timing is much less critical than in very fast designs. Consider routing

address lines to within 250 mil, and data/strobes/mask to within 100 mil for each byte lane. The SDRAM byte lane ports include self-optimizing adjustment of timing so data across byte lanes can remain matched to within 500 mil.

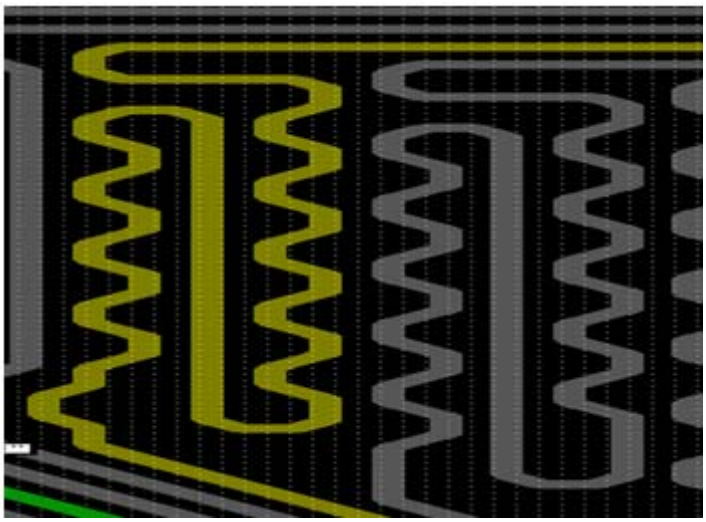

Figure 18. Example of excessive serpentine routing

The impedance of the differential clock traces should be configured to 100 ohms to maximize impedance matching.

6.7 Notes on board simulation

Two types of board simulation are recommended to optimize the design: signal simulation and power integrity. Signal simulation allows the effect of the trace layout and schematic design on the signal transfer. By simulating related signals together crosstalk and other effects can be examined as well.

Power integrity allows the stability of the power supplies to be examined. This gives a keen insight into the worst-case noise conditions on the power supplies. When considering power integrity the major energetic modules should be made active in their worst case conditions - for example, SDRAM at 125 MHz, DCU/DCULite at 32 MHz, QuadSPI at 80 MHz.

7 Further Reading

Refer to the following documents for more information available at www.freescale.com

1. MC34845 Data sheet
2. MPC5645S Data Sheet
3. MPC5645S Reference Manual
4. FTF10_ENT_F0964 Effective PCB Design: Techniques to Improve Performance, D. Beeker, Freescale

8 Acknowledgements

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