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HPC II — A High-Performance, Low-Profile Server System

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The High-Performance Computing Platform II (HPC II) is a high-performance PowerPC™ server reference design that is optimized for high-speed throughput between the processor and the memory, disk drive, and Ethernet port subsystems. The PowerPC processors supported by this board are as follows: MPC7448, MPC7447A, MPC7447, MPC7445, and MPC7441.

HPC II is designed to the micro-ATX chassis, so it can be used in a 1U or 2U rack-mount chassis, as well as in a standard ATX/Micro-ATX chassis. The advanced thermal management demonstrates the low power consumption and minimal cooling requirements needed for Freescale Semiconductor PowerPC products.

This document focuses on the physical, hardware aspects of the board.The board is shipped with a board support package, boot loader, and operating system installed. Documentation of the software is provided separately, and is included with the system and with software updates.

Note that during development, the working name “Taiga” was used for HPC II. This name appears in numerous locations, including schematics, code comments, and within this document. In all cases, the names “Taiga” and “HPC II” are synonymous.

Contents

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1 Features

The features of the HPC II board are as follows:

- Processor
  - MPC7448
  - 200 MHz front-side bus
- North bridge
  - TSI109 or TSI108
  - Integrated Ethernet controllers: two 10/100/1000 base T ports
  - Two DDR2 DIMM sockets: up to 4 Gbyte at 400 MHz
  - PCI/PCI-X bus:
    - Two user-defined slots supporting PCI 2.3 at 33–66 MHz and PCI-X at up to 133 MHz
    - SATA and USB
    - Isolation of unused portions of bus to maximize frequency
  - Host local port
    - 16 Mbyte Flash memory (32 bits wide)
    - PromJet Flash emulator support option
    - 8K non-volatile SRAM
    - Real-time clock
  - DUART
  - Integrated clock generator
  - I^2C module
- SATA disk controller
  - Four channels
  - RAID-1 support
- USB interface
  - UHCI/EHCI USB 2.0 interface
  - Two ports on stacked USB header
  - Two ports on PCB header (mates with standard PC chassis connectors)
- System logic
  - Manages system reset sequencing
  - Manages system bus and PCI clock speeds
  - Controls system and user LED monitoring
  - Manages optional fan PWM control
  - Implements registers for system control and monitoring
- Clocks
  - Supports use of the internal clock generator on the TSI109

HPC II is not a desktop machine, so it does *not* include the following features:

- Video
- Audio
- Floppy
- Gameport
- Parallel port

These features are not typically needed on a server, and they just waste power and cause extra heat. If necessary, the slots on the PCI/PCI-X bus can be used.

2 System Architecture

Figure 1 shows the overall architecture of the HPC II system. The rest of this section describes the modules shown in this diagram, starting with the MPC7448 processor.

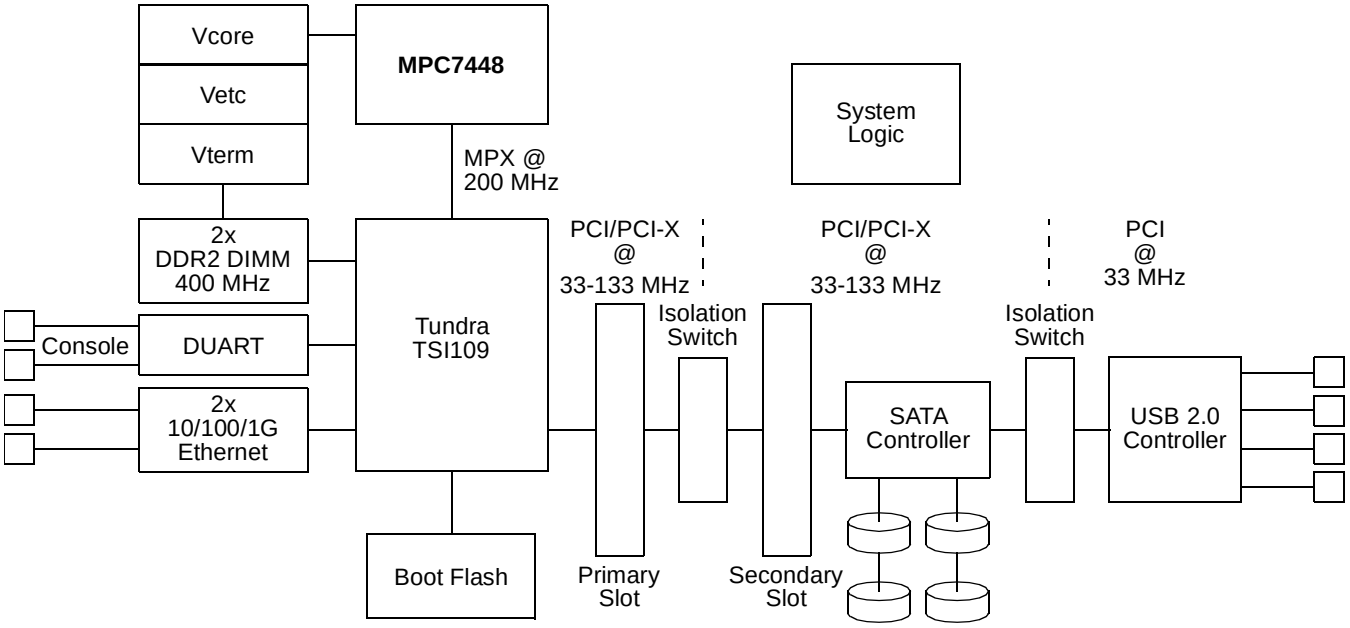


Figure 1. HPC II Block Diagram

2.1 Processor

HPC II supports the PowerPC MPC7448 microprocessor as well as the following processors:

- MPC7447A
- MPC7447
- MPC7445
- MPC7441

The system bus uses the MPX bus protocol and is optimized for 200 MHz to support the MPC7448, but it can be reduced to 166 MHz to support the MPC7447A. The bus protocol can be configured for 60x bus mode through switch settings.

The MPC7448 supports thermal monitoring through an on-chip diode connected to a dedicated monitor chip, which is configured through the I^2C bus and alerts the system if a threshold temperature is exceeded. Various options are available when an over-temperature or alarm condition is indicated, including generating an interrupt, reducing the processor core frequency through dynamic frequency switching, and increasing the fan speed.

2.2 System Controller

HPC II uses the Tundra TSI109 or TSI108 system controller (sometimes referred to as the “bridgechip”) to provide the following features:

- *DDR2 memory controller.* Control of two 240-pin DDR2 DIMM sockets for up to 4 Gbyte of memory.
- *Ethernet*. Two 10/100/1G Ethernet ports, each connected to an RJ45 jack through a Marvell 88E1111 PHY in MII/GMII mode.
- *PCI/PCI-X bus*. One interface supports PCI-X and PCI 2.3. On HPC II, the TSI109 is configured as the central resource. It drives the $\overline{\text{PCIRST}}$ signal, determines the mode and speed based on its PCIXCAP[1:0] and M66EN inputs, and drives the configuration pattern on the PCI/PCI-X bus. The multi-level PCIXCAP signal must be externally decoded. The PCI/PCI-X bus is fully described in Section 2.6, “PCI/PCI-X Bus.”
- *DUART.* A DUART to provide two RS-232 serial ports on HPC II for console support with Linux, DINK, uBOOT, and so on.
- *Host local port (HLP)*. Can be used as a general-purpose flash interface. On HPC II, HLP is used to access the flash memory, flash emulator, and the NVRAM+RTC chip. The HLP is configured to use Flash/ROM cycles in latch mode. Because the TSI109 defaults to 8-bit, non-latch mode, it must be re-configured to the correct mode using the I^2C boot feature (see below). The HLP interface is discussed in more detail in Section 2.4, “Local Bus.”
- *I^2C interface.* There is one I^2C interface in addition to the dedicated I^2C interface on the DDR2 interface. The I^2C bus is used on HPC II to connect to access several peripheral devices, including thermal monitoring, power measurement, and the configuration word for the TSI109. The I^2C bus is described in more detail in Section 2.5, “I2C Bus.”

Note that systems currently ship with the TSI109 installed, while earlier systems shipped with the TSI108 installed. For simplicity, this document refers to the TSI109 throughout. However, except where explicitly noted, all information also applies to systems shipped with the TSI108.

2.3 System Logic (TICK)

HPC II contains a small FPGA, the Taiga initializer/controller/keeper (TICK), which provides the following functions:

- Glue logic for NVRAM, flash memory, PromJet and internal registers.
  - — Chip select decoding
  - — Boot flash sectoring
- Internal registers to monitor/instrument the following:
  - — DFS control

  - Fan PWM control
  - Power off
  - Device reset
  - PCI/PCI-X mode and speed detection.
- Chip-select masking during reset
- Sequence reset signals.

The TICK is implemented in an Actel APA150 in a 256-pad micro-BGA package.

2.3.1 Reset Sequencer

The TICK reset sequencer brings the various HPC II subsystems out of reset at the proper time (see Table 1). Both the processor and the bridge chip timing specifications are based upon bus clocks. Because the HPC II supports variable bus clock speeds, the TICK uses a constant frequency base of 125 MHz.

Table 1. HPC II Reset Chronology

Event	Time (ms)	Events	irst_B	tsi_rst_B	gen_rst_B mem_rst_B phy_rst_B
t0	0	**Reset event detect** TICK internal logic in reset. External devices in reset. All CS outputs masked (high). CPU/Bridge clock controls to selected values. Set RST status.	0	0	0
t1	0.02	**TICK start** Maintain reset to all devices except TICK internal logic.	1	0	0
t2	102.0	**TSI109 start** Maintain reset to all devices except for TSI109 and TICK internal logic.	1	1	0
t3	102.2	**All other devices start** Release reset to all remaining devices.	1	1	1

Because of the long wait required between t1 and t2, the TICK system clock is divided down to generate a slow clock for a free-running counter. State machine transitions are then triggered off specific numerical counts. Note that the TSI109 has a reset output intended to drive the $\overline{\text{HRESET}}$ input of the CPU. This signal is merged with the gen_rst_B and $\overline{\text{COP\_HRST}}$ signals such that, unless defeated by switch configuration, the TSI109 can reset the CPU and hold it in reset. (See Section 3.5, “TSI109 PB_RST Disable Option (TSI_RST_DIS).)

2.3.2 Local Bus Manager

The TICK uses the TSI109 chip-select signals to implement access to several system features:

- Boot flash memory
- Flash emulator

- TICK control/status register
- NVRAM + RTC device

Apart from swapping the boot flash and flash emulator chip selects based on configuration switch settings, chip selects are generally left unaffected. The TICK also manages boot flash sectoring by controlling the most significant bit of the address bus. The local bus is fully described in Section 2.4, “Local Bus.”

2.3.3 PCI Bus Manager

The TICK detects the desired speed of the PCI/PCI-X buses and drives the correct values on the 108_PCIXCAP[1:0] and 108_M66EN signals. This bus is fully described in Section 2.6, “PCI/PCI-X Bus.”

2.3.4 PWM Controller

To assist with thermal management, in addition to the thermal measurement devices on the I^2C bus, the TICK includes status monitoring for thermal events and a PWM controller to modulate the ON time of a standard fan.

NOTE

This section applies only to systems with a fansink; it does not apply to systems shipped with passive heatsinks.

HPC II provides two headers to power the fan, as described in Table 2. Both are located near the ATX power connector.

Table 2. Fansink Power Headers

Header	Function	Description
J20	PWM power header	Fan speed controlled by PWM controller in TICK
J24	Full Speed power header	Fan powered directly by +12V (VCC_12) rail, no PWM control. (Default)

Boards are shipped with the fansink connected to J24, the full-speed power header, to prevent accidental damage to the CPU if software inadvertently modifies the PWM value (see Table 3). To use the PWM feature, simply move the fansink power cord from J24 to J20. Fans are typically modulated in the ~22 kHz region to avoid human-hearing ranges. The TICK PWM control uses the same 125 MHz/4 clock source as the reset sequence (q.v.) and produces a periodic high/low value on the FANPWM signal. Using a circulating 16-bit shift-register loaded with a 50 percent pattern, clocked at the following rate produces a 22 kHz rate

125 MHz / 4 / 710 (= ~44kHz)

Varying the digital pattern from all zeros to all ones produces a rate from 0 (always off), to 1 (always on), with a linearly interpolated speed from intermediate values. Table 3 shows representative speeds.

Table 3. PWM Values

PWM Value	Bits Set	Approximate Fan Speed	Notes
0x0000	0	0 (off)	2
0x0001	1	6%	1
0x0101	2	13%	1
0x8420	3	19%	1
0x1111	4	25%	1
0x2492	5	31%	
0x4545	6	38%	
0x5545	7	44%	
0x5555	8	50%	
0xD555	9	56%	
0xD5D5	10	63%	
0xDDD5	11	69%	
0xDDDD	12	75%	
0xFDDD	13	81%	
0xFDFD	14	88%	
0xFFFD	15	94%	
0xFFFF	16	100% (on)	

Note:

1 Speeds below 25 percent may produce audible noise and/or be ineffective in keeping the fan moving enough to provide any cooling at all, which may result in damage to the CPU. Software can determine (through temperature measurement feedback) whether PWM speeds are sufficiently fast enough.

2 If the system includes a fansink, shutting the fan off while the CPU is powered can result in damage to the CPU.

3. Low speed settings can result in overheating of the CPU, which may result in malfunction and/or damage.

Note that it is possible to choose very low fan speed settings and even disable the fan entirely using this feature. Because the CPU may malfunction or suffer damage if it overheats, the temperature of the CPU should be monitored when the PWM controller is in use.

2.3.5 System Logic Registers

The TICK contains several software-accessible registers. For details on these registers, refer to Section 4, "TICK System Logic Registers."

2.4 Local Bus

The system accesses the local bus through the HLP interface of the TSI109. Because HPC II implements some special logic and control of this bus, it deserves special attention. As shown in Figure 2, the local bus provides access to several devices:

- Boot flash memory
- Flash emulator (PromJet)
- TICK status and control registers
- NVRAM + RTC device

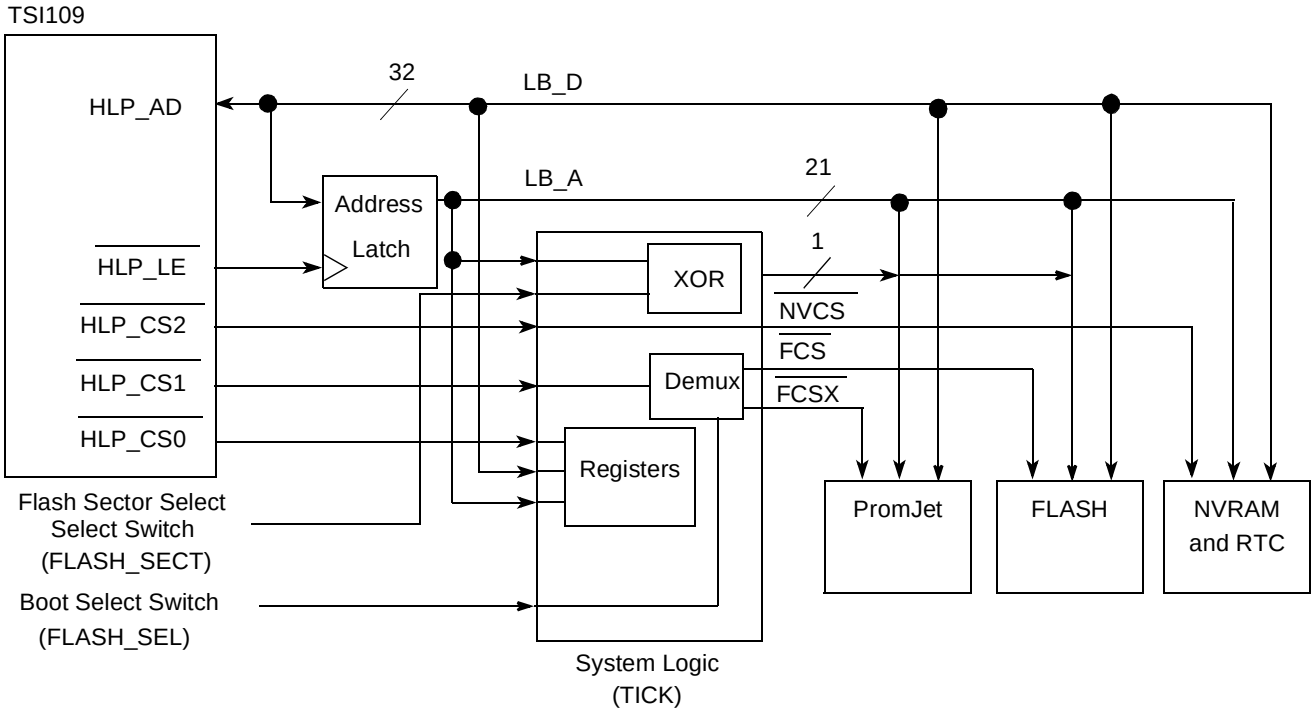


Figure 2. Host Local Port Bus Diagram

2.4.1 HLP Address Mapping

The HLP bus provides the boot code for the processor when it comes out of reset. The TSI109 always uses HLP Bank 0 ($\overline{\text{HLP\_CS0}}$) as the boot bank. However, HPC II implements two features to allow the user to choose among several options for where the CPU fetches its boot code.

First, $\overline{\text{HLP\_CS0}}$ is routed to either the flash chips or the flash emulator (PromJet) by the system logic based on switch settings. By default (FLASH_SELL switch OFF), $\overline{\text{HLP\_CS0}}$ is routed to the flash memory and the PromJet is selected by $\overline{\text{HLP\_CS3}}$; the chip selects are swapped when the FLASH_SEL switch is ON. The FPGA always responds to accesses to HLP Bank 1, and HLP Bank 2 accesses are always routed to the NVRAM+RTC chip.

Additionally, the flash space is arranged into two sectors by controlling the most significant bit of the address bus. When the FLASH_SECT switch is OFF (default), LB_A[27] is passed through the FPGA unmodified and the boot code is fetched from the lower half of the boot memory space. When the FLASH_SECT switch is ON, LB_A[27] is inverted, effectively swapping the two halves of the boot address space so that the processor fetches its boot code from the upper half of the address space. This allows the flash memory to contain two different boot sequences that the user can select using a switch setting.

Table 4. Boot Device Selection and Local Bus Address Map

FLASH_SEL	FLASH_SECT	HLP Bank	Chip Select	Destination	Address	Description
0	0	0	$\overline{\text{HLP\_CS0}}$	Flash Sector 0	0xFF0x_xxxx	Boot from lower half of flash (default)
				Flash Sector 1	0xFF8x_xxxx	
		3	$\overline{\text{HLP\_CS3}}$	PromJet	0xFExx_xxxx	
0	1	0	$\overline{\text{HLP\_CS0}}$	Flash Sector 1	0xFF0x_xxxx	Boot from upper half of flash
				Flash Sector 0	0xFF8x_xxxx	
		3	$\overline{\text{HLP\_CS3}}$	PromJet	0xFExx_xxxx	
1	X	0	$\overline{\text{HLP\_CS0}}$	PromJet	0xFFxx_xxxx	Boot from PromJet (FLASH_SECT ignored)
		3	$\overline{\text{HLP\_CS3}}$	Flash Sector 0	0xFE0x_xxxx	
				Flash Sector 1	0xFE8x_xxxx	
X	X	1	$\overline{\text{HLP\_CS1}}$	Register File	0xFDxx_xxxx	TICK internal registers
X	X	2	$\overline{\text{HLP\_CS2}}$	NVRAM + RTC	0xFCxx_xxxx	Battery-backed NVRAM and RTC

Bank 1 of the HLP interface is used to access the internal registers of the TICK. The TICK is accessed as an 8-bit device. Bank 2 of the HLP interface is used to access the battery-backed non-volatile RAM and real-time clock. This device is also an 8-bit device. The operation of these devices is not affected by any of the configuration switches, and their chip selects are simply passed through unchanged by the TICK.

Note that Table 4 shows only the local bus addresses, and is not a complete system address map. A full address map is available in the user's guide for the board support package (BSP), which is shipped with the system and is included in BSP updates downloaded from the Freescale website.

2.4.2 Byte Swapping

The TSI109 is configured to perform byte-swapping by default (that is, when the TSI109 BOOT bit is set). To preserve a consistent image of flash memory after BOOT is cleared, the software shipped with HPC II configures the look-up table (LUT) entries mapping HLP banks 0 and 3 to perform byte swapping. This configuration requires special consideration when you are creating flash driver code. For example, when you are reading factory-configured internal flash registers, keep in mind that the values read are byte-swapped.

2.5 I^2C Bus

The TSI109 provides two I^2C interfaces. One is dedicated for use by the DDR2 interface for SPD, and is considered part of that interface. The remaining I^2C bus is used on HPC II to access several peripheral devices, as summarized in Table 5.

Table 5. I²C Address Map

Device	Description	I²C Address
ISC4C02	256 x 8 serial EEPROM	1010_000
ADT7415-0	Ambient temperature monitor	1001_010
ADT7461	CPU thermal diode monitor	1001_100
MCP3021	ADC for VDD current measurement	1001_101

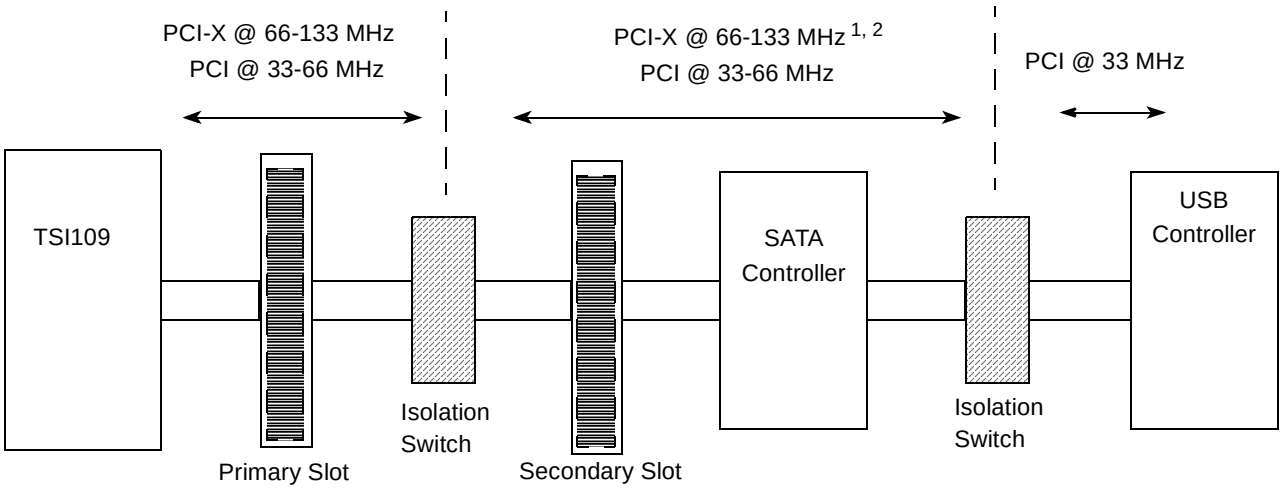
The ISC4C02 serial EEPROM performs a vital role in the system since the TSI109 must be reconfigured for 32-bit latched mode before the processor can successfully access the flash memory. After coming out of reset, the TSI109 attempts to access I²C address 0b1010_000. If a device responds with an acknowledge, it reads the boot configuration information from the I²C device to reconfigure its internal registers. If this mechanism fails or if the I²C memory is corrupted, the board does not boot correctly. For details, see Appendix A, "I²C EEPROM Programming."

NOTE

To allow for maximum flexibility, the EEPROM hardware write protection is not implemented on HPC II. Therefore, use extreme caution when writing to the EEPROM to avoid overwriting the TSI109 configuration data.

2.6 PCI/PCI-X Bus

The TSI109 provides one interface for PCI-X and PCI 2.3. This bus is divided into sections using fast FET switches to isolate unused devices that slow the bus, as shown in Figure 3. The more sections of the bus that are enabled, the slower the bus frequency. The first section contains a single PCI-X/PCI slot. When the other sections are disabled, the bus can operate as a PCI-X bus at up to 133 MHz or as a PCI bus at up to 66 MHz. The second section contains the SATA controller and a second PCI-X/PCI slot. When this section is enabled, the bus can operate in PCI or PCI-X mode at up to 133 MHz, though this may need to be reduced for stable bus operation. As a result, the bus defaults to 66 MHz in PCI-X mode; the higher frequencies can be obtained by changing a resistor option (see schematics). The third section contains the USB controller. When this third section is enabled, the bus must operate as a 33 MHz PCI bus due to the constraint imposed by the USB controller. The bus features automatic mode and speed detection, but these can be partially controlled through configuration switches.



Notes:
1. Default frequency for this segment is 66 MHz. 100-133 MHz operation are enabled by depopulating R1.
2. Maximum frequency varies with bus load and may need to be constrained to 100 MHz in PCI-X mode.

Figure 3. PCI/PCI-X Bus Diagram

The PCI bus speed is detected by the TICK from the PCIXCAP pin decoder and the M66EN pin, as well as the relevant configuration switch settings, and the configuration signals of the TSI109 are driven with the corresponding pattern, as shown in Table 6. For system flexibility, the TICK does not attempt to intelligently control the bus frequency based on the number of devices on the PCI/PCI-X bus or which sections of the bus are enabled. However, configuration switches allow the user to throttle the bus frequency if necessary. Note that the second segment of the bus (containing the secondary slot and SATA controller) defaults to 66 MHz in PCI-X mode via a resistor option on the board. Operation at 100–133 MHz is not directly configurable through switches, but the bus can be configured to operate in this mode when the second section of the bus is enabled (that is, PCI_ISO_A = 0, PCI_ISO_B = 1) when optional resistor R1 is removed (see page 36 of the schematics). The bus is constrained to PCI mode at 33 MHz when the third section of the bus is enabled (that is, PCI_ISO_A = 0, PCI_ISO_B = 0) due to the constraint imposed by the USB controller.

Table 6. PCI Speed Detection and Configuration

PCIXCAP	M66EN	PCIXC [1:0]	PCI33_FRC (SW4[7]) [1]	PCIX100_FRC (SW4[8]) [1]	Mode and Speed	108_PCIXCAP [1:0]	108_M66EN	Notes
X	X	XX	1	X	PCI 33 MHz	00	0	
Ground	0	11	0	X	PCI 33 MHz	00	0	2
Ground	1	11	0	X	PCI 66 MHz	00	1	
Pull-down	X	01	0	X	PCI-X 66 MHz	01	0	
No-connect	X	11	0	1	PCI-X 100 MHz	10	0	3

Table 6. PCI Speed Detection and Configuration

PCIXCAP	M66EN	PCIXC [1:0]	PCI33_FRC (SW4[7]) [1]	PCIX100_FRC (SW4[8]) [1]	Mode and Speed	108_PCIXCAP [1:0]	108_M66EN	Notes
No-connect	X	11	0	0	PCI-X 133 MHz	11	0	

Notes:
1. 0 = OFF, 1 = ON.
2. Due to hardware termination of the PCIXCAP and M66EN signals, this is the state when PCI_ISO_A and PCI_ISO_B switches are both 0 (OFF).
3. PCIX100_FRC = 1 (ON) may be required for stable bus operation when PCI_ISO_A = 0 (OFF) and PCI_ISO_B = 1 (ON). The TICK does not automatically reduce the bus speed based on the state of PCI_ISO_A and PCI_ISO_B.

Table 7 shows the IDSEL and INT configurations for the various devices on the bus.

Table 7. HPC II PCI Bus Information

Device	IDSEL	Interrupt Mapping			
		INTA#	INTB#	INTC#	INTD#
TSI109	AD16	0	1	2	3
Slot 1	AD17	0	1	2	3
Slot 2	AD18	1	2	3	0
SATA	AD19	2	—	—	—
USB	AD20	3	0	1	—

2.7 Disk Controller

HPC II contains a Marvell 88SX5040 SATA disk controller. Channels 0–3 are available for SATA IDE disks, operating individually or grouped into a RAID (level 0). Refer to the Marvell web site for programming information and Linux driver code.

2.8 USB Controller

HPC II contains a USB 2.0 UHCI/EHCI-compliant USB interface. Ports 0 and 1 are connected to the upper and lower stacked USB header, respectively, on the rear panel. Ports 2 and 3 are available on a standard ATX-chassis-compatible USB header.

2.9 Clocks

The TSI109 provides an integrated spread-spectrum clock generator to supply clocks to the system bus, DDR2 interface, and PCI/PCI-X bus. The TSI109 supports the following clock frequencies:

- System bus interface: 100, 133, 167, 183, 200 MHz
- DDR2 interface: 133, 166, 200, 233 MHz
- PCI/PCI-X interface:
  - PCI-X mode: 66, 100, 133 MHz
  - PCI mode: 33, 66 MHz

The TSI109 derives all of these clocks from a 33 MHz reference clock supplied by the MPC9817, which also supplies the 25 MHz reference clocks required by the SATA controller and Ethernet PHYs. The TSI109 reference clock can also be supplied externally through an SMA connector and resistor option, which is not normally populated. The TSI109 has an internal path from the clock generator to the DDR2 interface, and no outside connection (apart from the feedback timing loop) is required. The footprint for an SMA connector is provided for use of external clocking of the DDR2 interface, but the SMA connector is not populated because this debug feature is not needed for normal board builds. The MPX and PCI buses require external connections from the clock generator to the TSI109 clock input. Because HPC II requires more PCI clocks than are provided by the TSI109, an MPC96203 fanout buffer is used to drive those clocks.

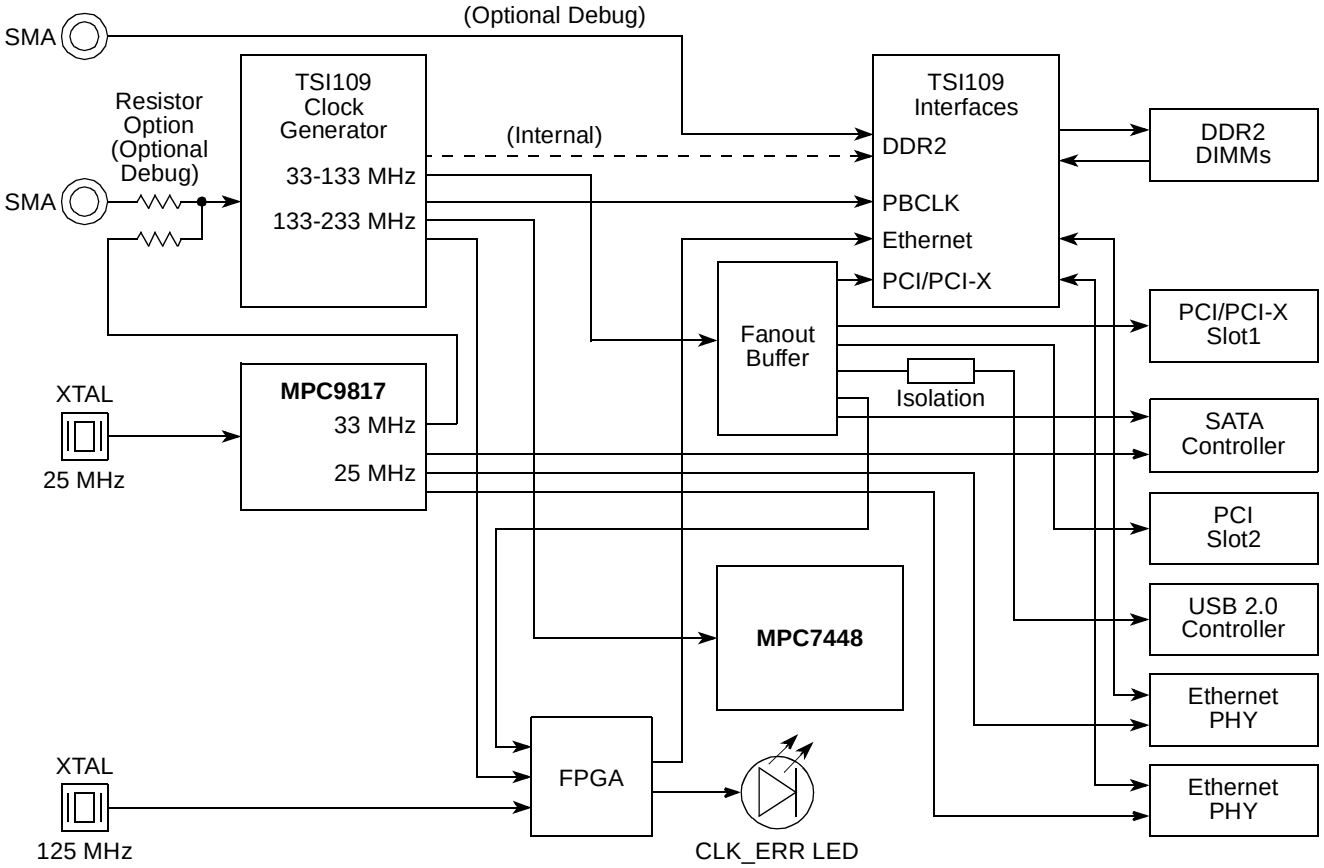


Figure 4. HPC II Clock Architecture

3 Setup and Configuration Switches

HPC II hardware configuration is set through four 8-switch DIP modules in the lower left corner of the board (with the I/O connectors on the top edge of the board). A convenient configuration guide is provided in Appendix B.

3.1 CPU Core Voltage (V_{DD}) Selection

SW1[1:5] configure the core voltage of the CPU as specified in Table 8. Note that it is possible to exceed the processor stress ratings with the higher voltage settings, and care must always be taken to select voltages supported by the processor.

Table 8. CPU Core Voltage Configuration

SW1					Output Voltage	SW1					Output Voltage
1	2	3	4	5		1	2	3	4	5	
1	1	1	1	1	0.600 V	0	1	1	1	1	1.000 V
1	1	1	1	0	0.625 V	0	1	1	1	0	1.050 V
1	1	1	0	1	0.650 V	0	1	1	0	1	1.100 V
1	1	1	0	0	0.675 V	0	1	1	0	0	1.150 V
1	1	0	1	1	0.700 V	0	1	0	1	1	1.200 V
1	1	0	1	0	0.725 V	0	1	0	1	0	1.250 V
1	1	0	0	1	0.750 V	0	1	0	0	1	1.300 V
1	1	0	0	0	0.775 V	0	1	0	0	0	1.350 V
1	0	1	1	1	0.800 V	0	0	1	1	1	1.400 V
1	0	1	1	0	0.825 V	0	0	1	1	0	1.450 V
1	0	1	0	1	0.850 V	0	0	1	0	1	1.500 V
1	0	1	0	0	0.875 V	0	0	1	0	0	1.550 V
1	0	0	1	1	0.900 V	0	0	0	1	1	1.600 V
1	0	0	1	0	0.925 V	0	0	0	1	0	1.650 V
1	0	0	0	1	0.950 V	0	0	0	0	1	1.700 V
1	0	0	0	0	0.975 V	0	0	0	0	0	1.750 V

3.2 FPGA Options (XOPT)

SW1[6:8] are currently unused by the system. The states of these switches are reflected in the TMON1 register of the TICK, and you can use them for any purpose.

3.3 CPU PLL Configuration

SW2[1–6] configure the core frequency of the CPU. The exact core frequency is determined by the states of these switches and the current bus frequency as configured by SW4[1:3]. The switches correspond to the PLL_CFG pins of the processor as shown in Table 9.

Table 9. CPU PLL_CFG pin mapping

SW2	CPU pin			Notes
	MPC7448	MPC7447A	Pin number	
1	PLL_CFG[0]	PLL_CFG[0]	B8	1
2	PLL_CFG[1]	PLL_CFG[1]	C8	1
3	PLL_CFG[2]	PLL_CFG[2]	C7	1
4	PLL_CFG[3]	PLL_CFG[3]	D7	1
5	PLL_CFG[4]	PLL_CFG[4]	A7	1
6	PLL_CFG[5]	TEST[4]	D10	1, 2

Notes:
1. 0 = OFF, 1 = ON.
2. TEST[4] must be 0 (SW1[6] must be OFF) for MPC7447A.

Note that PLL_CFG[5] is not supported for the MPC7447A. Instead, pin D10 is a factory-only test pin that must be pulled to GND for normal device operation. Therefore, SW2[6] must be OFF when an MPC7447A is populated in the system. Table 10 shows the CPU core configuration options for the MPC7448. For more information on configuring the HPC II, see Appendix B, “HPC II Configuration Guide.”

Table 10. MPC7448 Microprocessor Core Frequency Configuration

SW2[1–6]	Bus Frequency (configured Through SW4[1-3])				
	100 MHz	133 MHz	167 MHz	183 MHz	200 MHz
100000					600
101000			667	733	800
101100		667	835	917	1000
100100		733	919	1008	1100
110100	600	800	1002	1100	1200
010100	650	866	1086	1192	1300
001000	700	931	1169	1283	1400
000100	750	1000	1253	1375	1500
110000	800	1064	1336	1467	1600
011000	850	1131	1417	1558	1700
011110	900	1197	1500	1650	
011100	950	1264	1583		
101010	1000	1333	1667		
100010	1050	1397			
100110	1100	1467			
000000	1150	1533			
101110	1200	1600			

Table 10. MPC7448 Microprocessor Core Frequency Configuration (continued)

SW2[1–6]	Bus Frequency (configured Through SW4[1-3])				
	100 MHz	133 MHz	167 MHz	183 MHz	200 MHz
111110	1250	1667			
010110	1300				
111000	1350				
110010	1400				
000110	1500				
110110	1600				
000010	1700				

3.4 System Bus Mode Option

SW2[7] configures the CPU and TSI109 to use the MPX bus protocol when OFF (0), 60x bus protocol when ON (1).

Table 11. System Bus Mode Configuration Description

Switch	Setting	Description
SW2[7]	0	System bus uses MPX bus protocol (default)
	1	System bus uses 60x bus protocol
Notes: 1. 0 = OFF, 1 = ON.		

3.5 TSI109 $\overline{\text{PB\_RST}}$ Disable Option (TSI_RST_DIS)

The TSI109 features a reset output that can reset the processor. In normal operation, the TICK merges this signal with other reset sources to derive the $\overline{\text{HRESET}}$ signal for the CPU. Setting SW2[8] defeats this and prevents the TSI109 from initiating a reset or holding the CPU in reset.

Table 12. TSI109 Reset Out Disable Description

Switch	Setting	Description
SW2[8]	0	Allow TSI109 to reset CPU (default)
	1	Prevent TSI109 from causing CPU reset
Notes: 1. 0 = OFF, 1 = ON.		

3.6 Software System Option Switches (SYSOPT)

SW3[1–3] are connected to three general-purpose I/O (GPIO) pins on the TSI109. These pins have no defined function and can be used for any purpose.

Table 13. System Option Switch Descriptions

Switch	Port	Description
SW3[1]	GPIO[0]	System defined.
SW3[2]	GPIO[1]	System defined.
SW3[3]	GPIO[2]	System defined.
Notes: 1. 0 = OFF, 1 = ON.		

3.7 Boot Flash Sector Select Option (FLASH_SECT)

SW3[4] is used to swap the top and bottom half of the flash memory space when flash is the boot device (that is, FLASH_SEL = 0, see Section 3.11, “Boot Device Selection Option”). This allows two different boot images to reside in flash memory, and you can select which to use by the setting this switch. For more information, see Section 2.4, “Local Bus.”

Table 14. Flash Sector Select (FLASH_SECT) Description

Switch	Setting	Description
SW3[4]	0	Flash memory space is not swapped (default). CPU boots from Sector 0.
	1	The top and bottom halves of flash memory are swapped. CPU boots from Sector 1
Notes: 1. 0 = OFF, 1 = ON.		

3.8 PCI Bus Isolation Switch A (PCI_ISO_A)

SW3[5] is used to disconnect all PCI devices except Slot 1 from the bus to allow high-frequency operation by limiting the trace lengths and amount of loading on the bus. Note that this switch takes precedence over PCI_ISO_B (see Section 3.9, “PCI Bus Isolation Switch B (PCI_ISO_B)”). See Section 2.6, “PCI/PCI-X Bus.”

Table 15. PCI Bus Isolation Switch A (PCI_ISO_A) Description

Switch	Setting	Description
SW3[5]	0	Slot 2 and SATA are connected to PCI/PCI-X bus; USB connected if PCI_ISO_B = 0.
	1	Only Slot 1 is connected to PCI/PCI-X bus; Slot 2, SATA, and USB are disconnected.
Notes: 1. 0 = OFF, 1 = ON.		

3.9 PCI Bus Isolation Switch B (PCI_ISO_B)

SW3[5] is used to disconnect the USB controller the bus to allow high-frequency operation by removing the USB device, which is a 33 MHz PCI device, from the bus. Note that this switch has no function when PCI_ISO_A = 1 (see Section 3.8, “PCI Bus Isolation Switch A (PCI_ISO_A)”). See Section 2.6, “PCI/PCI-X Bus.”

Table 16. PCI Bus Isolation Switch B (PCI_ISO_B) Description

Switch	Setting	Description
SW3[6]	0	USB connected to bus and bus must operate in PCI mode at 33 MHz (if PCI_ISO_A = 0).
	1	USB is disconnected from bus.
Notes: 1. 0 = OFF, 1 = ON.		

3.10 Flash Write Protection Option

SW3[7] is used to write-protect the flash memory.

Table 17. PCI Bus Isolation Switch B (PCI_ISO_B) Description

Switch	Setting	Description
SW3[7]	0	Flash is write-protected.
	1	Flash is not write-protected.
Notes: 1. 0 = OFF, 1 = ON.		

3.11 Boot Device Selection Option

SW3[8] selects which device is connected to HLP Bank 0 of the TSI109 and therefore the device to provide boot code to the CPU.

Table 18. PCI Bus Isolation Switch B (PCI_ISO_B) Description

Switch	Setting	Description
SW3[8]	0	CPU boots from flash memory.
	1	CPU boots from the flash emulator (PromJet).
Notes: 1. 0 = OFF, 1 = ON.		

3.12 TSI109 System Clock Generator Configuration

SW4[1–3] configure the system clock frequency generated by the TSI109. The connections to the TSI109 pins are as listed in Table 19. For more information on configuring the TSI109 clock generator, see Appendix B, “HPC II Configuration Guide.

Table 19. System Bus Clock Frequency Select Pin Connectivity

SW4	TSI109		Notes
	Pin Name	Pin Number	
1	CG_PB_SELECT[2]	H29	1
2	CG_PB_SELECT[1]	K32	1

Table 19. System Bus Clock Frequency Select Pin Connectivity

SW4	TSI109		Notes
	Pin Name	Pin Number	
3	CG_PB_SELECT[0]	J31	1
Notes: 1. 0 = OFF, 1 = ON.			

3.13 TSI109 DDR2 Clock Generator Configuration

SW4[4–6] configure the DDR2 clock frequency generated by the TSI109. The connections to the TSI109 pins are as listed in Table 20. For more information on configuring the TSI109 clock generator, see the configuration guide in Appendix B.

Table 20. System Bus Clock Frequency Select Pin Connectivity

SW4	TSI109		Notes
	Pin Name	Pin Number	
4	CG_SD_SELECT[2]	H28	1
5	CG_SD_SELECT[1]	G32	1
6	CG_SD_SELECT[0]	G29	1
Notes: 1. 0 = OFF, 1 = ON.			

3.14 Force 33 MHz PCI Mode Option (PCI33_FRC)

SW4[7] can be used to force the PCI/PCI-X bus to operate in PCI mode at 33 MHz. Note that this overrides all other considerations, including speed and mode detection. This option is normally used only for debug.

Table 21. PCI Bus Mode Limiting Option

Switch	Setting	Description
SW4[7]	0	PCI/PCI-X bus operates normally (default).
	1	PCI/PCI-X bus operates in PCI mode at 33 MHz.
Notes: 1. 0 = OFF, 1 = ON.		

3.15 Force 100 MHz PCI-X Option (PCIX100_FRC)

SW4[8] can be used to constrain the PCI/PCI-X bus to operate at 100 MHz when 133 MHz would normally be selected. Note that this has no effect if the bus is in PCI mode or if the detection circuit indicates PCI-X 66 MHz. This option may be necessary if any devices are present in Slot 1 or 2.

Table 22. PCI Bus Mode Limiting Option

Switch	Setting	Description
SW4[8]	0	PCI/PCI-X bus operates normally (default).
	1	PCI/PCI-X bus frequency is limited to 100 MHz in PCI-X mode.
Notes: 1. 0 = OFF, 1 = ON.		

4 TICK System Logic Registers

The TICK device contains several software-accessible registers. Table 23 shows the register address map of the TICK device and indicates the page on which each is discussed.

Table 23. TICK Address Map

Base Address Offset	Register	Access	Reset	Section/Page
0x00	System ID register (TID)	R	15 (0x0F)	Section 4.1/Page 20
0x04	System version register (TVER)	R	0x42	Section 4.2/Page 21
0x08	General control/status register (TSCR)	R/W	0x00	Section 4.3/Page 21
0x0C	Reset control register (TRCR)	R/W	0x00	Section 4.4/Page 22
0x10	Power control register (TPWR)	R/W	0x00	Section 4.5/Page 23
0x14	PCI status register (TPCI)	R	*varies*	Section 4.6/Page 24
0x18	Debug options register (TDOR)	R/W	*varies*	
0x1C	LED data register (TLED)	R/W	0x00	Section 4.7/Page 25
0x30	PWM Low Pattern (TPWML)	R/W	0x00	Section 4.8/Page 25
0x34	PWM High Pattern (TPWMH)	R/W	0x00	Section 4.9/Page 26
0x40	Interrupt Control/Status Register (TISR)	R/W	0x80	Section 4.10/Page 26
0x44	Taiga Monitor and Debug Register (TMON1)	R/W	*varies*	Section 4.11/Page 27
all others	*reserved*	*reserved*	*undefined*	

4.1 ID Register (TID)

TID contains a unique classification ID number used by DINK/eDINK and other software to identify board types dynamically.

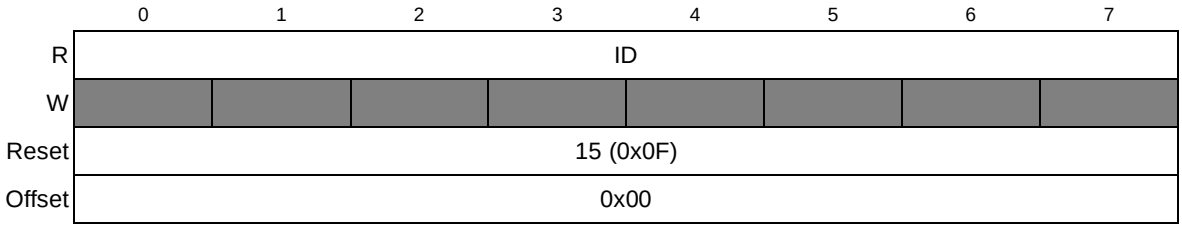


Figure 5. ID Register (FS_ID)

Table 24. FS_ID Field Descriptions

Bits	Name	Description
0–7	ID	Board identification

4.2 Version Register (TVER)

TVER contains board and revision information.

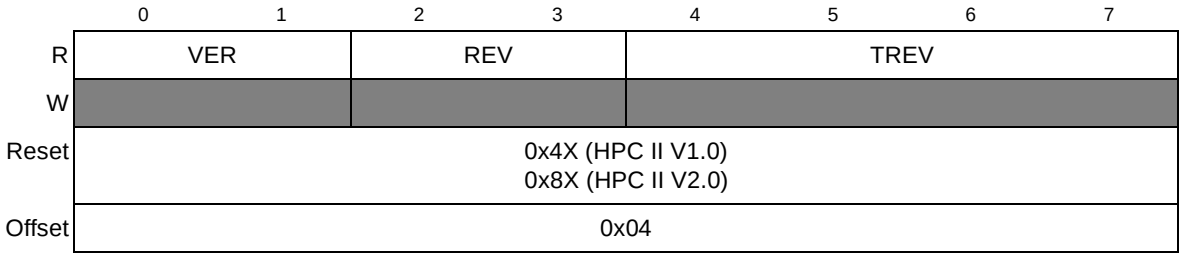


Figure 6. Version Register (FS_VER)

Table 25. TVER Field Descriptions

Bits	Name	Description
0–1	VER	Version Number: %01: V1 %10: V2 %11: *reserved* %00: *reserved*
2–3	REV	Revision Number (starts with 0)
4–7	TREV	TICK Revision Number (starts with 0)

4.3 General Status/Control Register (TSCR)

TSCR contains various control and status fields.

	0	1	2	3	4	5	6	7
R	LOCK	POE	RSTE	NOFAULT	—			LED
W								
Reset	0	0	0	0	0	0	0	0
Offset	0x08							

Figure 7. General Control/Status Register (TSCR)

Table 26. TSCR Field Descriptions

Bits	Name	Description
0	LOCK	If this bit is set, the following TICK registers become protected and are not writable: TSCR TRCR TPWR All others remain writable. Because TSCR is included in this set, LOCK cannot be disabled when set (except for system reset).
1	POE	PowerOff Enable. If set, the TPWR[PWROFF] bit can be asserted to turn off the system power.
2	RSTE	Setting this bit enables the TSCR[BRDRST] bit, allowing software to initiate a board reset. (TICK Rev 4+ only.)
	—	*-reserved-* (TICK Rev 0-3)
3	NOFAULT	Self-fault. Set this bit if no faults are found with TICK (this is part of the light path diagnostics).
4-6	—	Reserved; read as ‘0’
7	LED	If set, the internal LED buffers are driven by the contents of the FS_LEDCTL register; if clear (default), the contents are driven by various activities.

4.4 Reset Control Register (TRCR)

TRCR contains enable and assertion bits for reset controls.

	0	1	2	3	4	5	6	7
R	PBRSTDIS	PHYRST	—		MEMRST	—	BRDRST	SRESET
W								
Reset	X	0	0	0	0	0	0	0
Offset	0x0C							

Figure 8. Reset Control Register (TRCR)

Table 27. TRCR Field Descriptions

Bits	Name	Description
0	PBRSTDIS	This bit is set if the TSI_RST_DIS switch is set, inhibiting the PB_RST output of the TSI109 from causing HRESET assertion to the CPU (see Section 3.5, "TSI109 PB_RST Disable Option (TSI_RST_DIS)").
1	PHYRST	If set, causes the HPC II Ethernet PHYs (the Marvell 88E1111 devices) to be reset. Software must clear the bit to release the device from reset.
2	—	*Reserved*
3	—	*Reserved*
4	MEMRST	If set, causes the HPC II DDR DIMMs to be reset (not all DIMMs support reset). Software must clear the bit to release the device from reset.
5	—	*Reserved*
6	BRDRST	Setting this bit causes a board reset if TSCR[RSTE] is set. (TICK Rev 4+)
	—	*Reserved* (TICK Rev 0–3)
7	SRESET	If set, causes the TICK to assert SRESET to the processor. Note that SRESET is a self-resetting bit.

4.5 Power Control/Status Register (TPWR)

TPWR contains information, enables, and assertion bits for power/thermal management. Because special care must be exercised when using hardware control of the DFS modes, the TICK requires several bits to be changed before DFS modes can be enabled through hardware. First, the DFSEN bit prevents the TICK from driving the DFS2 and DFS4 pins when cleared, and must be set to allow hardware control of these signals. If DFSEN is cleared, the states of THROTTLE, ADFS2, ADFS4, DDFS2, and DDFS4 are ignored. If DFSEN is set, the THROTTLE bit determines whether the DDFS2 and DDFS4 pins are immediately driven to reflect the states of the DDFS2 and DDFS4 bits (THROTTLE = 0) or are driven to reflect the states of the ADFS4 and ADFS4 bits when a over-temperature condition exists (THROTTLE = 1 and OALARM = 0). ADFS2, ADFS4, DDFS2, and DDFS4 default at reset to '1' to ensure that accidentally setting the DFSEN bit does not enable DFS mode unintentionally or inadvertently disable software control of DFS modes through the internal registers of the MPC7448. (Driving both the DFS2 and DFS4 input pins of the MPC7448 low completely disables DFS mode, including software control via through the processor internal registers.)

	0	1	2	3	4	5	6	7
R	OALARM	THROTTLE	ADFS2	ADFS4	DFSEN	DDFS2	DDFS4	PWROFF
W								
Reset	1	0	1	1	0	1	1	0
Offset	0x10							

Figure 9. Reset Control Register (TPWR)

Table 28. TPWR Field Descriptions

Bits	Name	Description
0	$\overline{\text{OALARM}}$	$\overline{\text{The}}$ thermal over-temperature status signal from the processor temperature measurement monitor. $\overline{\text{OALARM}}$ is asserted until the programmed threshold is no longer exceeded. Note that this bit is a duplicate of the TISR[TALARM].
1	THROTTLE	If set, enables automatic reduction in the speed of the MPC7448 processor when temperature limits are exceeded. If $\overline{\text{OALARM}}$ is asserted, the setting in $\overline{\text{ADFS2}}$ and $\overline{\text{ADFS4}}$ are forced onto the DFS signals to the MPC7448. If THROTTLE is clear, the DFS pins are controlled by the DFS register bits when DFSEN is set. If DFSEN is not set, the DFS settings are entirely determined by external hardware.
2	$\overline{\text{ADFS2}}$	With $\overline{\text{ADFS4}}$, controls the DFS modes of the MPC7448 when automatic control of DFS is enabled through the THROTTLE bit. When the THROTTLE bit is set and an over-temperature condition is set, the state of this bit is driven on the MPC7448 $\overline{\text{DFS2}}$ pin. This bit name is written as active low to reflect that the DFS pin it controls is an active low input.
3	$\overline{\text{ADFS4}}$	With $\overline{\text{ADFS2}}$, controls the DFS modes of the MPC7448 when automatic control of DFS is enabled through the THROTTLE bit. When the THROTTLE bit is set and an over-temperature condition is set., the state of this bit is driven on the MPC7448 $\overline{\text{DFS4}}$ pin. This bit name is written as active low to reflect that the DFS pin it controls is an active low input.
4	DFSEN	If enabled, allows the $\overline{\text{DFS2}}$ and $\overline{\text{DFS4}}$ pins to be driven low; otherwise, the pins remain driven high. Because these signals are TEST[0:1] on the MPC7447A and should not be driven low, this bit should never be set in an MPC7447A system.
5	$\overline{\text{DDFS2}}$	Directly controls the $\overline{\text{DFS2}}$ pin of the MPC7448 when DFSEN is set and THROTTLE is cleared; it is reserved and should not be changed on the MPC7447A. This bit name is written as active low to reflect that the DFS pin it controls is an active low input.
6	$\overline{\text{DDFS4}}$	Directly controls the $\overline{\text{DFS4}}$ pin of the MPC7448 when DFSEN is set and THROTTLE is cleared; it is reserved and should not be changed on the MPC7447A. This bit name is written as active low to reflect that the DFS pin it controls is an active low input.
7	$\overline{\text{PWROFF}}$	Allows control of the system power. If the TSCR[POE] bit is set to enable it, the following sequence turns off the power: PWROFF = 1 Delay(10us) PWROFF = 0

4.6 PCI Bus Status Register (TPCI)

TPCI monitors the PCI Bus environment. Note that PCI-X mode at 100 MHz implies that the PCIX100FRC switch is set (see Section 3.15, “Force 100 MHz PCI-X Option (PCIX100_FRC)).

	0	1	2	3	4	5	6	7
R	$\overline{\text{SLOT1}}$	$\overline{\text{SLOT2}}$	ISOA	ISOB	PFORCE	PCIX	PSPEED	
W								
Reset	X	X	X	X	X	X	X	X
Offset	0x14							

Figure 10. PCI Status Register (FS_PCI0)

Table 29. TPCI Field Descriptions

Bits	Name	Description
0	$\overline{\text{SLOT1}}$	If set, slot 1 of PCI bus is occupied.
1	$\overline{\text{SLOT2}}$	If set, slot 2 of PCI bus is occupied.
2	ISOA	Set if PCI_ISO_A switch is ON, disconnecting all devices except Slot 1.
3	ISOB	Set if PCI_ISO_B switch is ON, disconnecting USB controller.
4	PFORCE	If set, the PCI bus was forced into PCI-33 mode.
5	PCIX	If set, the PCI bus is in PCI-X mode; otherwise, it is in conventional PCI 2.3 mode.
6–7	PSPEED	PSPEED indicates the detected PCI bus speed, as follows: 00 33 MHz 01 66 MHz 10 100 MHz 11 133 MHz

4.7 LED Data Register

The LED data register can be used to directly control the HPC II monitoring LEDs (for software message purposes, as an example). Direct control of LEDs 1–7 is possible only when TSCR[LED] is set, but LED8 has no predefined function and is dedicated to software use. Therefore, LED8 is not protected by TSCR[LED] and software can use it any time.

	0	1	2	3	4	5	6	7
R	LED							
W								
Reset	0	0	0	0	0	0	0	0
Offset	0x1C							

Figure 11. LED Control Register (TLED)

Table 30. TLED Field Descriptions

Bits	Name	Description
0–6	LED1–7	Corresponding values for monitoring LEDs L1–L7. Setting a bit illuminates the LED if TSCR[LED] is set.
7	LED8	Setting this bit illuminates LED8. This LED is not protected by TSCR[LED] and software can use it at any time.

4.8 PWM Low Data Register (TPWML)

TPWML contains the lower 8 bits of the 16-bit PWM shift register. Writing this register causes the PWM signal to be updated.

	0	1	2	3	4	5	6	7
R	PWML							
W								
Reset	0x00 (TICK Rev 0-3) 0xFF(TICK Rev 4+)							
Offset	0x30							

Figure 12. PWML Control Register (TPWML)

Table 31. TPWML Field Descriptions

Bits	Name	Description
0–7	PWML	Lower 8 bits of PWM waveform.

4.9 PWM High Data Register (TPWMH)

TPWMH contains the higher 8 bits of the 16-bit PWM shift register. Writing this register causes the PWM signal to be updated

	0	1	2	3	4	5	6	7
R	PWMH							
W								
Reset	0x00 (TICK Rev 0-3) 0xFF(TICK Rev 4+)							
Offset	0x34							

Figure 13. PWMH Control Register (TPWMH)

Table 32. TPWMH Field Descriptions

Bits	Name	Description
0–7	PWML	Upper 8 bits of PWM waveform.

4.10 INT Control/Status Register (TISR)

TISR contains interrupt masking and routing.

	0	1	2	3	4	5	6	7
R	$\overline{\text{TALARM}}$	$\overline{\text{TALERT}}$	TINT0	AINT0	TINT1	AINT1	SINT0	SINT1
W								
Reset	X	X	0	0	0	0	0	0
Offset	0x40							

Figure 14. PWMH Control Register (TISR)

Table 33. TISR Field Descriptions

Bits	Name	Description
0	TALARM	Reflects the state of the ADT7461 THERM output. ‘0’ indicates the device has asserted its THERM output, indicating an over-temperature condition has been detected at the CPU.
1	TALERT	Reflects the state of the ADT7461 ALERT output. ‘0’ indicates the device has asserted its ALERT output. This signal assertion can have multiple causes and will be system dependent.
2	TINT0	If set, the THERM output of the temperature monitor is allowed to assert an interrupt through the XINT0 pin.
3	AINT0	If set, the ALERT output from the temperature monitor is allowed to assert an interrupt through the XINT0 pin.
4	TINT1	If set, the THERM output l from the temperature monitor is allowed to assert an interrupt through the XINT1 pin.
5	AINT1	If set, the ALERT output from the temperature monitor is allowed to assert an interrupt through the XINT1 pin.
6	SINT0	If set, the “SERVICE” push button asserts XINT0 to the TSI109; otherwise, the push button asserts SRESET.
7	SINT1	If set, the “SERVICE” push button asserts XINT1 to the TSI109; otherwise, the push button asserts SRESET.

4.11 Monitor and Debug Register 1 (TMON1)

TMON1 shows the current status of the XOPT and TSI_RST_DIS switches and allows software to force assertion of the XINT0 and XINT1 pins.

	0	1	2	3	4	5	6	7
R	XOPT0	XOPT1	XOPT2	FLASH_SEL	FLASH_SECT	FXINTEN	FXINT0	FXINT1‘
W								
Reset	X	X	X	X	X	0	0	0
Offset	0x44							

Figure 15. MON1 Control Register (TMON1)

Table 34. TMON1 Field Descriptions

Bits	Name	Description
0–2	XOPT(0:2)	Reflects status of XOPT switches.
3	FLASH_SEL	Reflects the state of the FLASH_SEL configuration switch. (TICK Rev 3+)
	—	*Reserved* (TICK Rev 0–2)
4	FLASH_SECT	Reflects the state of the FLASH_SECT configuration switch. Note that FLASH_SECT is ignored by the hardware when FLASH_SEL = 1. (TICK Rev 3+)
	—	*Reserved* (TICK Rev 0–2)

Table 34. TMON1 Field Descriptions

Bits	Name	Description
5	FXINTEN	Setting this bit allows FXINT0 and FXINT1 to assert the XINT0 and XINT1 pins. This does not affect other sources that may assert these pins.
6	FXINT0	Setting this bit causes the TICK to assert $\overline{\text{XINT0}}$ to the TSI109 if FXINTEN is set. Software must clear this bit after setting it. (TICK Rev 3+)
	—	*Reserved* (TICK Rev 0–2)
7	FXINT1	Setting this bit causes the TICK to assert $\overline{\text{XINT1}}$ to the TSI109 if FXINTEN is set. Software must clear this bit after setting it. (TICK Rev 3+)
	—	*Reserved* (TICK Rev 0–2)

5 Document Revision History

Table 35. Revision History

Revision	Date	Significant Changes
0	2May05	Initial draft
1	9Jun05	Updated to reflect changes in TICK.
1.1	7Jul05	Minor editorial changes.
		Added Section 4.4.2 and Appendix A.
2	8/2007	Updated document to reflect migration to TSI109. Added Table 2. (Clarification only, no change in design or functionality.) Added Table 10. (Clarification only, no change in design or functionality.) Added Table 34 to Appendix A to document configuration EEPROM image for TSI109. Added Section 2.5. . (Clarification only, no change in design or functionality.)

Appendix A
I²C EEPROM Programming

Table 36 provides the code image programmed into the I²C EEPROM on HPC II to configure the TSI109 correctly at boot. Table 37 provides the code image programmed into the I²C EEPROM on HPC II to configure the TSI108 correctly at boot. Note that the TSI109 requires an additional register write to configure the processor (MPX) bus correctly.

Table 36. I2C EEPROM Code Image for TSI109

Address	Data
Size Packet = 5 CFG Writes	
01	05
02	FF
03	FF
04	FF
05	FF
06	FF
07	FF
HLP_B0_ADDR = 0000_0000	
08	00
09	00
0A	00
0B	00
0C	00
0D	00
0E	00
0F	00
HLP_B0_MASK = FFF0_0000	
10	00
11	00
12	00
13	04
14	FF
15	00
16	00
17	00

Table 36. I2C EEPROM Code Image for TSI109

Address	Data
HLP_B0_CTRL0 = 3FFC_44C2	
18	00
19	00
1A	00
1B	08
1C	3F
1D	FC
1E	44
1F	32
HLP_B0_CTRL1 = 7C0F_2000	
20	00
21	00
22	00
23	0C
24	7C
25	0F
26	20
27	00
PB_RSR = 0000_0108	
28	00
29	00
2A	30
2B	04
2C	00
2D	00
2E	01
2F	08

Table 37. I2C EEPROM Code Image for TSI108

Address	Data
Size Packet = 4 CFG Writes	
01	04
02	FF
03	FF
04	FF
05	FF
06	FF
07	FF
HLP_B0_ADDR = 0000_0000	
08	00
09	00
0A	00
0B	00
0C	00
0D	00
0E	00
0F	00
HLP_B0_MASK = FFF0_0000	
10	00
11	00
12	00
13	04
14	FF
15	00
16	00
17	00
HLP_B0_CTRL0 = 3FFC_44C2	
18	00
19	00
1A	00
1B	08
1C	3F
1D	FC

Table 37. I2C EEPROM Code Image for TSI108 (continued)

Address	Data
1E	44
1F	32
HLP_B0_CTRL1_7C0F_2000	
20	00
21	00
22	00
23	0C
24	7C
25	0F
26	20
27	00

Appendix B
HPC II Configuration Guide

The following page provides a quick reference guide for configuring the HPC II board. Highlighted entries indicate default settings. In some cases, only switch settings considered most useful are displayed. For a complete list of available settings, see Section 3, “Setup and Configuration Switches.”

NOTE

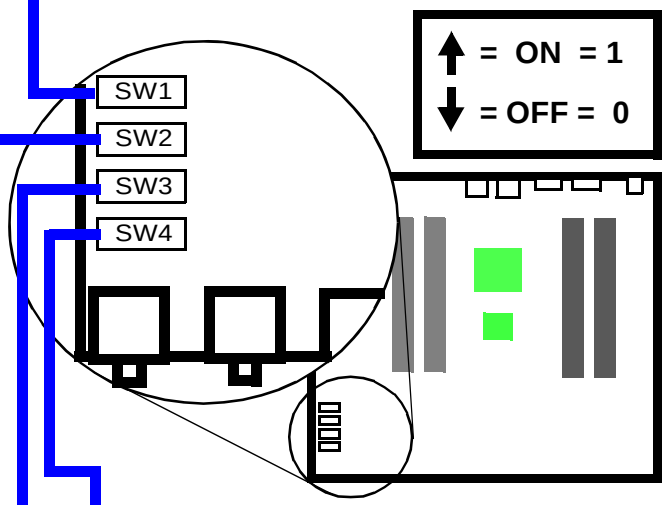
Use caution when changing switch settings. Some settings for CPU core voltage, CPU PLL, and system bus frequency may exceed device specifications, causing improper operation and/or device damage. For details, see the device hardware specifications.

Processor Core Voltage

SW1					Core Voltage	Comment
1	2	3	4	5		
0	1	1	1	1	1.000 V	
0	1	1	0	1	1.100 V	
0	1	0	1	1	1.200 V	
0	1	0	0	1	1.300 V	

SW1[6-8]: Optional Use

SW1	Name	Comment
6	XOPT0	Not presently used by system but values reflected in TICK
7	XOPT1	
8	XOPT2	



SW2[1-6]: CPU Core Frequency

SW2						CPU Core Frequency (MHz)				Ratio	Comment
						Bus Frequency (MHz)					
1	2	3	4	5	6	100	133	167	200		
1	0	1	1	0	0	500	667	833	1000	5x	
1	0	0	1	0	0	550	733	917	1100	5.5x	
1	1	0	1	0	0	600	800	1000	1200	6x	
0	1	0	1	0	0	650	866	1083	1300	6.5x	
0	0	1	0	0	0	700	930	1167	1400	7x	
0	0	0	1	0	0	750	1000	1250	1500	7.5x	
1	1	0	0	0	0	800	1066	1333	1600	8x	
0	1	1	0	0	0	850	1333	1417	1700	8.5x	
0	1	1	1	1	0	900	1200	1500	1800	9x	

Note: This table shows only a subset of available frequency options; see the CPU hardware specifications for more information..

SW2[7-8]: Bus Protocol and CPU Reset Option

SW2	Name	Set	Description
7	MPX_BUS	0	System bus uses MPX bus protocol
		1	System bus uses 60x bus protocol
8	TSI_RST_DIS	0	TSI108 can cause CPU reset
		1	TSI108 cannot cause CPU reset

SW3: System Options

SW3	Name	Set	Description
1-3	SYSOPT[0:2]	X	Connected to GPIO[0:2] on TSI108
4	FLASH_SECT	0	CPU boots from low half of flash (U-boot)
		1	CPU boots from high half of flash (DINK)
5	PCI_ISO_A	0	SATA and Slot 2 connected to PCI bus
		1	Only Slot 1 connected to PCI bus
6	PCI_ISO_B	0	USB connected to PCI bus
		1	USB disconnected from PCI bus
7	FLASH_WP	0	Flash is write-protected
		1	Flash in NOT write-protected
8	FLASH_SEL	0	CPU will boot from flash
		1	CPU will boot from PromJet

SW4[1-3]:System Bus Frequency

SW4			Bus Frequency (MHz)	Comment
1	2	3		
0	1	0	183	
0	1	1	100	
1	0	0	133	
1	0	1	166	MPC7447A
1	1	0	200	MPC7448
all others			*reserved*	

SW4[4-6]:DDR2 SDRAM Frequency

SW4			Bus Frequency (MHz)	Comment
4	5	6		
0	0	0	EXT	external clk
0	1	1	SYSCLK	sync w/ bus
1	0	0	133	
1	0	1	166	
1	1	0	200	
all others			*reserved*	

SW4[7-8]: PCI/PCI-X frequency control

SW1	Setting	Comment
7	0	PCI/PCI-X bus operates normally
	1	PCI bus forced to PCI-33 mode
8	0	PCI-X mode at 133 MHz allowed
	1	PCI-X mode limited to 100 MHz

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