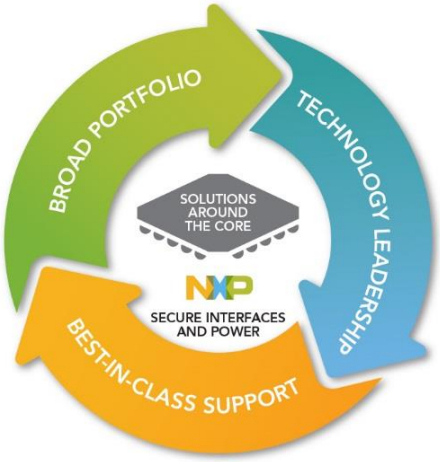
NXP RELEASES NEW VOLTAGE LEVEL TRANSLATORS – NEXT GENERATION OF INNOVATION IMPROVES SYSTEM PERFORMANCE



SECURE CONNECTIONS FOR A SMARTER WORLD

Featured Speakers:

Steve Blozis
Global Product Marketing Manager
BU Secure Interfaces and Power,
High-Performance Analog

Emmanuel Nana
Technical Marketing Manager
BU Secure Interfaces and Power

WHAT IS LEVEL TRANSLATION AND WHY IT'S SO ESSENTIAL?

Level Translators Applications

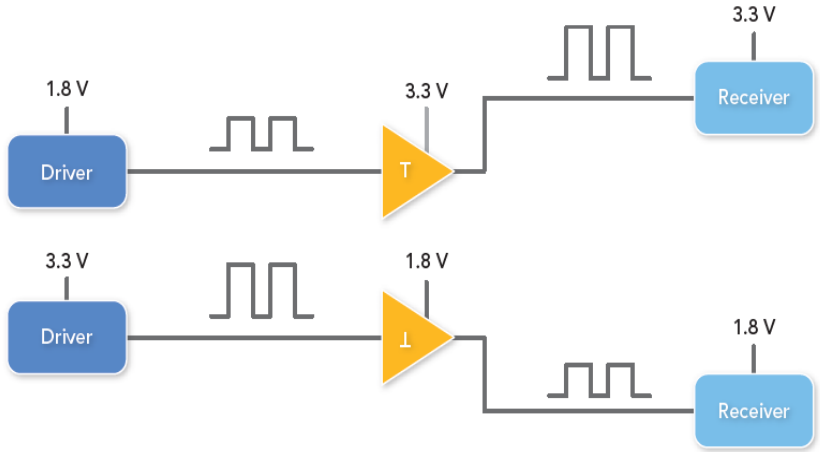


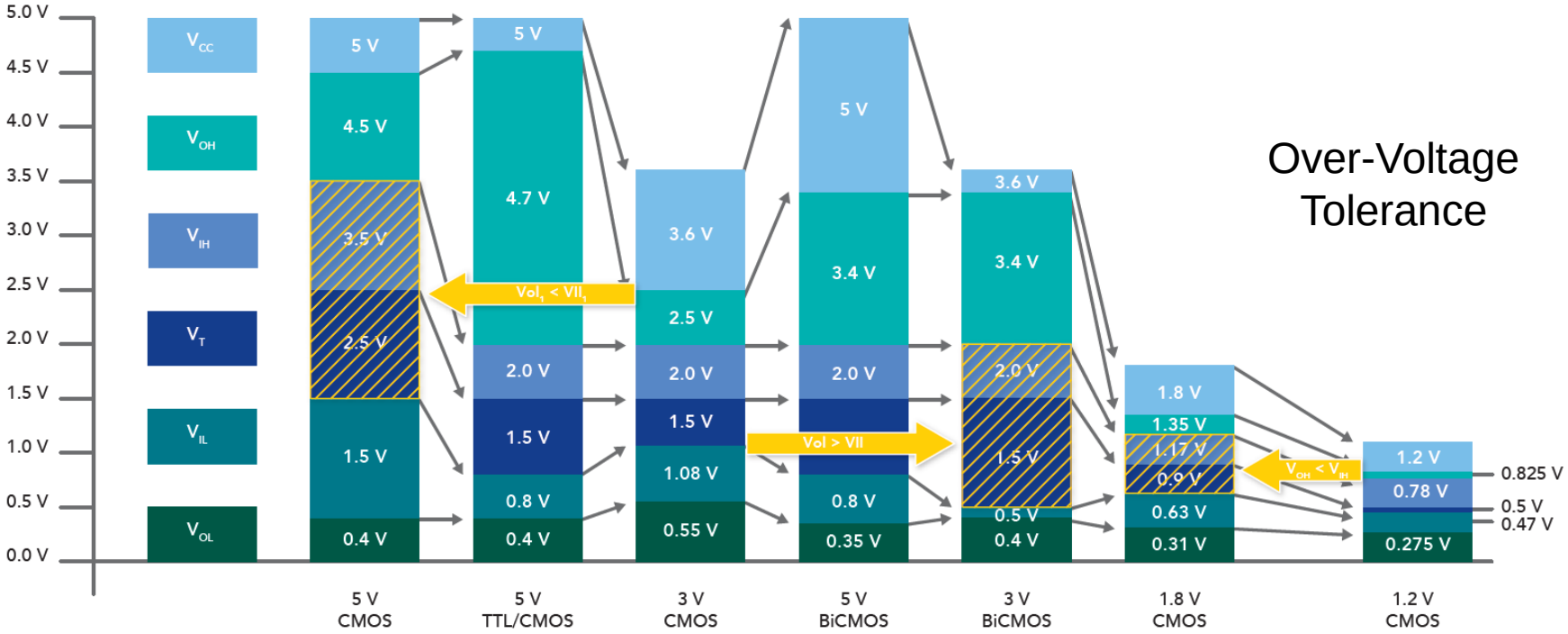
Figure 1-2. Shifting the output voltage level up or down

A quick overview

In most mixed-voltage designs, the output voltage level of a driver device needs to be shifted up or down so that the receiver device can interpret it correctly, or vice versa (Figure 1-2).

There are often variations in the logic switching input (V_{IH} and V_{IL}) and the output levels (V_{OH} and V_{OL}) for commonly used logic devices in the range of 3 and 5 V (Figure 1-3).

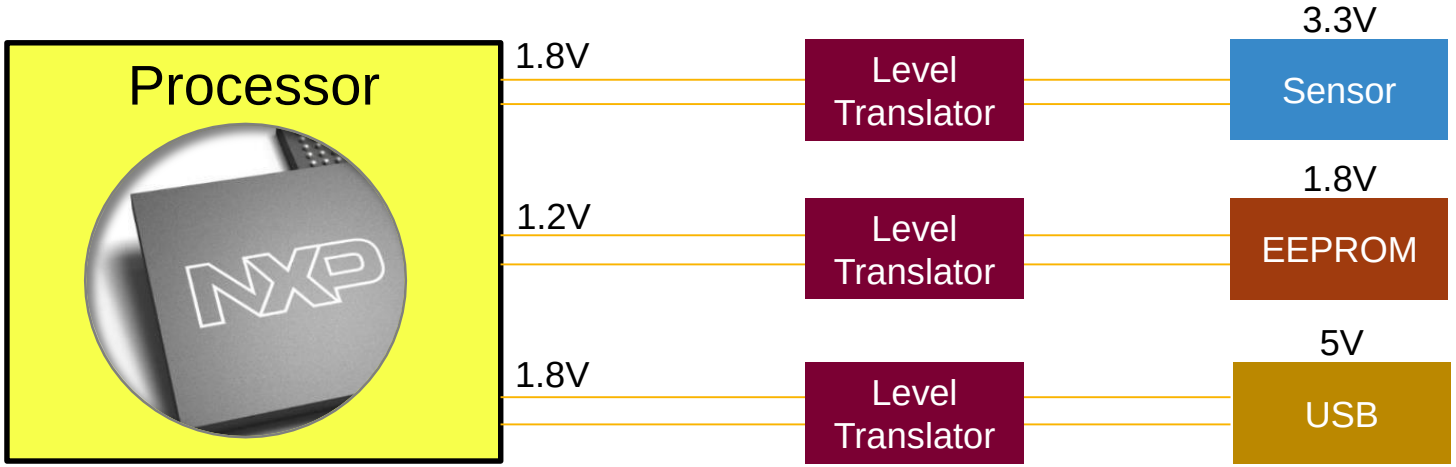
Level Translators Applications



Over-Voltage Tolerance

Trend: Digital IC's Driving for Lower Voltages & Lower Power

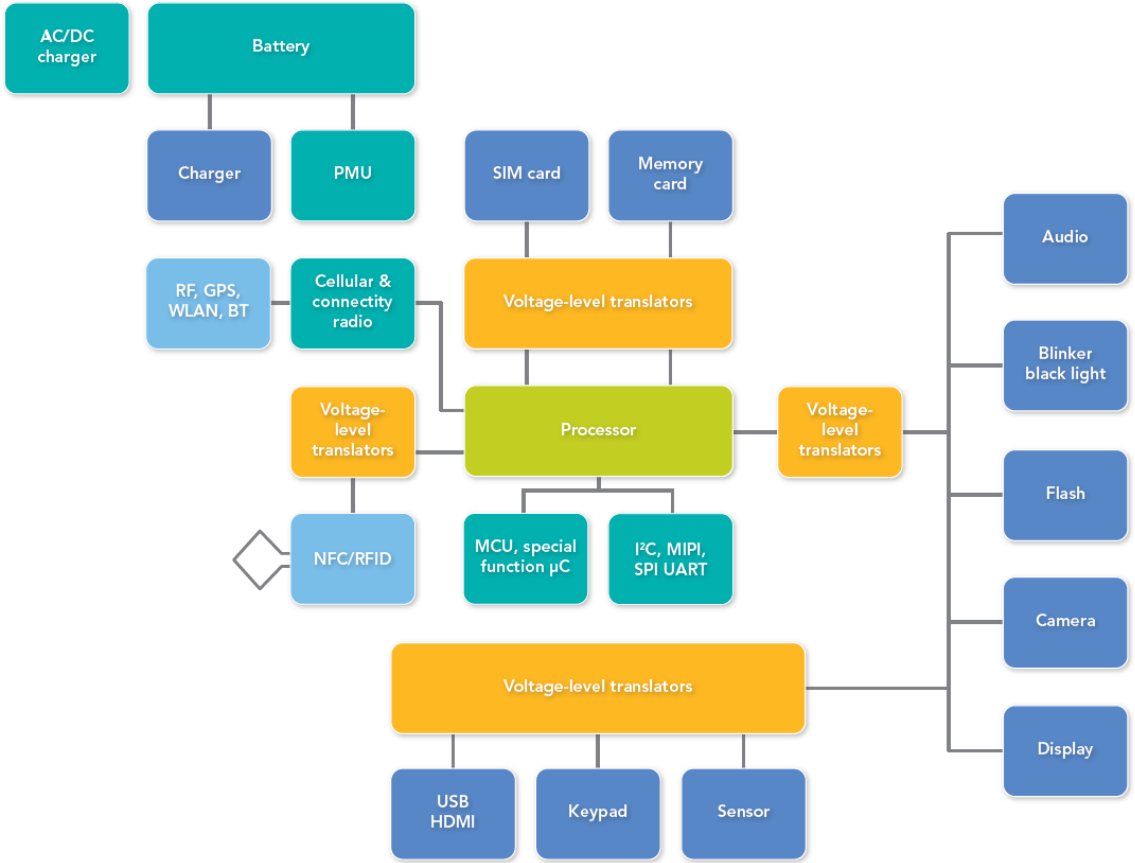
Result: More opportunities for Level Translators; peripherals aren't changing as quickly



Geometry	I/O Voltages
40nm	5V
28nm	3V
14nm	1.8V
10nm	1.2V
7nm	

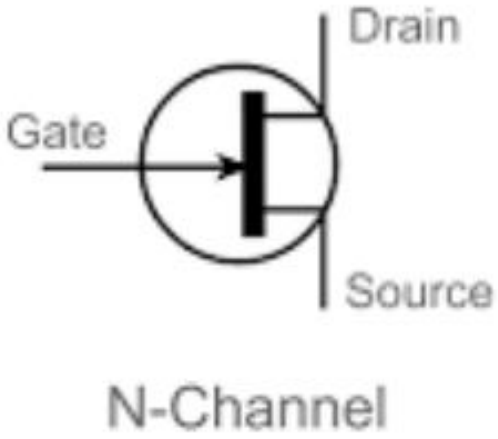
Level Translators are needed to support new lower voltage nodes to interface into legacy higher voltage nodes.

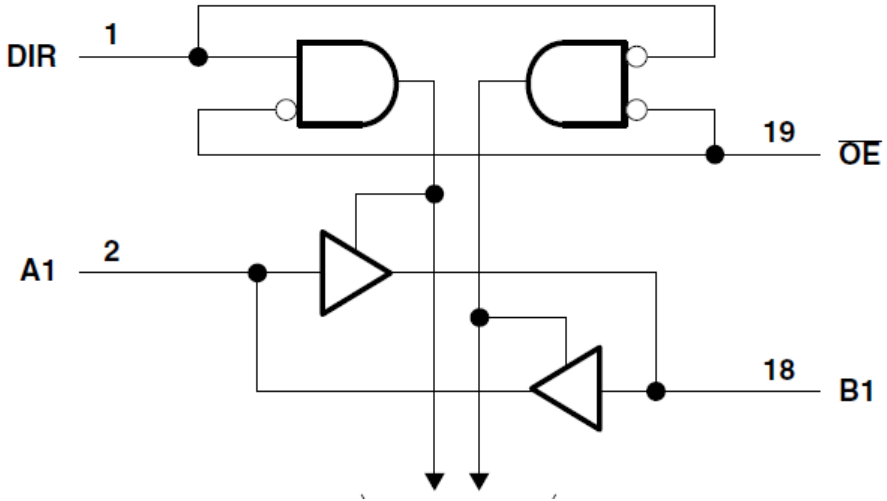
Level Translators Service Wide Range of Applications



HOW IS LEVEL TRANSLATION ACCOMPLISHED?

Level Translation - FET or Buffer





- Biased gate cuts off high voltage
- Allows bi-directional translation without control pin
- Any open drain or push pull application

- Different voltage domains for A and B port
- Needs direction control
- Push pull application shown

WHAT ARE THE OFFERINGS FROM NXP?

Voltage Level Translator Types and Features

I2C Family

Features:

- Single and Dual supply
- Bidirectional
- Auto-sensing
- Capacitive isolation
- High noise margin
- SCL/SDA – 2 bits

Applications

- I^2C buffering
- Long cable
- Hot-swap

FET Family

Features:

- Dual supply
- Bidirectional
- Auto-sensing
- Passive
- OD or PP
- External pull-ups required
- 1 - 10 bits wide

Applications

- Control interfaces
- I^2C-bus

NTS Family

Features:

- Dual supply
- Bidirectional
- Auto-sensing
- Passive
- OD or PP
- Integrated Pull up resistors
- 1 – 8 bits wide

Applications

- Control Interfaces
- I^2C-bus
-

NTB Family

Features:

- Dual supply
- Bidirectional
- Auto-sensing
- Isolates capacitance
- Push-pull only
- Low output drive
- 1 - 8 bits wide

Applications

- Control interfaces with active drive

GTL Family

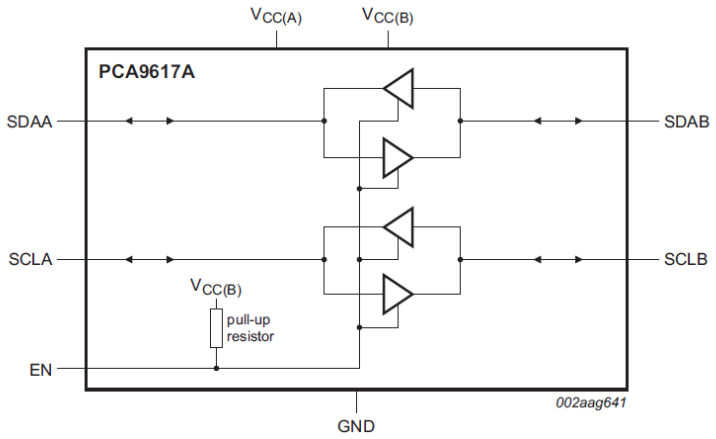
Features:

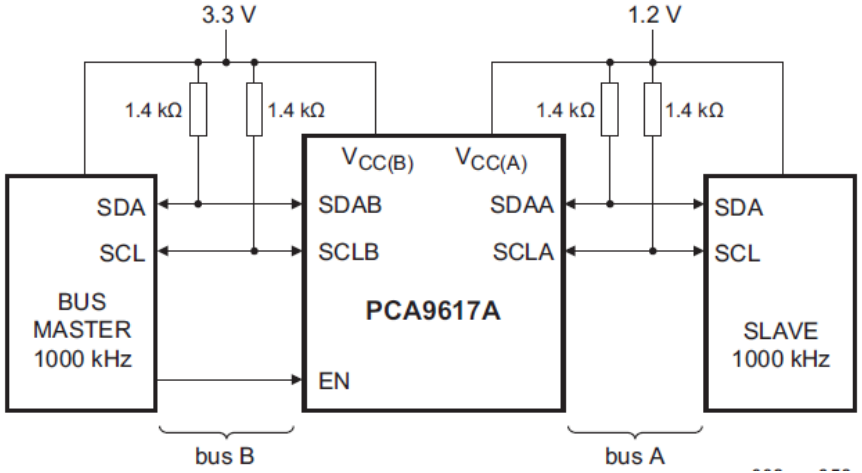
- Supports ‘GTL’ logic
- Dual supply
- Bidirectional
- Direction Pin
- Isolates capacitance
- GTL to LVTTL level translation – OD to PP
- 1 – 8 bits wide

Applications

- Supports GTL levels on Intel-processors

I²C Level Translating Buffer (Direction Sensing)

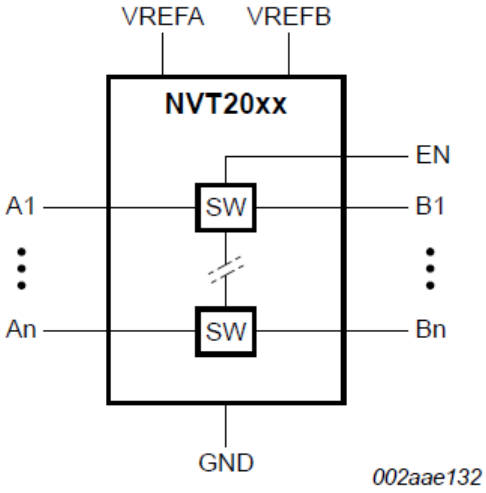


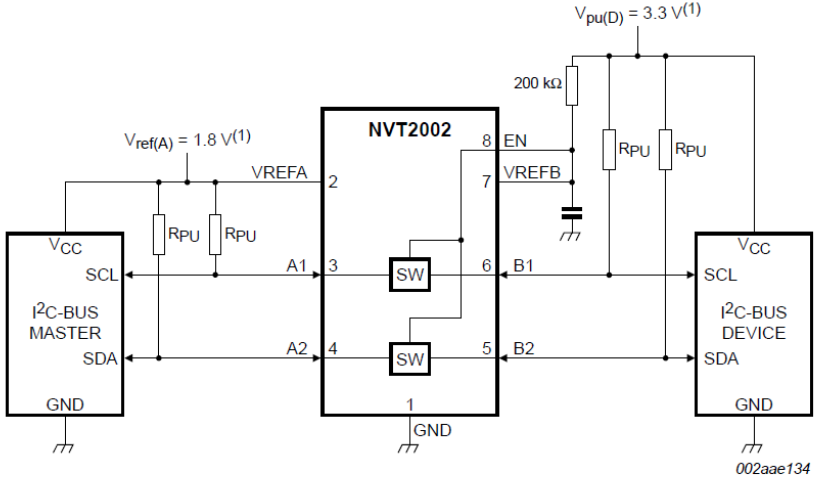


- I²C-bus up to 1 MHz
- Bi-directional with static offset on B Port for direction control
- Decided for I²C but can be used for any OD or PP application

- A Port works 0.8 V to 5.5 V
- B Port works 2.3 V to 5.5 V
- Different domains – Pull up resistor to rail
- Master and or slaves in any combination on either side

I²C Level Translating FET (Direction Sensing)



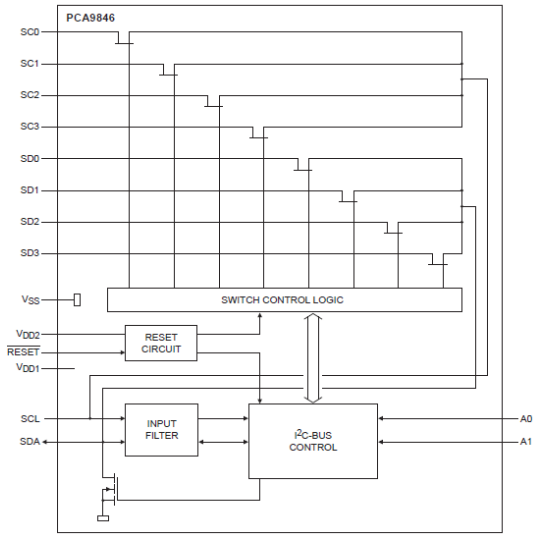


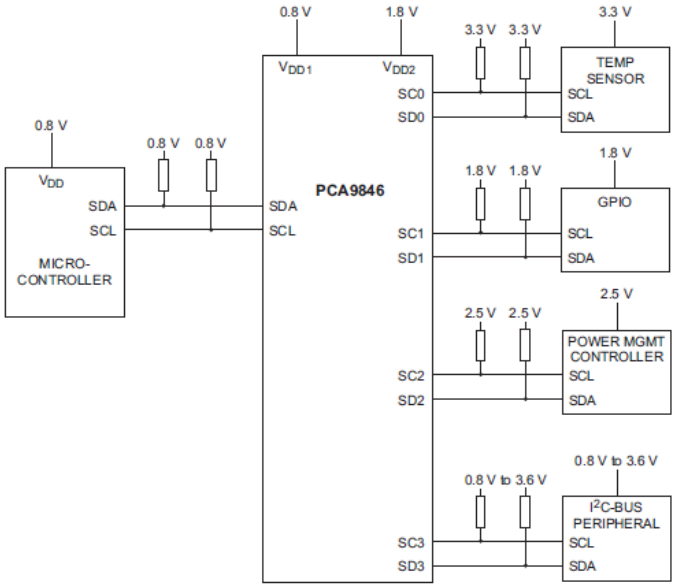
(1) The applied voltages at $V_{ref(A)}$ and $V_{pu(D)}$ should be such that $V_{ref(B)}$ is at least 1 V higher than $V_{ref(A)}$ for best translator operation.

- I2C-bus up to 3.4 MHz – RC time constant
- Bidirectional without control pin
- Any open drain or push pull application

- VREFA works 1.0V to 4.5V
- VREFB works 2.0V to 5.5V
- Lowest voltage clamps Vol – pull up resistor to rail
- Master and or slaves in any combination on either side

I²C Level Translating Mux (Direction Sensing)

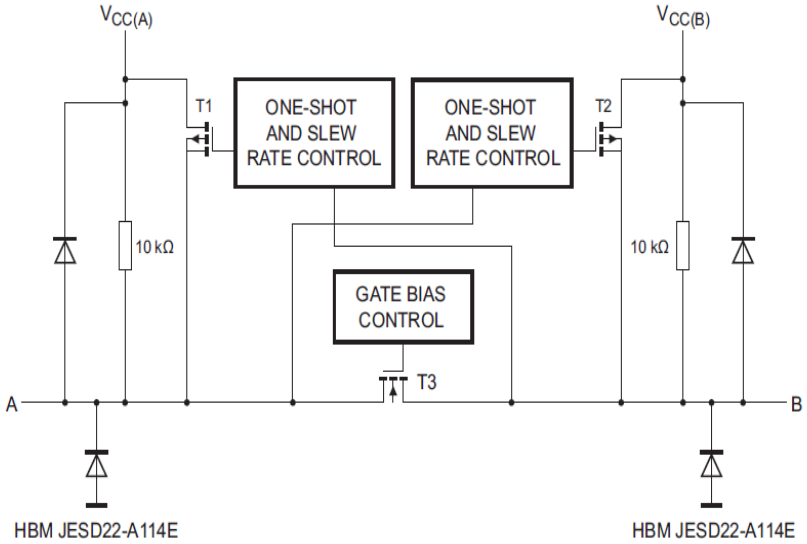


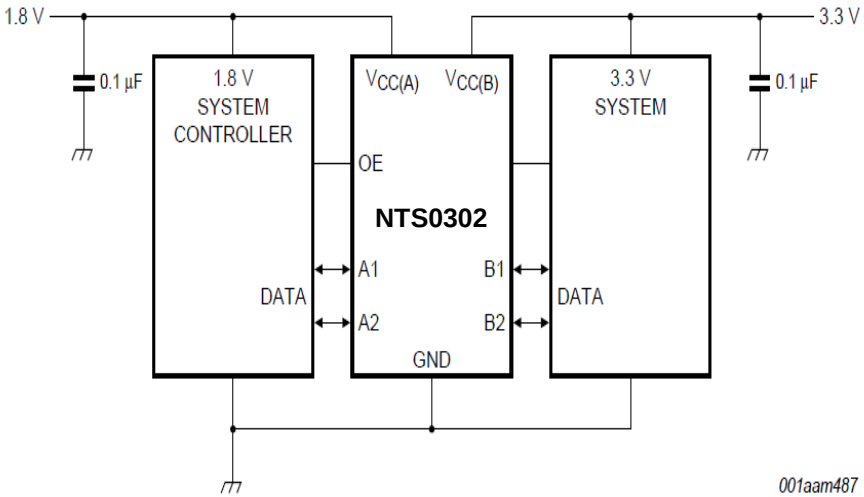


- I²C-bus up to 1 MHz
- Bidirectional without control pin
- Only for I²C-bus application

- VDD1 works 0.8 V to 3.6 V
- VDD2 works 1.65 V to 3.6 V
- Lowest voltage clamps Vol – pull up resistor to rail
- Master and or slaves in any combination on either side but need master on “inlet” to control state machine

I²C Level Translating FET with one shot (Direction Sensing)

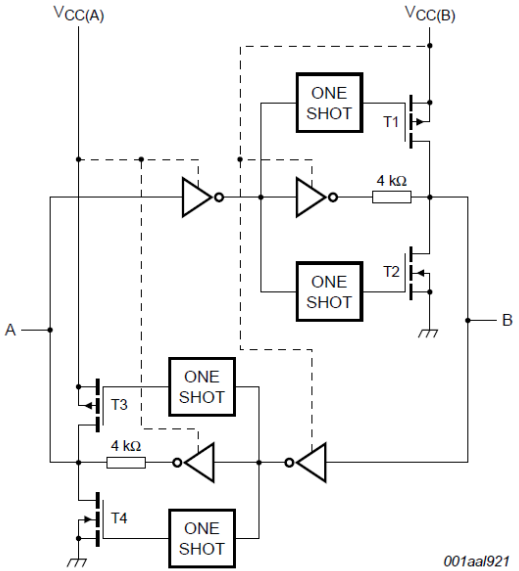


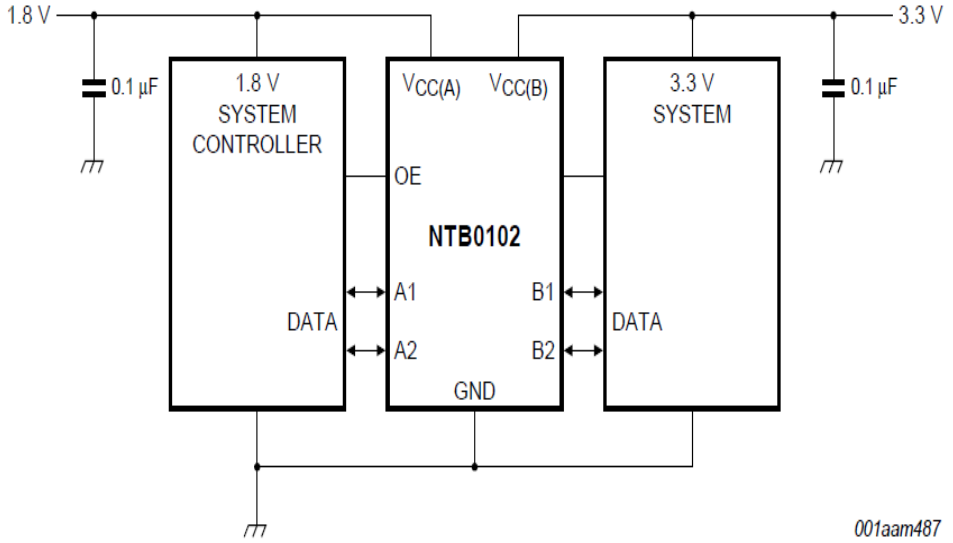


- I2C-bus up to 2MHz
- One shot potential ringing
- Bidirectional without control pin
- Any open drain or push pull application

- A Port works 0.95V to 3.6V
- B Port works 1.65V to 5.5V
- Lowest voltage clamps Vol – internal (or external) pull up resistor to rail and one shot
- Master and or slaves in any combination on either side

Level Translating Buffer with One Shot (Direction Sensing)

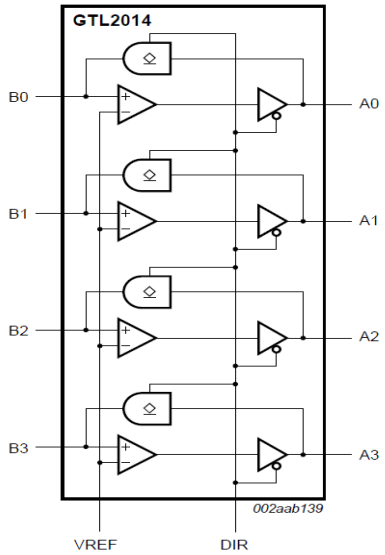




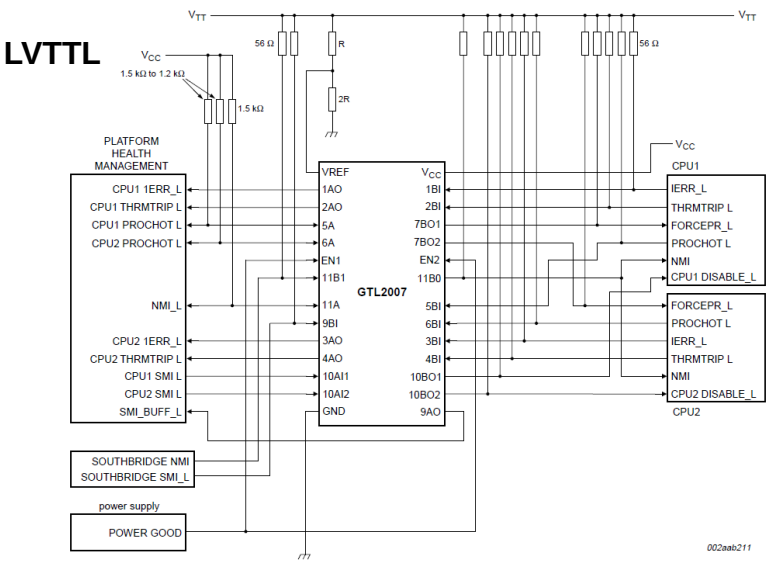
- Can not be used for I²C-bus
- Bi-directional without control pin – Weak output overdriven during reverse in direction
- Can be used for push pull application

- A Port works 1.2 V to 3.6 V
- B Port works 1.65 V to 5.5 V
- Buffer pulls to rail – one shot high and low
- Master and or slaves in any combination on either side

Level Translating Logic Buffer (No Direction Sensing)

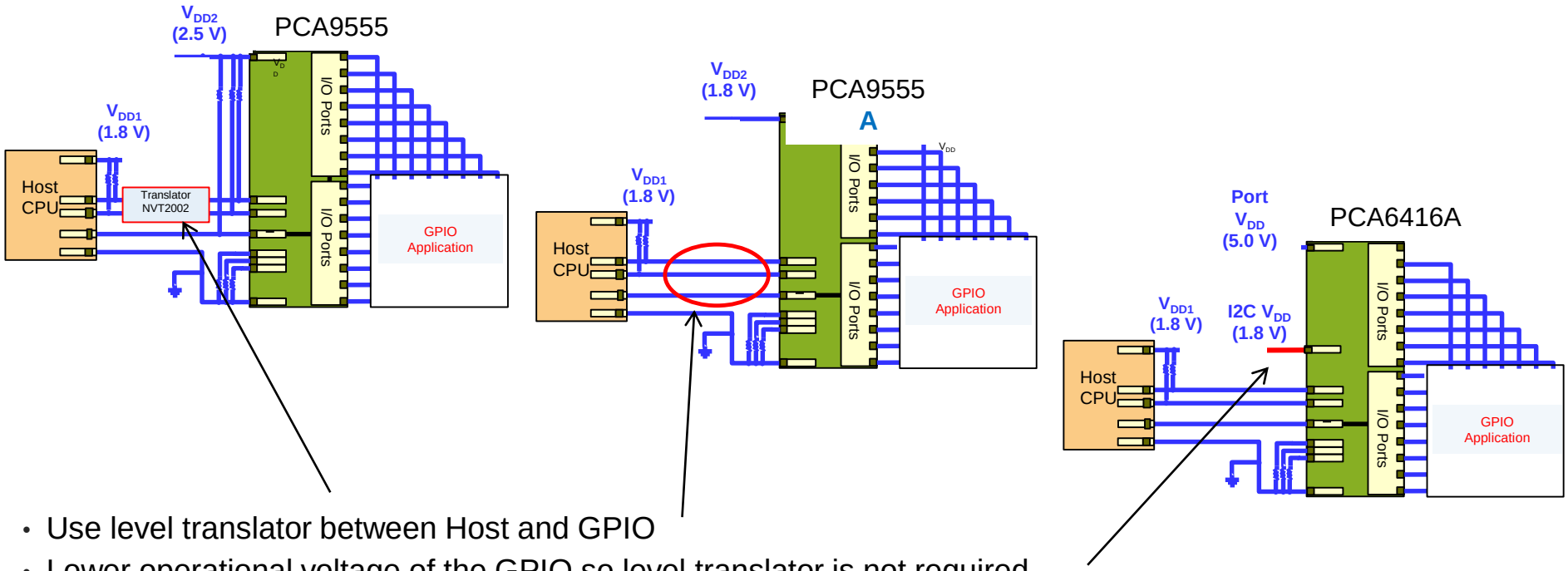


- Can not be used for I²C-bus
- **Direction pin** for control
- Can be used for open drain or push pull application



- A Port works 3.0 V to 3.6 V – not 5V tolerant
- B Port works to 3.6 V – threshold set by 2/3 of VTT
- A Port LVTTL - Buffer pulls to rail
- B Port open drain – pull up resistor to VTT (1.2 V)
- Standard logic is LVTTL both sides

Level Translating Logic Buffer (No Direction Sensing)

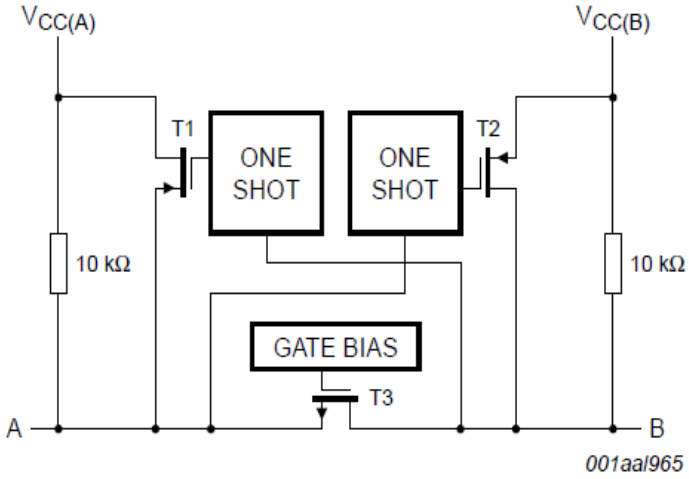


- Use level translator between Host and GPIO
- Lower operational voltage of the GPIO so level translator is not required
- Two supply pins so that I^2C interface and GPIO port operate at different voltages

WHAT ARE THE ADVANTAGES OF NXP'S VLT?

Introducing the NTS030x Level Translator

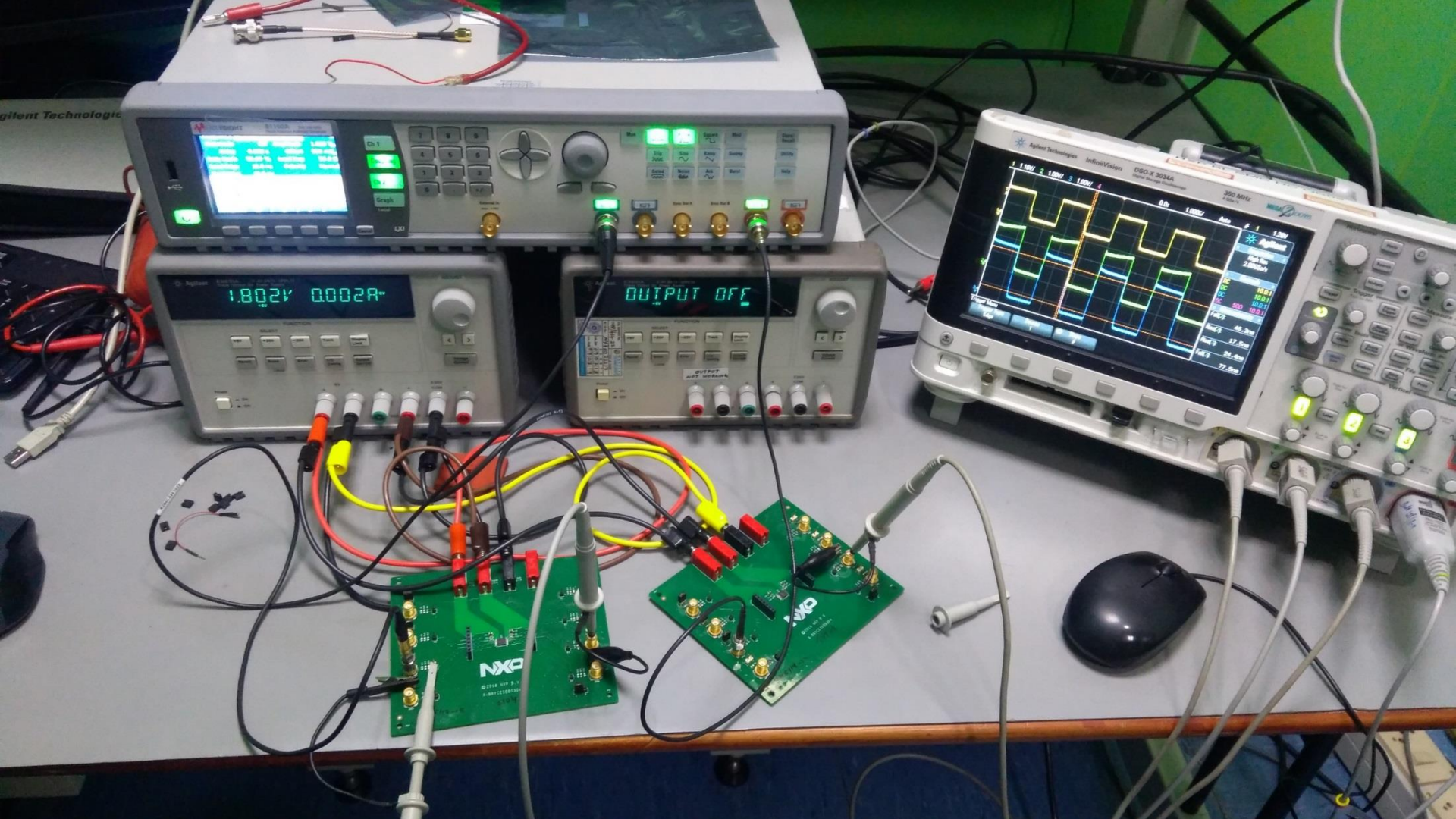
Wide & Ultra-Low Voltage
VCC(A): 0.95 V to 3.6 V &
VCC(B): 1.65 V to 5.5 V

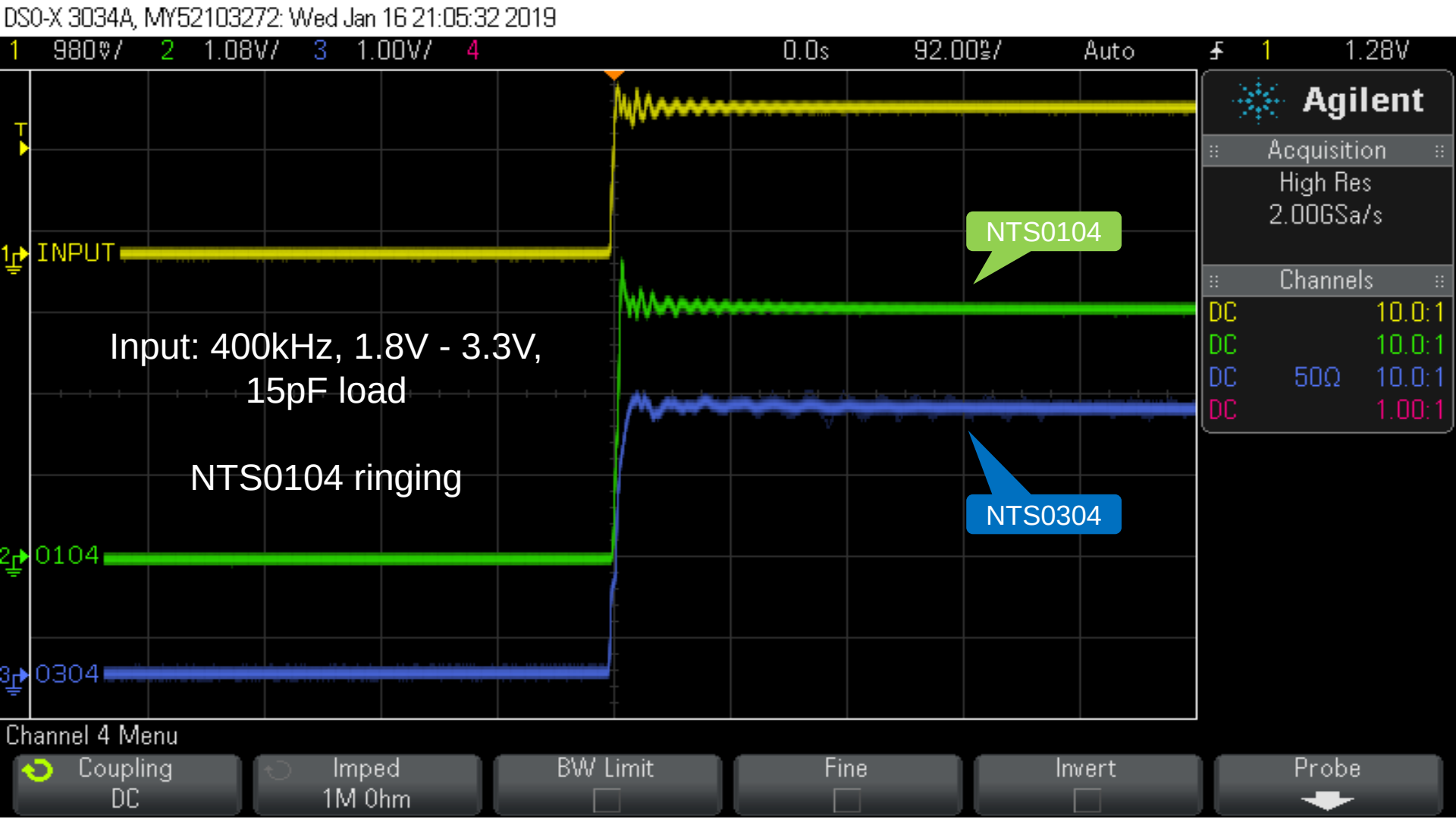


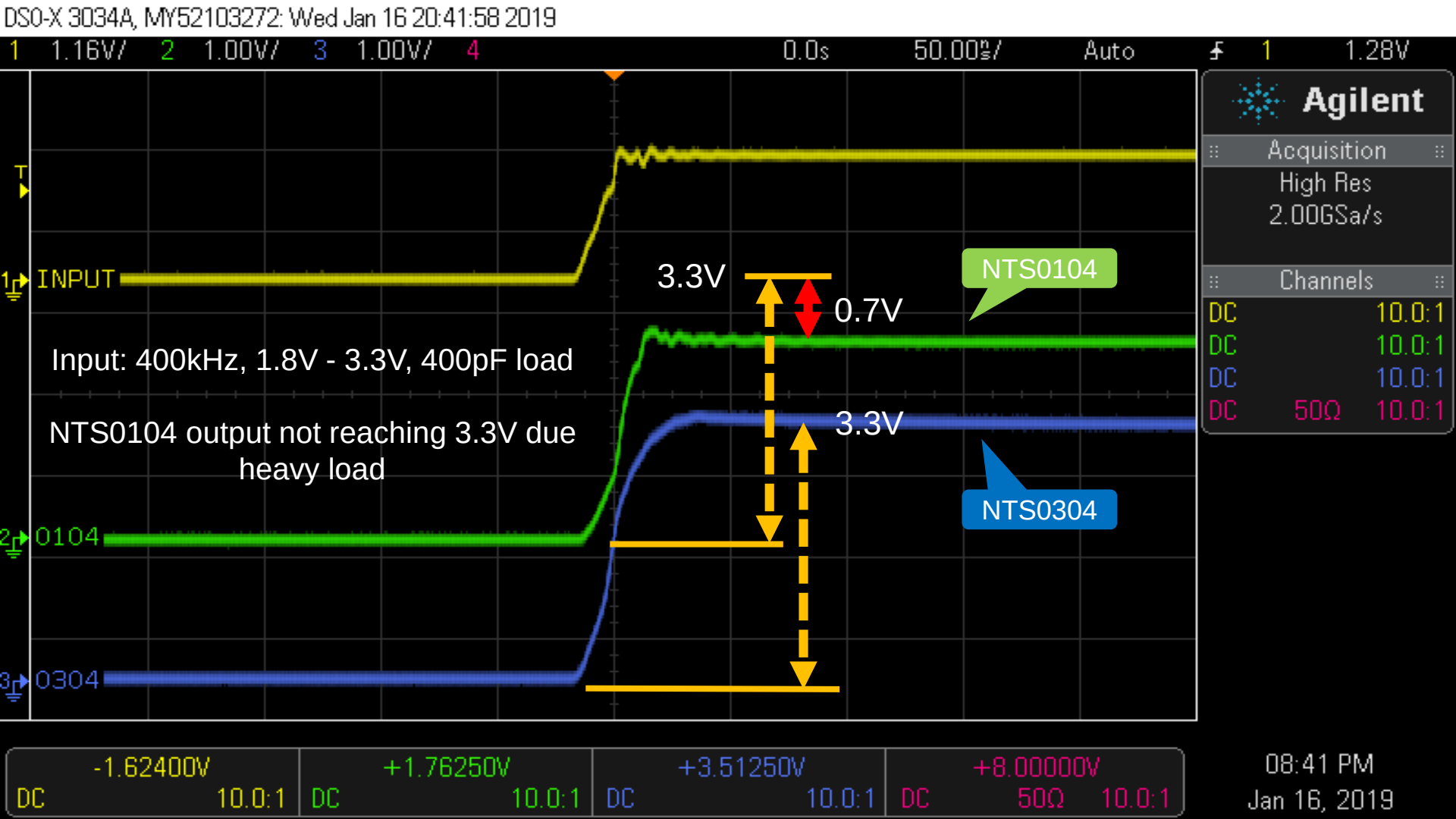
“Smart” One-Shot
50 ns Pulse & EMI Rejection

8 kV System-Level ESD Protection
(B-Port of 4 and 8-Ch)

Complete Family
1, 2, 4, and 8-Ch Level Translators


1.802V 0.002A
OUTPUT OFF
NXP
NXP


DSO-X 3034A, MY52103272: Wed Jan 16 21:05:32 2019
1 980mV/ 2 1.08V/ 3 1.00V/ 4
0.0s
92.00ns/
Auto
1 1.28V
Agilent
Acquisition
High Res
2.00GSa/s
Channels
DC 10.0:1
DC 10.0:1
DC 50Ω 10.0:1
DC 1.00:1
INPUT
NTS0104
Input: 400kHz, 1.8V - 3.3V,
15pF load
NTS0104 ringing
NTS0304
0104
0304
Channel 4 Menu
Coupling
DC
Imped
1M Ohm
BW Limit
Fine
Invert
Probe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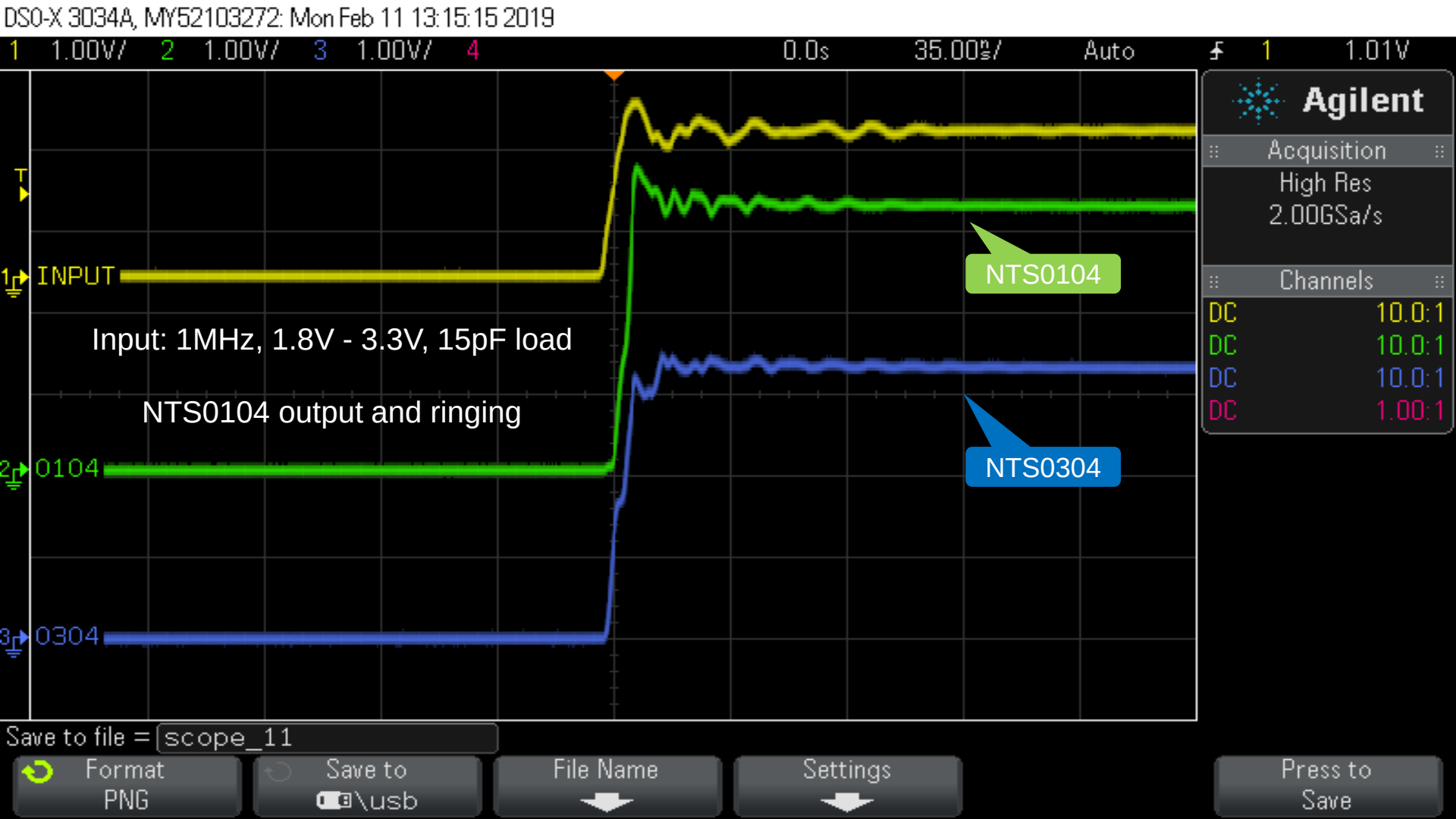
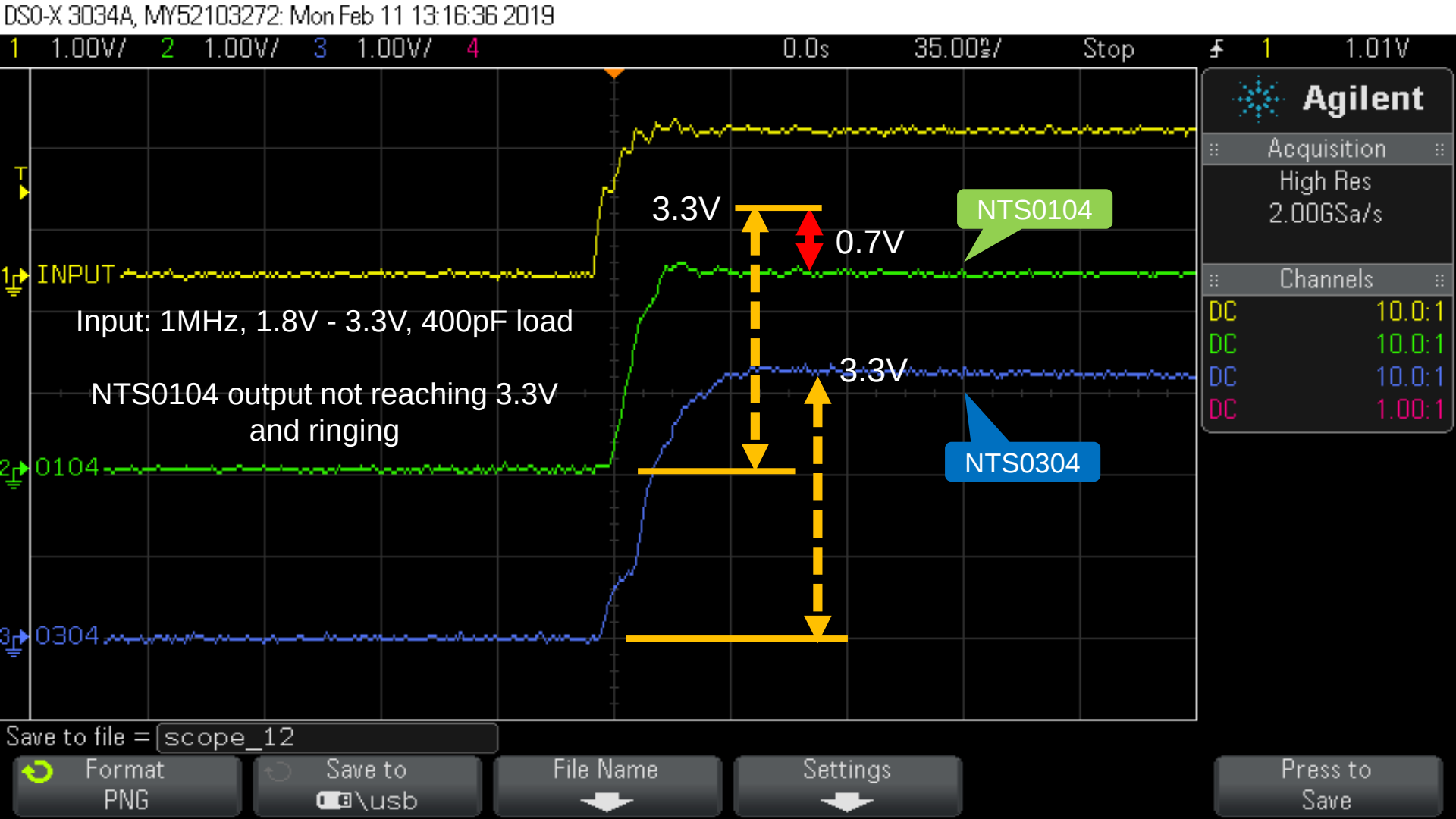
1 1.16V/ 2 1.00V/ 3 1.00V/ 4
0.0s
50.00ns/
Auto
1 1.28V
Agilent
Acquisition
High Res
2.00GSa/s
Channels
DC 10.0:1
DC 10.0:1
DC 10.0:1
DC 50Ω 10.0:1
INPUT
0104
0304
3.3V
0.7V
3.3V
NTS0104
NTS0304
Input: 400kHz, 1.8V - 3.3V, 400pF load
NTS0104 output not reaching 3.3V due heavy load
-1.62400V
DC 10.0:1
+1.76250V
DC 10.0:1
+3.51250V
DC 10.0:1
+8.00000V
DC 50Ω 10.0:1
08:41 PM
Jan 16, 2019


DSO-X 3034A, MY52103272: Mon Feb 11 13:15:15 2019
1 1.00V/ 2 1.00V/ 3 1.00V/ 4
0.0s
35.00ns/
Auto
1 1.01V
Agilent
Acquisition
High Res
2.00GSa/s
Channels
DC 10.0:1
DC 10.0:1
DC 10.0:1
DC 1.00:1
INPUT
0104
0304
NTS0104
NTS0304
Input: 1MHz, 1.8V - 3.3V, 15pF load
NTS0104 output and ringing
Save to file = scope_11
Format PNG
Save to \usb
File Name
Settings
Press to Save

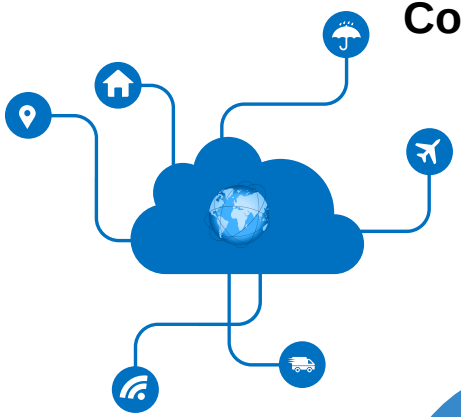

DSO-X 3034A, MY52103272: Mon Feb 11 13:16:36 2019
1 1.00V/ 2 1.00V/ 3 1.00V/ 4
0.0s
35.00ns/
Stop
1 1.01V
Agilent
Acquisition
High Res
2.00GSa/s
Channels
DC 10.0:1
DC 10.0:1
DC 10.0:1
DC 1.00:1
INPUT
0104
0304
3.3V
0.7V
NTS0104
3.3V
NTS0304
Input: 1MHz, 1.8V - 3.3V, 400pF load
NTS0104 output not reaching 3.3V
and ringing
Save to file = scope_12
Format
PNG
Save to
\usb
File Name
Settings
Press to
Save

Q&A

Level Translation Applications

Debit / Credit Cards

Communication Systems



Laptops

Smartphones

FOR MORE INFO PLEASE CONTACT

STEPHEN.BLOZIS@NXP.COM