Freescale Semiconductor
Addendum

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Errata to MPC750 RISC Microprocessor Family User's Manual, Rev. 1

This errata describes corrections to the *MPC750 RISC Microprocessor User's Manual*, Revision 1. For convenience, the section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

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C.4.2.2, C-16 In Section C.4.2.2, “isync Instruction Use with mtsr, mtsrin, and mtmsr” update the paragraph as follows:

The MPC750 and MPC755 have a restriction on the use of the **mtsr**, **mtsrin** or **mtmsr** instructions not described in the *Programming Environments Manual* or in Chapter 2, “Programming Model.” The MPC750 and MPC755 require that an **isync** instruction be executed after either an **mtsr** or **mtsrin** or **mtmsr** instruction. This **isync** instruction must occur after the execution of the **mtsr** or **mtsrin** or **mtmsr** and before the data address translation mechanism uses any of the on-chip segment registers.

C.5.2.3.2, C-24 In Section C.5.2.3.2, “Address Translation for Data Cache Locking,” update the code at the end of the section as follows:

```
# Enable instruction and data memory address translation. This
# corresponds to setting IR and DR in the MSR (bits 26 & 27)

mfmsr   r1
ori     r1, r1, 0x0030
sync
mtmsr   r1
isync
```

C.5.2.3.3, C-25 In Section C.5.2.3.3, “Disabling Exceptions for Data Cache Locking,” update the code at the end of the section as follows:

```
# Clear the following bits from the MSR:
#    EE (16)      ME (19)
#    FE0 (20)      FE1 (23)

mfmsr   r1
lis     r2, 0xFFFF
ori     r2, r2, 0x66FF
and     r1, r1, r2
sync
mtmsr   r1
isync
```

C.5.2.3.10, C-30 In Section C.5.2.3.10, “Address Translation for Instruction Cache Locking,” update the code at the end of the section as follows:

```
# Enable instruction and data memory address translation. This
# corresponds to setting IR and DR in the MSR (bits 26 & 27)

        mfmsr   r1
        ori     r1, r1, 0x0030
        sync
        mtmsr   r1
        isync
```

C.5.2.3.11, C-30 In Section C.5.2.3.11, “Disabling Exceptions for Instruction Cache Locking,” update the code at the end of the section as follows:

```
# Clear the following bits from the MSR:
#    EE (16)     ME (19)
#    FE0 (20)     FE1 (23)

        mfmsr   r1
        lis     r2, 0xFFFF
        ori     r2, r2, 0x66FF
        and     r1, r1, r2
        sync
        mtmsr   r1
        isync
```

C.11.6.2, C-72 Add sentence “The L2 tags must be globally invalidated before the L2 is enabled as a cache, private memory, or shared cache and private memory.”

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