Integrated Quad Half-Bridge and Triple High-Side with Embedded MCU and LIN for High End Mirror

908E621ACDWB

54-TERMINAL SOICW-EP

DWB SUFFIX
98ARL105910
54-TERMINAL SOICW-EP

Note For package dimensions, refer to the 908E621 device datasheet.

Thermal Addendum

Introduction

This thermal addendum ia provided as a supplement to the MM908E621 technical data sheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application and packaging information is provided in the data sheet.

Package and Thermal Considerations

This MM908E621 is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2. This results in two junction temperatures, T_{J1} and T_{J2}, and a thermal resistance matrix with $R_{\theta JAmn}$.

For *m*, *n* = 1, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1.

For *m* = 1, *n* = 2, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2. This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 1. Thermal Performance Comparison

Thermal Resistance	1 = Power Chip, 2 = Logic Chip [°C/W]		
	***m* = 1, *n* = 1**	***m* = 1, *n* = 2 *m* = 2, *n* = 1**	***m* = 2, *n* = 2**
$R_{\theta JAmn}$ (1)(2)	23	20	24
$R_{\theta JBmn}$ (2)(3)	9.0	6.0	10
$R_{\theta JAmn}$ (1)(4)	52	47	52
$R_{\theta JCmn}$ (5)	1.0	0	2.0

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.

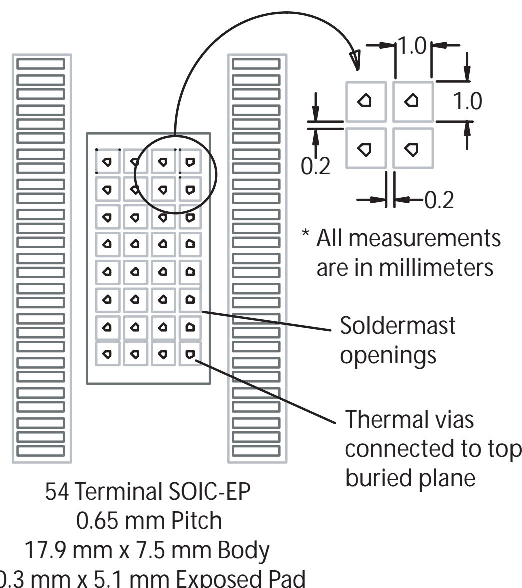

Figure 1. Thermal Land Pattern for Direct Thermal Attachment Per JEDEC JESD51-5

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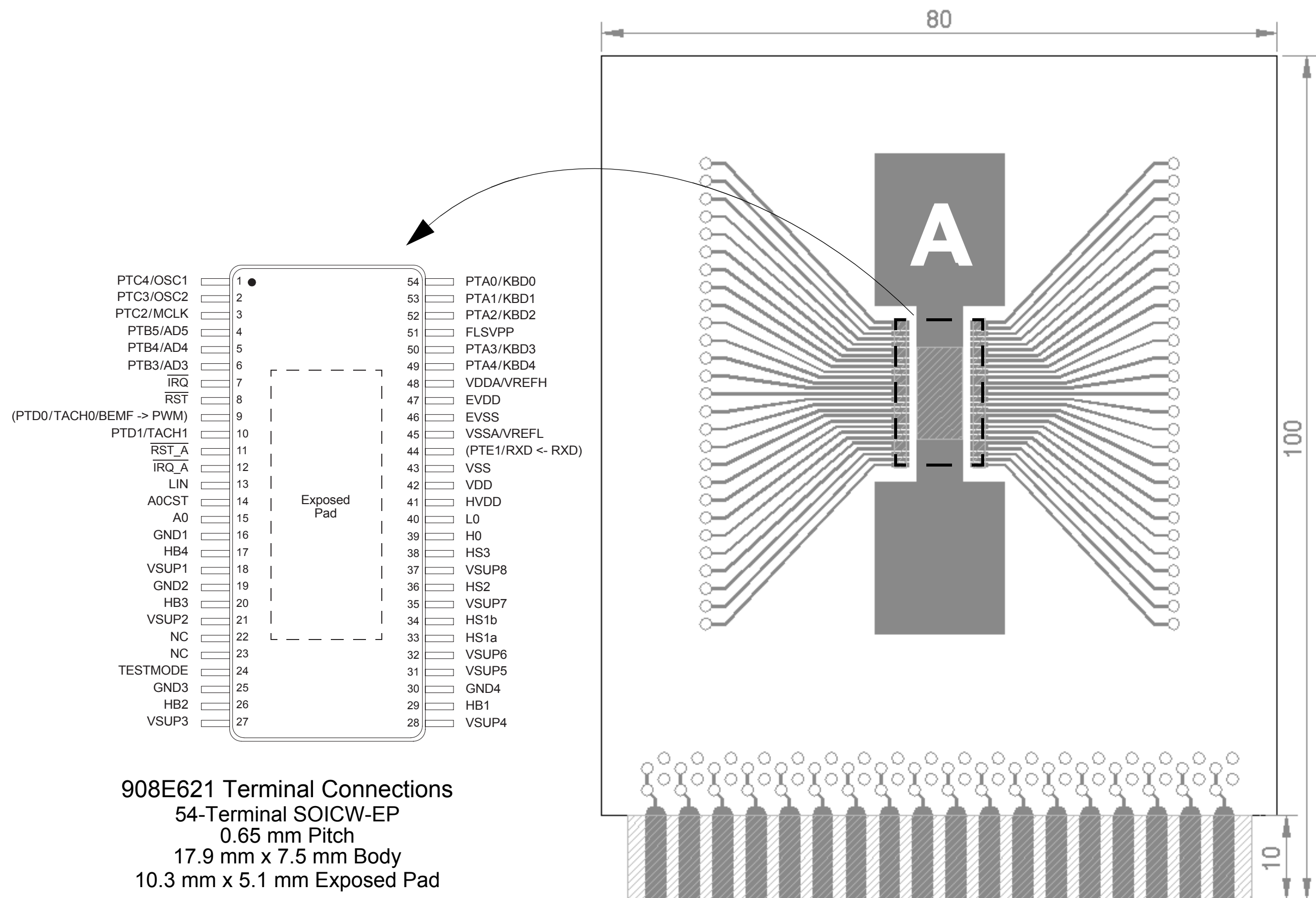

Figure 2. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area **A**:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 2. Thermal Resistance Performance

Thermal Resistance	Area A (mm^2)	1 = Power Chip, 2 = Logic Chip (°C/W)		
		m **= 1, *n*** **= 1**	***m*** **= 1, *n*** **= 2** ***m*** **= 2, *n*** **= 1**	***m*** **= 2, *n*** **= 2**
$R_{\theta JAmn}$	0	53	48	53
	300	39	34	38
	600	35	30	34
$R_{\theta JSmn}$	0	21	16	20
	300	15	11	15
	600	14	9.0	13

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

$R_{\theta JSmn}$ is the thermal resistance between die junction and the reference location on the board surface near a center lead of the package (see Figure 2)

This device is a dual die package. Index *m* indicates the die that is heated. Index *n* refers to the number of the die where the junction temperature is sensed.

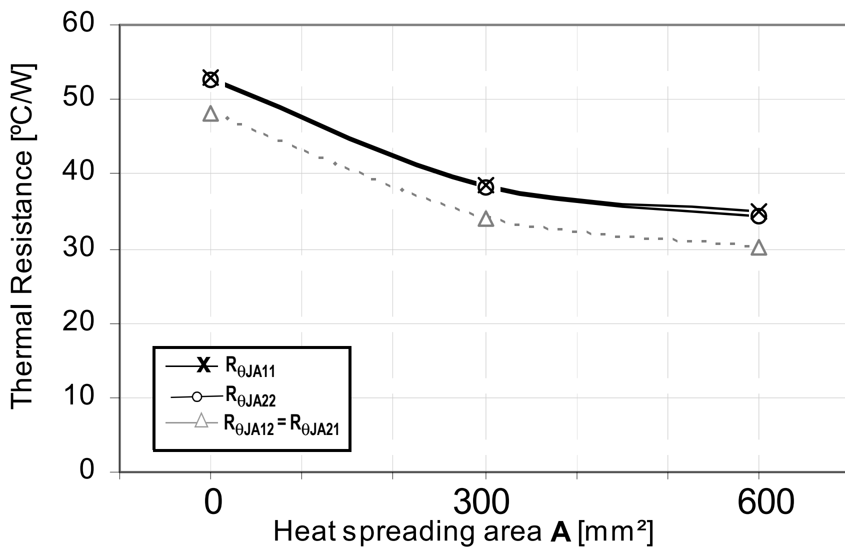

Figure 3. Device on Thermal Test Board $R_{\theta JA}$

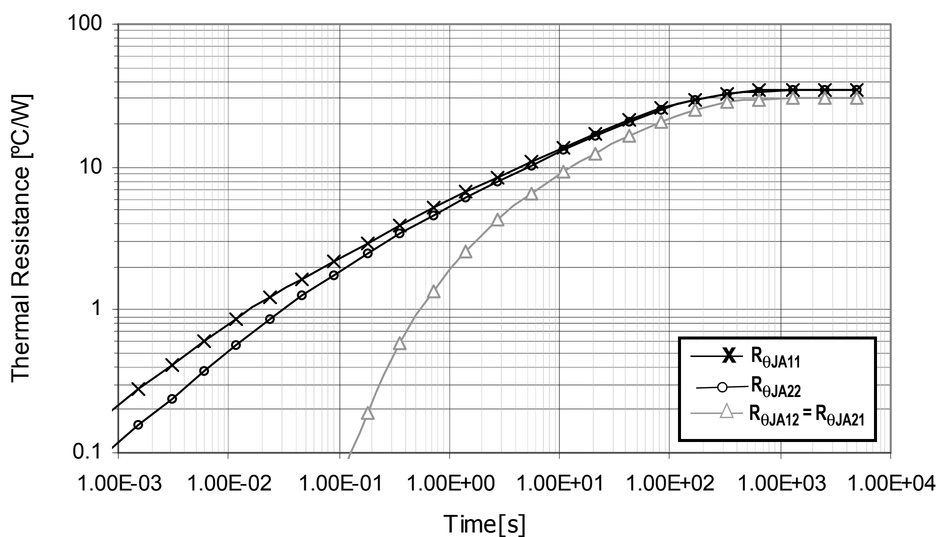

Figure 4. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response)
Device on Thermal Test Board Area A = 600 (mm^2)

How to Reach Us:

Home Page:
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E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
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