erformance Processors

MPC7410
Host Processor Built on Power Architecture™ Technology

The MPC7410 microprocessor is a high-performance, low-power, 32-bit implementation of the RISC architecture, built on Power Architecture™ technology, combined with a full 128-bit implementation of Freescale's AltiVec™ technology. It is an ideal microprocessor for leading-edge computing, embedded network control, signal processing, health care/imaging and other industrial applications. The MPC7410 offers the high-bandwidth MPX bus with minimized signal setup times and reduced idle cycles to increase maximum operating frequency to over 100 MHz, in addition to increased address and data bus bandwidth. To maintain compatibility for existing designs, the MPC7410 also supports the 60x bus protocol. MPC7410 microprocessors offer single-cycle, double-precision, floating-point performance; full symmetric multiprocessing (SMP) capabilities; and support for up to 2 MB of backside L2 cache. While the MPC7410 is software-compatible with existing MPC6xx and MPC7xx microprocessors, changes to existing source code are required in order to utilize the full potential of the AltiVec technology.

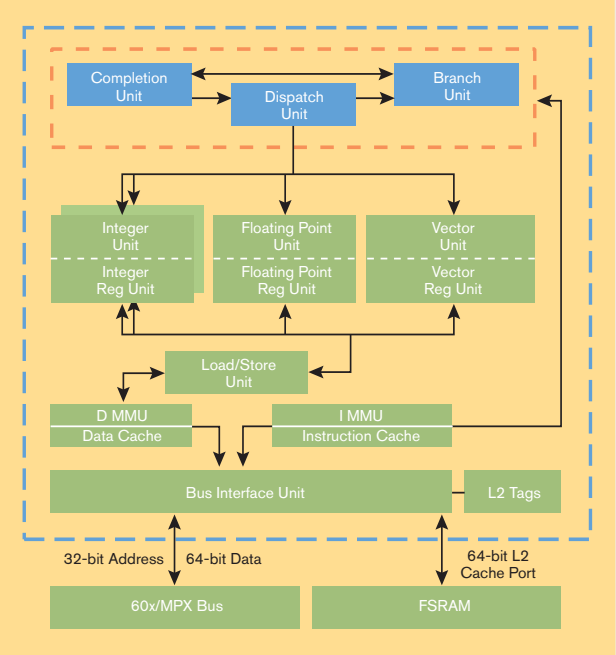
Example Applications

> Networking and telecommunications infrastructure

> High-performance computing (scientific, medical, etc.)

> Military/Aerospace/Industrial

MPC7410 BLOCK DIAGRAM



MPX Bus Interface

MPC7410 microprocessors support the MPX bus protocol with 64-bit data bus and 32-bit address bus. Support is included for burst, split, pipelined and out-of-order transactions, in addition to data streaming and data intervention (in SMP systems). The interface provides snooping for data cache coherency. The MPC7410 implements the MERSI cache coherency protocol for multiprocessing support in hardware, allowing access to system memory for additional caching bus masters, such as DMA devices.

Power Management

MPC7410 microprocessors feature a low-power 1.8V design with three power-saving, user-programmable modes—nap, doze (with bus snoop) and sleep—which progressively reduce the power drawn by the processor.

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MPC7410 HOST PROCESSOR HIGHLIGHTS

CPU Speeds–Internal	400, 450 and 500 MHz
CPU Bus Dividers	x3, x3.5, x4, x4.5, x5, x5.5, x6x6, .5x7, x7.5, x8, x9
Bus Interface	64-bit
Bus Protocol	MPX/60x
Instructions per Clock	3 (2 + Branch)
L1 Cache	32 KB instruction, 32 KB data
L2 Cache	512 KB, 1 MB or 2MB
Core-to-L2 Frequency	1:1, 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1
Typical Power Dissipation	5.3W @ 500 MHz, 3.29W @ 450 MHz (Low-Power Version)
Die Size	52 mm^2
Package	360 CBGA, HCTE and LGA
Process	0.18m CMOS
Voltage	1.5V or 1.8V internal, 1.8/2.5/3.3V I/O
SPEC int95 (estimated)	22.8 @ 500 MHz
SPECfp95 (estimated)	17.0 @ 500 MHz
Other Performance	917 MIPS @ 500 MHz
Execution Units	Integer(2), Floating-Point, Vector, Branch, Load/Share, System

Superscalar Microprocessor

MPC7410 microprocessors feature a high-frequency superscaler core, built on Power Architecture technology, capable of issuing three instructions per clock cycle (two instructions + branch) into eight independent execution units:

> Two integer units

> Double-precision floating-point unit

> Vector permute unit

> Vector arithmetic logic unit

> Branch processing unit

> Load/store unit

> System unit

Cache and MMU Support

The MPC7410 microprocessor has separate 32 KB, physically addressed instruction and data caches. Both caches feature cache locking and are eight-way set associative. The MPC7410 microprocessor's dedicated L2 cache interface with on-chip L2 tags features a very fast (up to core speed, 1:1) interface to memory, instruction-only or data-only modes, and parity checking on L2 data. The L2 data bus has both 32-bit and 64-bit modes, which can also be configured as private memory.

The MPC7410 microprocessor contains separate memory management units (MMUs) for instructions and data, supporting 4 petabytes (252) of virtual memory and 4 GB (232) of physical memory. The MPC7410 also has four instruction block address translation (iBAT) and four data block address translation (dBAT) registers.

AltiVec Technology

AltiVec technology expands the capabilities of Freescale's fourth generation of microprocessors implementing Power Architecture by providing leading-edge, general-purpose processing performance while concurrently addressing high-bandwidth data processing and algorithmic-intensive computations in a single-chip solution.

AltiVec Technology

> Meets the computational demands of networking infrastructure such as echo cancellation equipment and basestation processing.

> Enables faster, more secure encryption methods optimized for the SIMD processing model.

> Provides compelling performance for multimedia-oriented desktop computers, desktop publishing and digital video processing.

> Enables real-time processing of the most demanding data streams (MPEG-2 encode, continuous speech recognition and real-time, high-resolution 3-D memory for additional caching bus masters, such as DMA devices).

Contact Information

Freescale offers user manuals, application notes, sample code and full local support for all of its processors. For more information, visit: **www.freescale.com/networking**.

Learn More: For more information about Freescale products, please visit **www.freescale.com**.

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