PT2000ER

Errata sheet PT2000

Rev. 1.0 — 30 November 2016

Document information

Information	Content
Keywords	MC33PT2000, PT2000ER
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

1 Revision history

Table 1. Revision history

Rev	Date	Description
1.0	11/2016	• Initial release (added ERR1, ERR2) as per CIN# 201611050I

2 Product identification

This errata document applies to the PT2000 product family.

Table 2. Orderable part number identification

Part number	Version	Die ID	Package	Chip marking
PC33PT2000AE	2.0	N87J	LQFP80 EP	PC33PT2000AE
MC33PT2000AF				MC33PT2000AF

2.1 Device part number prefixes

The device samples marked with an M pre-fix indicates the product is in production, has full characterization, qualification and testing has been performed, unless otherwise noted.

2.2 Device build information / date code

The marked trace code is the link between the physically marked materials and the manufacturing lot's system genealogy information. Once the connection between the marked material and system genealogy information is made, traceability reports provide the material's manufacturing/shipping history. All devices listed in the Errata are affected unless specific date codes are provided.

3 Errata overview

Table 3. Functional problems table

Functional problems	Short description	Severity level [1][2][3][4]	Solution	Detailed description
ERR1	cksys out of spec	Low	When cksys error occurs, the IRQB pin must be pulled low and the MCU must undergo a full reset.	Section 4.1
ERR2	Missing access control for stfw instruction	Low	Assure that microcode is properly constructed to avoid accessing unassigned drivers.	Section 4.2

[1] High: Failure mode that severely inhibits the use of the device for all or a majority of intended applications
[2] Medium: Failure mode that might restrict or limit the use of the device for all or a majority of intended applications
[3] Low: Unexpected behavior that does not cause significant problems for the intended applications of the device
[4] Enhancement: Improvement made to the device due to previously found issues on the design

4 Functional problems detail

4.1 ERR1: cksys out of spec

4.1.1 Severity level

Low

4.1.2 Introduction

The PT2000 digital core and memories are specified for clock frequencies at or below 25.725 MHz (nominal 24 MHz). However, simulations of the PT2000 cksys frequency show that when a single event like phase shift, a missing pulse or a short pulse is created on the external CLK pin signal, cksys may exceed 24 MHz while still being propagated to the digital core. The high clock frequency can lead to a malfunction of the digital core.

Table 4 shows the situation where a critical cksys frequency can occur.

Table 4. List of cksys frequency issues

Situation	Fault(s)
Disturbance on CLK reference (when device is running on CLK reference)	1. cksys > 30 MHz for some clock pulses 2. PLL is unlocked

4.1.3 Problem

The PLL reacts very quickly to a disturbance in the CLK clock reference. In doing so, it may occasionally produce a cksys output frequency that exceeds the 24 MHz limit.

4.1.4 Work-around

To avoid a malfunction of the digital core and the power stage when ext. CLK fails, apply the following strategy:

- Configure ASIC to assert IrqB when loss of clock is detected
- IrqB is detected by µC
- Read ASIC status via SPI (for example, *backup_clock_status* register)
- Trigger SW reset of ECU if loss of clock is detected

Simulation confirms that the function of the IrqB pin and the SPI interface and registers is reliable up to a PLL output frequency of 83.3 MHz, which is 41.65 MHz on *cksys*.

4.1.5 Fix plan

None

4.2 ERR2: Missing access control for stfw instruction

4.2.1 Severity level

Low

4.2.2 Introduction

In the stfw instruction description section, the specification states that “the operation is successful only if the sequencer has the right to drive the output it has defined as shortcut1 (output access register)."

4.2.3 Problem

This feature was not implemented in silicon. Therefore, the stfw instruction is able to set/un-set outputs into free-wheeling mode even if the executing sequencer has no access to drive them.

4.2.4 Work-around

The stfw instruction's output_access limitation has no impact on the functional requirements of the device. The output_access limitation is a safety feature intended to prevent application code from inadvertently trying to use a driver not assigned to it. The absence of this feature has no affect on properly constructed application code. Therefore, no work-around is necessary.

4.2.5 Fix plan

None

5 Legal information

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