Mask Set Errata for Mask 0M74K

Introduction

This mask set errata applies to the mask 0M74K for these products:

- MC9S08DZ60
- MC9S08DZ48
- MC9S08DZ32
- MC9S08DZ16
- MC9S08DV60
- MC9S08DV48
- MC9S08DV32
- MC9S08DV16
- MC9S08DN60
- MC9S08DN48
- MC9S08DN32
- MC9S08DN16
- MC9S08DE60
- MC9S08DE32
- MC9S08EN32
- MC9S08EN16

MCU Device Mask Set Identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0J27F. All standard devices are marked with a mask set number and a date code.

MCU Device Date Codes

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "0301" indicates the first week of the year 2003.

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MCU Device Part Number Prefixes

Some MCU samples and devices are marked with an SC, PC, or XC prefix. An SC prefix denotes special/custom device. A PC prefix indicates a prototype device which has undergone basic testing only. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC or SC prefix.

SE157-ADC-INCORRECT-DATA : Boundary case may result in incorrect data being read in 10- and 12-bit modes

Errata type: *Silicon*
Affected componenet:*ADC*

Description

In normal 10-bit or 12-bit operation of the ADC, the coherency mechanism will freeze the conversion data such that when the high byte of data is read, the low byte of data is frozen, ensuring that the high and low bytes represent result data from the same conversion.

In the errata case, there is a single-cylce (bus clock) window per conversion cycle when a high byte may be read on the same cycle that subsequent a conversion is completing. Although extremely rare due to the precise timing required, in this case, it is possible that the data transfer occurs, and the low byte read may be from the most recently completed conversion.

In systems where the ADC is running off the bus clock, and the data is read immediately upon completion of the conversion, the errata will not occur. Also, in single conversion mode, if the data is read prior to starting a new conversion, then the errata will not occur.

The errata does not impact 8-bit operation.

Introducing significant delay between the conversion completion and reading the data, while a following conversion is executing/pending, could increase the probability for the errata to occur. Nested interrupts, significant differences between the bus clock and the ADC clock , and not handling the result register reads consecutively, can increase the delay and therefore the probability of the errata occuring.

Workarounds

Using the device in 8-bit mode will eliminate the possibility of the errata occuring.

Using the ADC in single conversion mode, and reading the data register prior to initiating a subsequent conversion will eliminate the possibility of the errata occuring.

Minimizing the delay between conversion complete and processing the data can minimize the risk of the errata occuring. Disabling interrupts on higher priority modules and avoiding nested interrupts can reduce possible contentions that may delay the time from completing a conversion and handling the data. Additionally, increasing the bus frequency when running the ADC off the asynchronous clock, may reduce the delay from conversion complete to handling of the data.

SE156-ADC-COCO : COCO bit may not get cleared when ADCSC1 is written to

Errata type: *Silicon*
Affected componenet:*ADC*

Description

If an ADC conversion is near completion when the ADC Status and Control 1 Register (ADCSC1) is written to (i.e., to change channels), it is possible for the conversion to complete, setting the COCO bit, before the write instruction is fully executed. In this scenario, the write may not clear the COCO bit, and the data in the ADC Result register (ADCR) will be that of the recently completed conversion.

If interrupts are enabled, then the interrupt vector will be taken immediately following the write to the ADCSC1 register.

Workarounds

It is recommended when writing to the ADCSC1 to change channels or stop continuous conversion, that you write to the register twice. The first time should be to turn the ADC off and disable interrupts, and the second should be to select the mode/channel and re-enable the interrupts.

SE143-ICS :
ICS Internal Reference Can Remain Enabled in Stop3 Mode

Errata type: *Silicon*
Affected componenet:*ICS*

Description

When transitioning from FEI or FBI modes to FEE or FBE modes, the internal reference clock may remain active in stop3 mode if the STOP instruction is executed soon after the IREFST bit in the ICSSC register clears. This can lead to elevated stop3 I_{DD}.

If interrupts are enabled, then the interrupt vector will be taken immediately following the write to the ADCSC1 register.

Workarounds

To ensure the internal reference clock is disabled before entering stop3, wait three internal reference clock periods after the IREFST bit has cleared before entering stop3. On a device with a trimmed internal reference, one period will be between 25.6 µs and 32 µs, therefore waiting 100 µs is adequate for all trimmed devices.

Or

To ensure the internal reference clock is disabled before entering stop3, transition into FEE mode and wait until the LOCK status bit indicates the FLL has attained lock before entering stop3 or transitioning into FBE mode and entering stop3.

SE127-IIC :
IIC Does Not Function When High Drive Strength Is Enabled on the IIC Pins

Errata type: *Silicon*

Affected componenet:*PWM*

Description

IIC operation requires open drain configuration but when the PTxDS bit associated with the IIC SDA or SCL pin is set for high drive strength (PTxDS = 1) the pin will be in complementary drive mode instead of open drain mode. This will cause IIC communication conflicts that lead to IIC malfunction.

Workarounds

The PTxDS bits associated with the IIC SDA and SCL pins should be cleared for low drive strength operation. This configuration will ensure that the corresponding pin will enter open drain mode and IIC communications will function correctly. The IIC pull-up resistor in the final application may need to be modified to account for the lower drive strength of the SDA and SCL pins.