Mask Set Errata for Mask 2N05E

This report applies to mask 2N05E for these products:

- MC9S12VR64
- MC9S12VR48

Table 1. Errata and Information Summary

Erratum ID	Erratum Title
e5310	LINPHY: False wake-up pulse by re-entering STOP
e8346	SCI: RXEDGIF interrupt miss while enter STOP
e4598	SCI: RXEDGIF occurs more times than expected in IR mode

Table 2. Revision History

Revision	Changes
October 25, 2012	Initial revision
August 12, 2015	Errata added: e8346, e5310 Errata removed: None Errata changed: None

e5310: LINPHY: False wake-up pulse by re-entering STOP

Description: When using the LINPHY wake-up functionality in combination with other wake-up sources the following can happen:

If other wake-up source (like a periodic time interrupt) wakes the device up while it is receiving a LIN bus wake-up pulse there is a small probability that in the moment of re-entering STOP mode the LINPHY generates a false wake-up impulse.

This happens when the other wake-up source wakes the device in a small window after the recessive edge of the LIN wake-up pulse. Also can happen if the LIN bus is dominant when the device goes again into stop mode.

This false wake-up does not disrupts the LINPHY wake-up functionality and afterwards the LINPHY resumes its normal operation.

Workaround: As there is no way to distinguish it was a false LIN wake-up event, the software must implement an idle timeout control in the RxD line and go to sleep again if no break is fetch 250ms after the wake-up event. (LIN Protocol Specification v2.1).

Furthermore software must take care not to go into stop mode if the LIN bus is dominant.

e8346: SCI: RXEDGIF interrupt miss while enter STOP

Description: If an active edge (falling if RXPOL=0, rising if RXPOL=1) on the RXD input occurs shortly after the execution of the STOP instruction the RXEDGIF is not asserted and the CPU is not woken up. The time window in during which the edge is missed starts about 10 bus cycles after the STOP instruction and is 2-3 bus cycles wide.

Workaround: (1) If more than one edge with a minimum distance of 4 bus cycles occur, the 2nd edge will wake up the CPU. This is the case for instance in a LIN bus system. “The Wake Up Signal consists of a dominant pulse minimum 250 microseconds and maximum 5 milliseconds in length, and it may be sent by any LIN node.”

(2) Use the API to enforce a periodic wake up and check the level of the LIN input.

(3) Reduce the likelihood of occurrence by increasing the bus frequency.

e4598: SCI: RXEDGIF occurs more times than expected in IR mode

Description: Configured for Infrared Receive mode, the SCI may incorrectly set the RXEDGIF bit if there are consecutive ‘00’ data bits. There are two cases:

Case 1: due to re-sync of the RXD input, the received edge may be delayed by one bus cycle. If an edge (bit = ‘0’) is detected near an SCI clock edge, the next edge (bit = ‘0’) may be detected one SCI clock later than expected due to re-sync logic.

Case 2: if external baud is slower than SCI receiver, the next edge may be detected later than expected.

This glitch can be detected by the RXEDGIF circuit, but it does not impact the final data result because the SCI receive and data recovery logic takes samples at RT8, RT9, and RT10.

Workaround: Case 1 and case 2 may occurs at same time. To avoid those unexpected RXEDGIF at IR mode, the external baud should be kept a little bit faster than receiver baud by:

$P > (1/16)/(SBR)$

or

$(P)(SBR)(16)> 1$

Where SBR is baud of receiver, P is external baud faster ratio.

For example:

1.- When SBR = 16, P = 0.4%, this means the external baud should be at least 0.4% faster than receiver.

2.- When SBR = 4, P = 1.6%, this means the external baud should be at least 1.6% faster than receiver.

Case 1 will cover case 2, i.e. case 1 is the worst case. If case1 is solved, case 2 is also solved.

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