ES_FXLS8962AF

Errata sheet - FXLS8962AF

Rev. 1 — 21 December 2017

Errata sheet
COMPANY PUBLIC

Document information

Information	Content
Keywords	FXLS8962AF
Abstract	This errata sheet describes the known functional problems and/or deviations from the product electrical specifications as of the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

1 Revision history

Table 1. Revision history

Rev	Date	Description
1	20171221	Added E1, E2, E3

2 Product identification

The WHO_AM_I register (address 13h) identifies the device.

The PROD_REV register (address 12h) identifies the device revision.

This Errata sheet covers the following devices:

Table 2. Device identification table

Identifier	WHO_AM_I	PROD_REV	Device	Revision
'A'	62h	11h	FXLS8962AF	1.0

3 Errata overview

Table 3. Functional problems table

Functional problems	Short description	Identifier	Detailed description
E1	Noise coupling in analog front end (AFE) measurements during serial communication	'A'	Section 4.1
E2	Unintended pulse during boot phase	'A'	Section 4.2
E3	FIFO burst read operation error using I2C interface	'A'	Section 4.3

4 Functional problems detail

4.1 E1: Noise coupling in analog front end (AFE) measurements during serial communication

Introduction

This erratum is related to the noise coupling in sensor measurements when serial communications (through I^2C or SPI) overlaps with the measurement phase of the device.

Problem

Serial bus signals (I^2C/SPI) through the SA0, SPI_MISO, SPI_MOSI, SPI_DATA, SDA, SCL and SCLK pins couple noise to the sensor's internal voltage shield. If communication occurs during the measurement phase of the device, then the coupled noise to the voltage shield affects the magnitude of the current measurements (see Figure 1 and Figure 2), causing the device to exceed its noise specification.

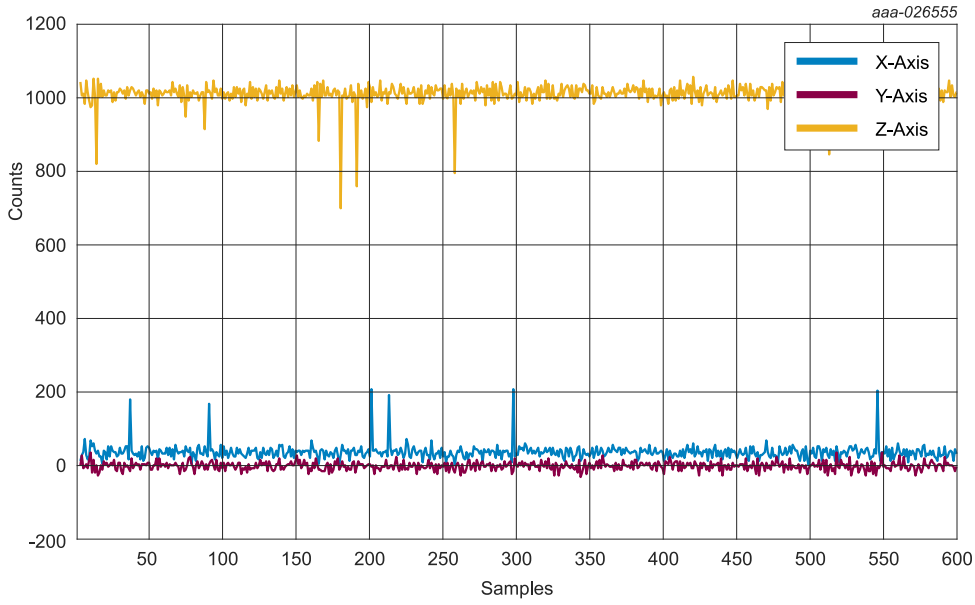


Figure 1. Noise coupling due to serial communication

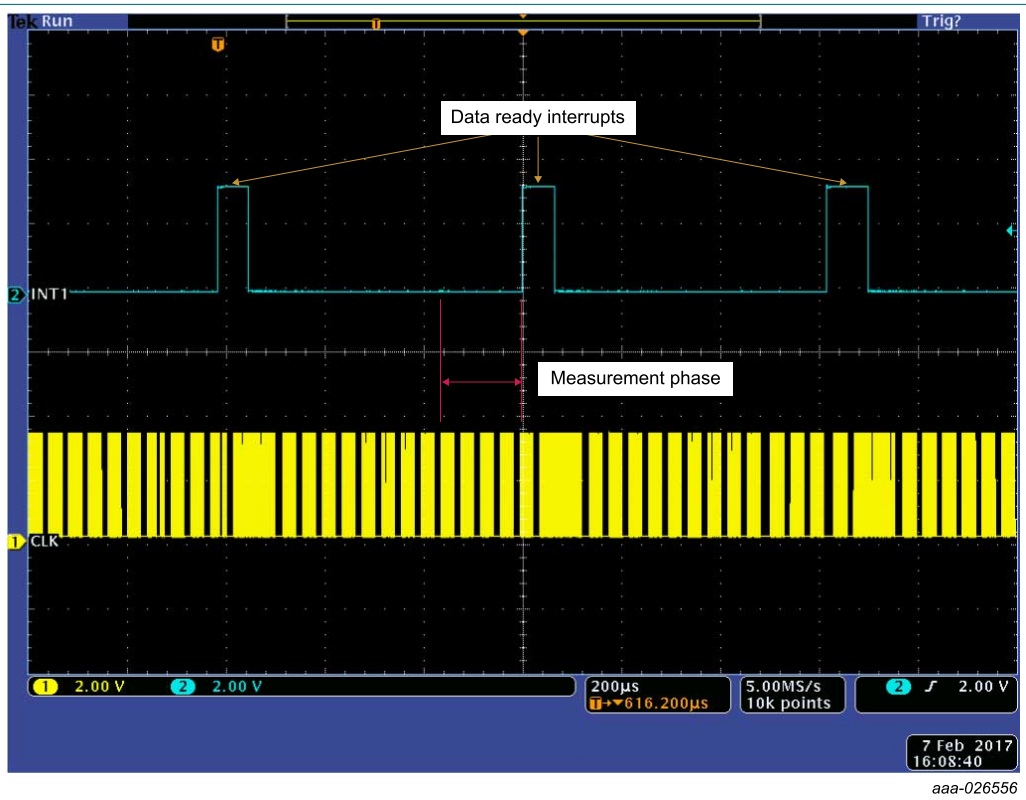


Figure 2. Serial communication overlapping with sensor measurement phase

Workaround

Reduce the susceptibility of the sensor measurements to induced noise by minimizing the communication traffic on the serial interface during the measurement phase of the

sensor. Configure the system such that the host MCU collects sensor data using data ready interrupts before the next measurement phase begins. (see Figure 3 and Figure 4).

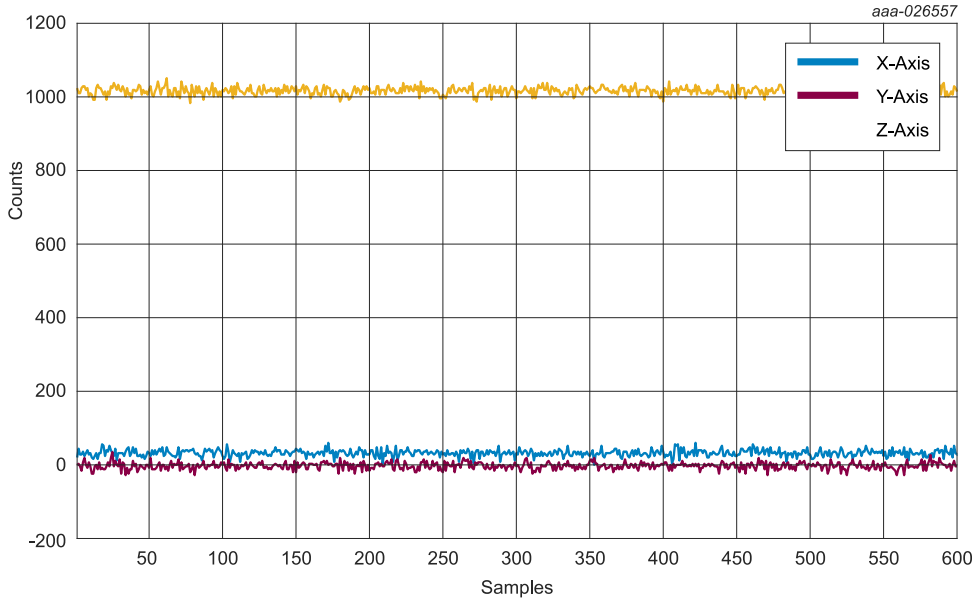


Figure 3. No noise coupling in sensor measurements

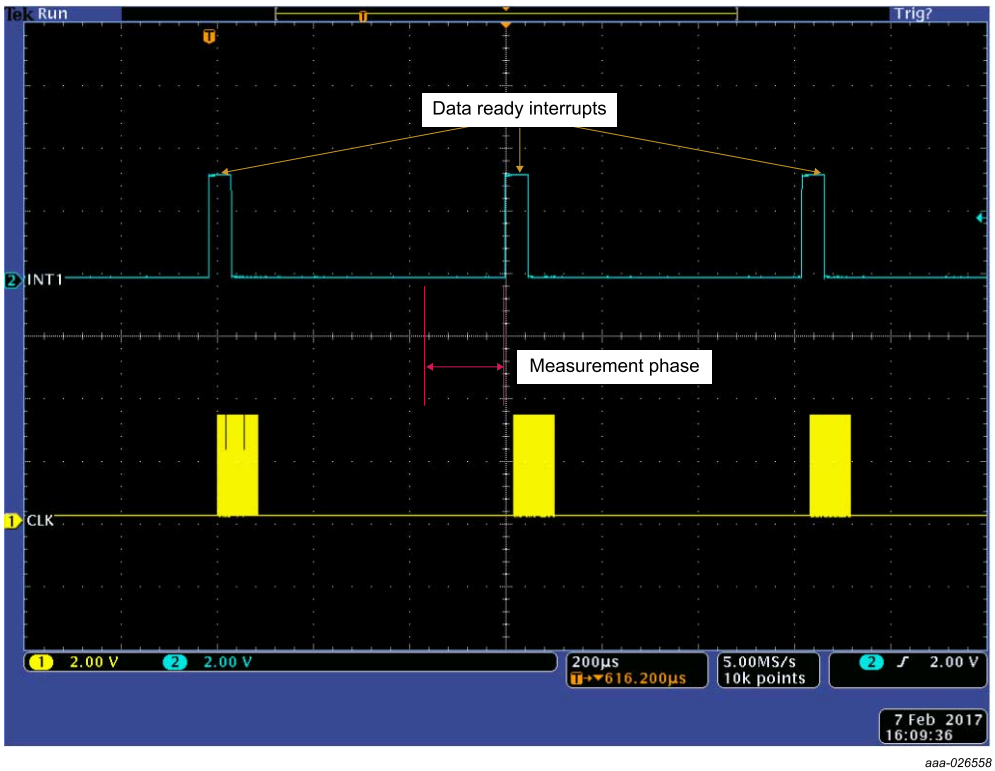


Figure 4. No serial communication overlap with measurement phase

Using data ready interrupts

The data ready interrupt in FXLS8962 is enabled using the INT_EN register (address 20h) and INT_PIN_SEL register (address 21h) (Table 4 and Table 5).

1. Enable **INT_EN[**DRDY_EN**]**.
2. Map the data ready interrupt to one of the INTx pins available on the device. Set DRDY_INT2 bit to route data ready interrupt to INT2 pin or clear the bit to route to INT1 pin.

Note:

In the case of BT_MODE = V_{DD} (motion detect mode), only INT1 pin can be used. The INT2 pin function is reserved for the boot output pulse and, therefore, is not available for this purpose.

*Also, when the INT2 pin is configured for the external trigger function, for example, when **SENS_CONFIG4[**INT2_FUNC**]** = 1, a logic '1' value in DRDY_INT2 bit field is ignored.*

Table 4. INT_EN register (address 20h)

Bit	7	6	5	4	3	2	1	0
Name	DRDY_EN	BUF_EN	SDCD_ OT_EN	SDCD_ WT_EN	ORIEN T_EN	ASLP_EN	BOOT_DIS	WAKE_ OUT_EN
Reset (BT_MODE = 0)	0	0	0	0	0	0	0	0
Reset (BT_MODE = 1)	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 5. INT_PIN_SEL register (address 21h)

Bit	7	6	5	4	3	2	1	0
Read	DRDY_INT2	—	SDCD_ OT_INT2	SDCD_ WT_INT2	ORIEN T_INT2	ASLP_INT2	BOOT_INT2	WAKE_O UT_INT2
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Time window to perform serial communication after receiving data ready interrupt

Note that upon reception of the data ready interrupt on the selected interrupt pin, the host must quickly do a burst read of the data registers before the next measurement cycle begins for the successive data sample. This ensures that the bus communications associated with reading the current data sample does not couple noise to the successive data sample measurement.

In addition, if FXLS8962 is used in a shared I^2C/SPI bus along with other devices, the communication with other devices must complete before the next measurement cycle in FXLS8962 begins, in order to prevent bus traffic from inducing noise to the sensor measurement.

Table 6. Measurement phase timings

Sample size = 30

Mean (µs)	Standard deviation (µs)
126.1	0.88

Table 7 identifies the maximum time window (from the starting edge of the data ready interrupt) within which all the serial communications must complete before the measurement phase for the next sample begins.

Table 7. Time window allowed for serial communications after the rising edge of the data ready interrupt

Average value from 30 samples.

Mode	Time (µs)
LPM (ODR dependent)	$Time\ window = \frac{1.0 \times 10^6}{1.1 \times ODR} - 1.1 \times measurement\ phase$ where: measurement phase = 126.1 µs (Table 6),
HPM	$Time\ window = \frac{1.0 \times 10^6}{1.1 \times 3200} - 1.1 \times measurement\ phase = 145.38$ where: measurement phase = 126.1 µs (Table 6),

For example, with the device operating with ODR = 200 Hz in LPM mode, the time window allowed for serial communications after the starting edge of the DRDY interrupt = 4406 µs.

Fix plan

None.

4.2 E2: Unintended pulse during boot phase

Introduction

During boot phase execution of FXLS8962AF with BT_MODE = GND, the device is initialized and any default configuration parameters are loaded from OTP memory. When this phase is complete, the SRC_BOOT bit is set and a $T_{PULSE\text{-}BOOT1}$ ms pulse may be signaled on either one of the INT1/2 pins (defaults to enabled on the INT1 pin after POR) (see Figure 5).

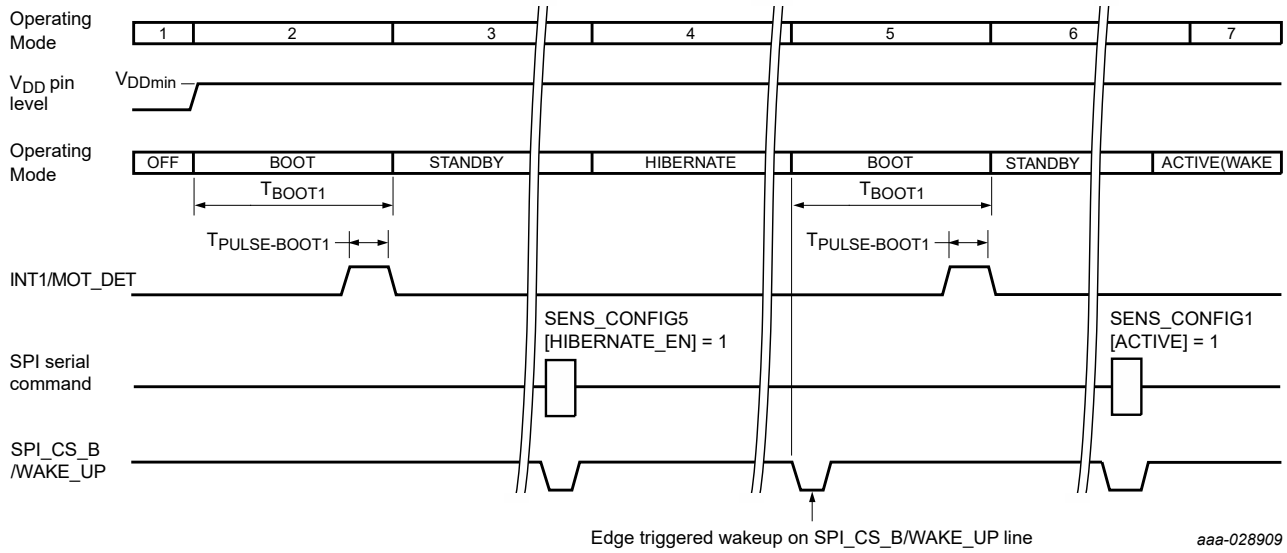


Figure 5. BOOT1 sequence (BT_MODE = GND)

Similarly, during boot phase execution with BT_MODE = VDD, this device is initialized and any default configuration parameters are loaded from OTP memory, along with any default Motion Detection function specific parameters. When this phase is complete, the SRC_BOOT bit is set and a $T_{PULSE-BOOT2}$ ms pulse is signaled on the INT2 pin (see Figure 6).

Note: *With BT_MODE = VDD, the boot pulse is routed to the INT2 pin and cannot be routed to the INT1 pin.*

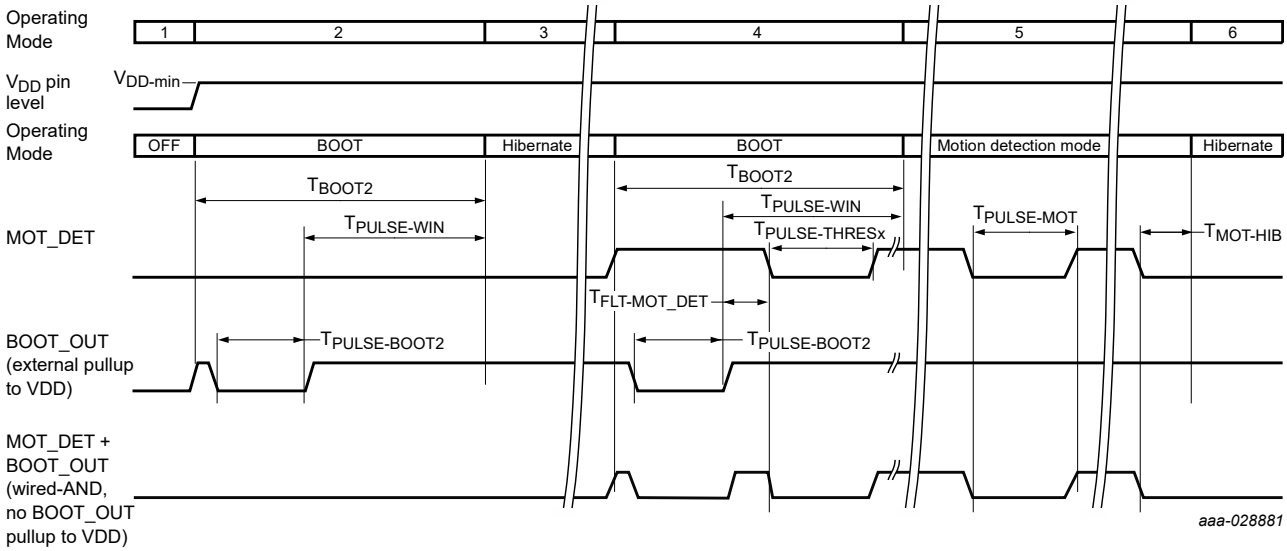


Figure 6. BOOT2 sequence (BT_MODE = V_{DD})

Problem

An unintended pulse occurs just before the occurrence of $T_{PULSE-BOOT1}$ or T_{PULSE_BOOT2} under the following boot execution scenarios:

- Power on Reset (POR) when BT_MODE = GND
- POR when BT_MODE = VDD
- Soft reset when BT_MODE = VDD

The unintended pulse leads to a double pulse observation.

POR when BT_MODE = GND

Upon POR, the boot pulse is issued for $T_{PULSE-BOOT1}$ ms at the completion of boot phase on either the INT1 or INT2 lines depending on the device configuration (see Figure 5). However, an unintended pulse approximately 50 µs in duration occurs just before the starting edge of the boot pulse, as shown in Figure 7.

Note: *The unintended pulse occurs on POR only when there is a pull-up resistor on the configured interrupt.*

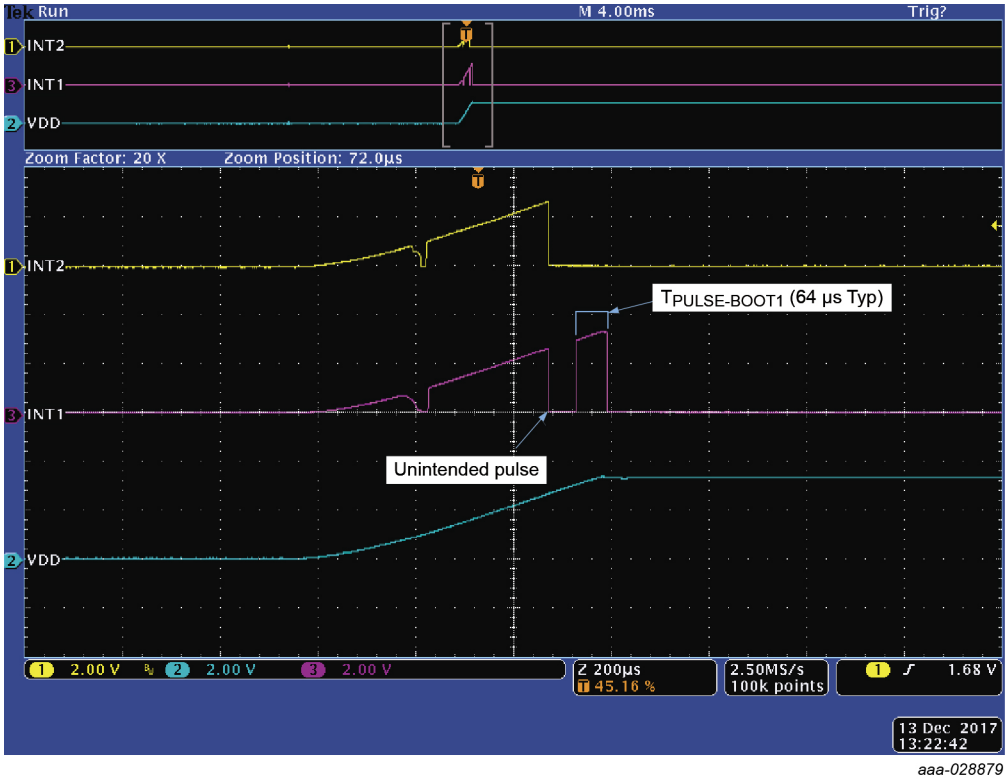


Figure 7. Unintended pulse during POR (BT_MODE=GND)

POR when BT_MODE = VDD

Upon POR, the boot pulse is issued for $T_{PULSE-BOOT2}$ ms upon completion of the boot phase (see Figure 6). However, an unintended pulse approximately 10 µs in duration occurs just before the starting edge of the $T_{PULSE-BOOT2}$ pulse, as shown in Figure 8.

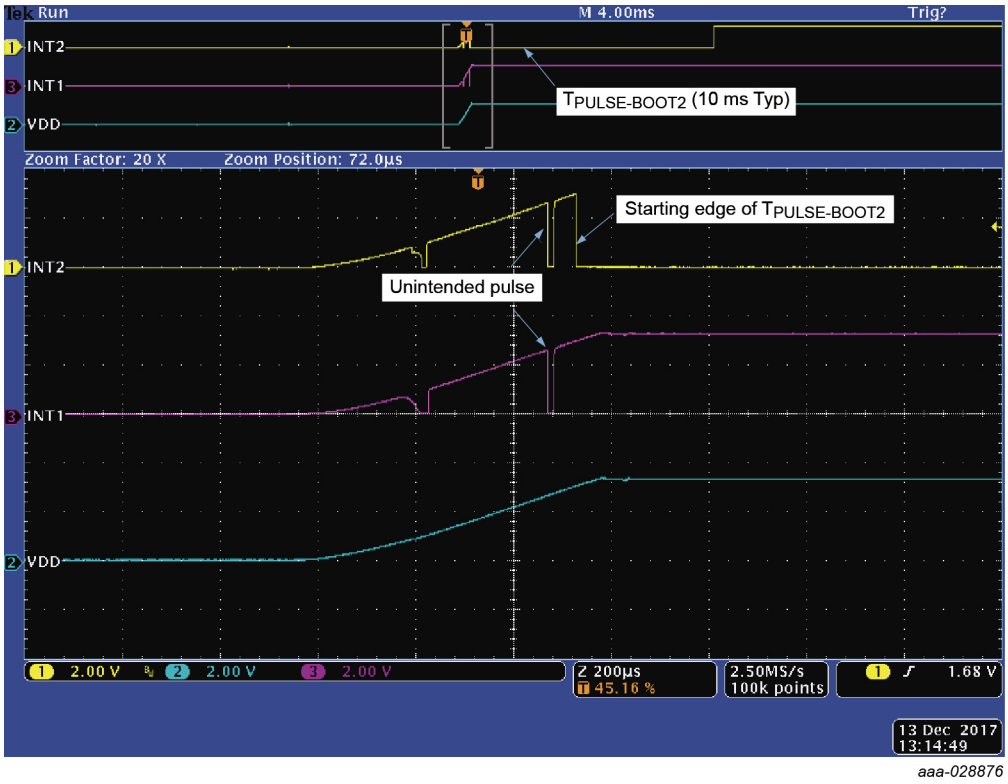


Figure 8. Unintended pulse during POR (BT_MODE = V_{DD})

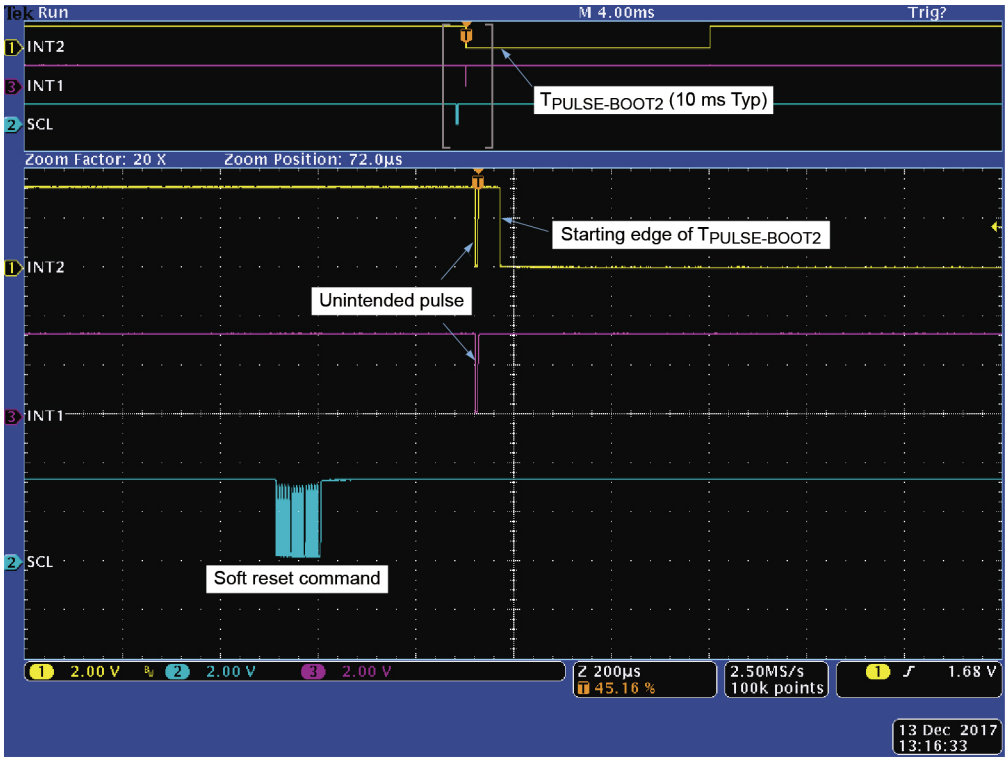
Soft reset when BT_MODE = VDD

Upon issuing a soft reset command through setting the RST bit in SENS_CONFIG1 (address 15h) register (see Table 8), the boot pulse is issued for $T_{PULSE-BOOT2}$ ms upon completion of the boot phase (see Figure 6). However, an unintended pulse approximately 10 µs in duration occurs just before the starting edge of the $T_{PULSE-BOOT2}$ pulse, as shown in Figure 9.

Note: *No unintended pulse is seen on issuing a soft reset command when BT_MODE = GND and when .setting the RST bit in the SENS_CONFIG1 register (see Figure 10).*

Table 8. SENS_CONFIG1 register (address 15h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	RST	ST_AXIS_SEL[1:0]		ST_POL	SPI_M	FSR[1:0]		ACTIVE
Reset (BT_MODE = 0)	0	0	0	0	0	0	0	0
Reset (BT_MODE = 1)	0	0	0	0	0	0	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W



aaa-028880

Figure 9. Unintended pulse during Soft reset (BT_MODE=VDD)

aaa-028878

Figure 10. No unintended pulse during soft reset (BT_MODE=GND)

Workaround

Workaround 1

To avoid the unintended pulse from being mistaken for a boot pulse, the host MCU should measure the time between the starting and the ending edges of the pulse and validate it with boot pulse timing parameters. Typical boot pulse timing parameters for $T_{PULSE-BOOT1}$ is 64 µs and $T_{PULSE-BOOT2}$ is 10 ms.

Workaround 2

Alternatively, if the host MCU enables the sensor VDD supply under software control, or if the boot sequence is initialized through a soft-reset command, configure the host software to ignore the first edge triggered interrupt corresponding to the unintended boot pulse event (rising edge when BT_MODE = GND or falling edge when BT_MODE = VDD).

Fix plan

None.

4.3 E3: FIFO burst read operation error using I2C interface

Introduction

FXLS8962AF has a 32-sample FIFO buffer that can hold up to 144 bytes of data (32 12-bit X, Y, Z data triplets) at a time.

The FIFO buffer is intended for saving power by allowing the host MCU to read out multiple samples using a burst read operation.

Problem

In I^2C mode, a burst read attempt for three or more samples results in incorrect data beginning with the third sample. For example, a burst read attempt for 144 bytes of data results in unique and correct data for samples 1 and 2, but incorrect data starting from sample 3. The data returned starting with sample 3 is a replica of sample 2 (see Table 8), due the FIFO read pointer not incrementing as expected and continuing to point to sample 2.

Additionally, as a result of the FIFO read pointer not incrementing, the buffer sample counter BUF_CNT[5:0] in BUF_STATUS register (0Bh) does not decremented as expected.

Table 9. Example of incorrect data starting at sample 3 (burst read - I^2C)

Sample No.	X	Y	Z	Buffer count (BUF_CNT)
1	29	34	1024	31
2	23	32	1019	31
3	23	32	1019	31
4	23	32	1019	31

Sample No.	X	Y	Z	Buffer count (BUF_CNT)
5 and so on up to 32	23	32	1019	31

Workaround

Workaround 1 (preferred)

Use SPI interface.

Workaround 2 (interface restricted to I^2C)

Limit the burst read operation to a discrete sample frame block. For example, read the 32-sample FIFO as 32 one-sample frame (6 bytes) burst reads. In this case, since each burst read consists of one sample, the FIFO read pointer properly increments automatically to the next sample frame through all samples. Additionally, the buffer counter BUF_CNT[5:0] in BUF_STATUS register (0Bh) properly decrements as each discrete sample frame is read. Thus, all samples are read as intended (see Table 9), and the undesirable behavior is avoided.

Table 10. Reading 6 bytes of data (1 sample at a time)

Sample No.	X	Y	Z	Buffer count (BUF_CNT)
1	29	34	1024	31
2	23	32	1019	30
3	19	22	1020	29
4	18	27	1027	28
5 and so on up to 32	19	30	1030	27

Fix plan

None.

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