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MPC577xK STCU Online BIST Configuration

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1 Introduction

This document describes the MPC577xK Self-Test Control Unit 2 (STCU2) configuration for online Built-In Self-Test (BIST). This BIST is destructive, meaning that the user must ensure that the application is not dependent on the MCU before the BIST is initiated by software configuration of the STCU2 module. The purpose of online BIST is to execute a comprehensive test of memory and module logic without the start-up time constraint that applies to offline (startup) BIST. The configuration for offline BIST is detailed in a separate document that is numbered EB823.

To configure online BIST testing via software an IPS (peripheral bridge) interface allows access by the device CPU(s) to the STCU2 registers. Software must configure the device correctly in preparation for executing the online tests and then configure the STCU2 registers for execution of the tests. After completion of the BIST, a global functional reset will be triggered by the STCU2 and the device will restart. After restart software can check the results of the BIST reported through a number of STCU2 registers.

This engineering bulletin details device specific configuration settings for executing online BIST and is intended to be used in close conjunction with the device reference manual. For detailed information on how to apply these settings to the device and instructions on how to use the STCU2 to execute

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online BIST please see the device reference manual, specifically the chip specific section STCU configuration and the Self-Test Control Unit (STCU2) chapter.

2 STCU2 Online BIST configuration summary

- Overall coverage level: ASIL-D
- PLL0: 60.72 MHz with IRCOSC[1] as reference
- LBIST
  - Logic partitions 0-7, tested in parallel and sequentially
  - Coverage/Algorithm: 90% Stuck-at
  - Execution time: 11.3 ms (+/- 8% according to IRC trim tolerance)
- MBIST
  - Memory partitions 0-91, tested in parallel
  - Coverage/Algorithm: Full test (including PMOS)
  - Execution time: 32.3 ms (+/- 8% according to IRC trim tolerance
- 650 mA maximum current draw of VDD_LV_CORE

3 LBIST

LBIST operates on the digital logic of the MPC577xK and uses scan test techniques to provide high coverage defect detection. The digital logic of the MPC577xK is segmented into eight individual LBIST partitions, as in the table below.

Table 1. LBIST module partitioning

Partition	Logic Partition
0	INTC, ENET
1	AIPS1, PBRIDGE_1 peripherals
2	RCCU, Check core
3	Core0, Core1
4	MEMU, Flash, PRAM_CTRL, PFLASH_CTRL
5	AIPS0, PBRIDGE_0 peripherals
6	SPT, WGM, PDI, CTE
7	MC_ME, JTAG

The default execution order of the LBIST partitions is illustrated in Figure 1. Note that LBIST tests are executed both in parallel and sequentially, to provide an optimal balance of execution time and current consumption.

Phase 1	Phase 2	Phase 3	Phase 4
LBIST0	LBIST3	LBIST4	LBIST6
LBIST1		LBIST5	LBIST7
LBIST2			

Figure 1. LBIST execution order

1. This PLL0 frequency takes into account the possibility that the IRCOSC reference operates at -8% of the target frequency, according to the specified IRCOSC trim tolerance.

4 MBIST

MBIST is executed for each of the memories listed in the table below. The memories are segmented into 92 individual memory partitions, as shown in the table below. The MBIST configuration tests all MPC577xK memory partitions, 0-91, in parallel.

Table 2. MBIST memory partitioning

Partition Number	Memory Association
0	BAM_ROM
1	CAN_0
2	CAN_1
3	FLEXRAY DATA
4	FLEXRAY LUT
5	CAN_2
6	CAN_3
7	ETHERNET
8	CORE0 DCACHE
9	
10	
11	
12	CORE0 DTAG
13	CORE0 DTCM
14	
15	CORE0 ICACHE
16	
17	
18	
19	CORE0 ITAG
20	CORE1 DCACHE
21	
22	CORE1 DTAG
23	CORE1 DTCM
24	
25	CORE1 ICACHE
26	
27	CORE1 ITAG
28	CORE2 DCACHE
29	
30	CORE2 DTAG
31	CORE2 DTCM

Table continues on the next page...

Table 2. MBIST memory partitioning (continued)

Partition Number	Memory Association
32	
33	CORE2 ICACHE
34	
35	CORE2 ITAG
36	DMA
37	PRAM0
38	
39	PRAM1
40	
41	PRAM2
42	
43	PRAM3
44	
45	PRAM4
46	
47	
48	
49	PRAM5
50	
51	
52	
53	PRAM6
54	
55	
56	
57	PRAM7
58	
59	
60	
61	RESERVED
62	
63	SPT
64	
65	
66	
67	
68	
69	
70	

Table continues on the next page...

Table 2. MBIST memory partitioning (continued)

Partition Number	Memory Association
71	
72	
73	
74	
75	
76	
77	
78	
79	SPT TWIDDLE
80	
81	
82	
83	
84	
85	
86	
87	CWG LUT
88	
89	
90	
91	MCAN

5 Preparing the MCU

- Only a single core should be active and used to configure the MCU for online BIST. Core 0 (e200z4) is the recommended core.
- The MCU should enter an operating mode which configures the e200z7 cores (core 1 and core 2) as disabled
- All peripherals should be disabled in this operating mode through relevant MC_ME PCTL registers

6 Online BIST clock settings

STCU2 online BIST must use PLL0 with or IRC as the PLL reference input to generate an internal 60.72 MHz clock. No external clocks are required to run online self-test. PLL0 must be configured by software to generate 60.72 MHz PLL0_PHI_CLK from the IRC reference input. Then, PLL0_PHI_CLK must be selected as the source of system clock using the system clock selector and as the source for each peripheral clock through the auxiliary clock selectors. Care must be taken to ensure that the system and auxiliary clock dividers are configured so that the clock frequency for each module just does not exceed the figures shown in the table Maximum system level clock frequencies in the device reference manual. Detailed information on how to configure the device for these settings can be found in the reference manual.

7 Configuring the STCU2

The software can now proceed with configuration of the STCU2 module before initiating the online BIST. This engineering bulletin serves only to communicate specific settings required for the online BIST, the STCU2 chapter in the reference manual describes the configuration sequence in full.

Any setting not specifically mentioned is considered flexible and it is the user's responsibility to configure correctly. The user must configure the settings not covered by this EB according to the reference manual and the desired online BIST operation.

7.1 Unlocking the STCU2 registers

The STCU2 registers have a runtime access protection mechanism that is described in detail in the STCU2 chapter in the reference manual. The STCU2 SK Code Register (STCU2_SKC) must be written with the pair of key values for online BIST.

Table 3. STCU2 SK Code register keys

Key Number	Value
1	0x753F924E
2	0x8AC06DB1

7.2 General configuration

Configure the BIST and STCU2 core clock for a 1:1 ratio with the system clock by setting the 'Logic, Memory Bist and STCU2 core CLK Clock configuration' field of the STCU2 Configuration Register to sys_clk (STCU2_CFG[CLK_CFG] = 0x0).

7.3 MBIST controller settings

- Configure all MBIST partitions to run concurrently by setting the STCU2 MBIST Control Registers 'Concurrent/ sequential mode' field to Concurrent mode (STCU2_MB_CTRLn[CSM] = 0x1). There is a control register for each of the 92 partitions, numbered 0 – 91 (STCU2_MB_CTRL0 - STCU2_MB_CTRL91).
- Select the full test algorithm for execution. Clear the 'MBIST MBU Test Enabled' field of the STCU2 Configuration Register (STCU2_CFG[MBU] = 0x0) and set the 'MBIST PMOS Test Enable' field (STCU2_CFG[PMOSEN] = 0x1).

7.4 LBIST configuration

Configure the delay between the starting points of each concurrent LBIST execution to 255 x 16 STCU2 Core clock cycles by setting the 'Delay LBIST run' field of the STCU2 Configuration Register to 0xFF (STCU2_CFG[LB_DELAY] = 0xFF).

7.5 LBIST controller settings

Each LBIST controller (each corresponding to a single partition) is configured with a dedicated STCU2 LBIST Control Register, numbered from 0 to 7 (STCU2_LB_CTRL0 to STCU2_LB_CTRL7).

- The ‘Shift Speed’ field for each LBIST controller should be set to Shift at full rate of STCU2 core clock (STCU2_LB_CTRLn[SHS] = 0x0).
- The ‘Scan enable OFF’ and ‘Scan enable ON’ fields for each LBIST controller should be set to 2 delay cycles (STCU2_LB_CTRLn[SCEN_OFF] = 0x2 and STCU2_LB_CTRLn[SCEN_ON] = 0x2).
- The ‘Capture window size’ fields for each LBIST controller should be set so that the Controller waits 8 shift cycles for capture to finish (STCU2_LB_CTRLn[CWS] = 0x8).
- The ‘Enable PRPG Loading’ field should be set so the Default LBIST value of the PRPG is used during LBIST run (STCU2_LB_CTRLn[PRPGEN] = 0x0).
- The ‘Past Flush Test’ field should be set to 0 so that the LBIST controller applies the 32 Flush Test patterns (STCU2_LB_CTRLn[PFT] = 0x0).

7.6 LBIST pattern count settings

The number of test patterns to be run must be set for each LBIST controller. This is set by the ‘Pattern counter stop’ field in each STCU2 LBIST PC Stop Register.

Table 4. Pattern count values

Partition	Register	PCS Value (decimal/hexadecimal)
0	STCU2_LB_PCS0	1600/0x640
1	STCU2_LB_PCS1	1750/0x6D6
2	STCU2_LB_PCS2	1650/0x672
3	STCU2_LB_PCS3	960/0x3C0
4	STCU2_LB_PCS4	1280/0x500
5	STCU2_LB_PCS5	1472/0x5C0
6	STCU2_LB_PCS6	896/0x380
7	STCU2_LB_PCS7	512/0x200

7.7 Expected LBIST MISR result settings

The expected MISR results for each LBIST partition (corresponding to the patterns detailed above) must be set. The values are set using the STCU2 On-Line LBIST MISR Expected high and low registers (STCU2_LB_MISRELSWn and STCU2_LB_MISREHSWn).

Table 5. Expected MISR results

Partition	Low (STCU2_LB_MISRELSWn) Value	High (STCU2_LB_MISRELHWn) Value
0	0xDC373C82	0xD25DE7D3

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Table 5. Expected MISR results (continued)

Partition	Low (STCU2_LB_MISRELSWn) Value	High (STCU2_LB_MISRELHWn) Value
1	0xFF0268C2	0xAAC83DCB
2	0xB4C01D4D	0xB0AF0FF1
3	0x1834FA73	0x7DB367B8
4	0xD494E189	0xBB65FB80
5	0x422951FD	0x830FE097
6	0xD6BEEC52	0x80B84E10
7	0x978B819F	0x5F91F9ED

These values are compared against the actual results of each LBIST partition. These results are provided by the STCU2 after test completion (following device reset) in the STCU2 On-Line LBIST MISR Read high and low registers (STCU2_LB_MISRRLSWn and STCU2_LB_MISRRHSWn).

8 Fault handling

A full explanation of the fault handling mechanisms provided on the MPC577xK is out with the scope of this engineering bulletin. However the intention of this section is to identify the mechanisms that the user must employ when dealing with the online BIST results.

After online BIST execution a functional reset will be issued to the system. When the device exits the reset sequence, software can determine that the reset was issued by the STCU2 post online BIST completion by checking the ‘Flag for self test completed’ in the Reset Generation Module ‘Functional’ Event Status Register (RGM_FES[F_ST_DONE] = 0x1).

Application software can then check the following registers to determine whether a fault has occurred:

- STCU2 error register: STCU2_ERR_STAT (will read all zeros if no fault occurred)
  - Recoverable Faults Status Flag: STCU2_ERR_STAT[RFSF]
  - Unrecoverable Faults Status Flag: STCU2_ERR_STAT[UFSF]

If a fault has occurred, the following STCU2 status registers should be read to determine the source of the fault:

Table 6. STCU2 Status registers

STCU Register Name	Register Description	Expected value if no fault after BIST execution
STCU2_MBSLSW	On-Line MIBST Status Low Register	0xFFFF_FFFF
STCU2_MBSMSW	On -Line MBIST Status Medium Register	0xFFFF_FFFF
STCU2_MBSHSW	On-Line MBIST Status High Register	0x0FFF_FFFF
STCU2_MBELSW	On-Line MBIST End Flag Low Register	0xFFFF_FFFF
STCU2_MBEMSW	On-Line MBIST End Flag Medium Register	0xFFFF_FFFF
STCU2_MBEHSW	On-Line MBIST End Flag High Register	0x0FFF_FFFF
STCU2_LBSSW	On-Line LBIST Status Register	0X0000_00FF
STCU2_LBESW	On-Line LBIST End Flag Register	0X0000_00FF

The STCU2 communicates fault information to the Fault Control and Collection Unit (FCCU) to indicate the occurrence of an unrecoverable fault and/or a recoverable fault failure during the BIST sequence. If a fault does occur, application software should check the FCCU status registers to see if a multi-bit error has occurred. The FCCU has dedicated fault input mappings for STCU BIST fault indications, as shown in table D.

Table 7. FCCU Non-Critical fault mapping for STCU module

FCCU Non-Critical Fault Number	Description
NCF[6]	Critical fault indication from STCU
NCF[7]	Non-critical fault indication from STCU
NCF[8]	Critical fault indication from STCU in case LBIST or MBIST control signals go to wrong condition during user application

Please refer to the FCCU module chapter in the device reference manual for more information. Please consult the MPC577xK Reference Manual and Safety Manual to ensure that fault handling is performed correctly in order to achieve required safety coverage levels.

8.1 PLL loss of lock during online BIST

If PLL loss of lock (LOL) occurs while MBIST or LBIST execution is in progress the BIST execution will be aborted with appropriate flags set in the STCU2 Error Register (STCU2_ERR_STAT).If the PLL LOL occurs during the small time window between the end of MBIST and before beginning of LBIST execution, then system clock reverts to the safe clock i.e. IRCOSC. There are two possibilities after this event: :

- If the LOL event occurs before the STCU state machine enters the “CHECK_PLL” state, then the STCU waits for the PLL to achieve lock again.
  - If PLL re-lock is achieved before the STCU watchdog timer expires, then the STCU state machine proceeds as normal. LBIST will be executed in the remainder of the time window until completion or until the STCU watchdog timer expires, whichever is earlier.
  - If the PLL re-lock is not achieved and the STCU watchdog timer expires, then the STCU exits self-test with a watchdog time-out reset.
- If the LOL event occurs after the “CHECK_PLL” state, then the LBIST run continues execution on IRCOSC clock and completes after a longer period of time. No STCU watchdog time-out reset happens.

9 Revision history

Table 8. Revision history

Revision	Description of changes
0	Initial release

1	• Editorial updates.
	• In STCU2 Online BIST configuration summary :
	  • Removed XOSC as option for PLL0 reference
	  • Modified PLL0 target frequency to account for IRCOSC tolerance
	• In Online BIST clock settings :
	  • Removed XOSC as option for PLL0 reference
	  • Modified PLL0 target frequency to account for IRCOSC tolerance
	• Added PLL loss of lock during online BIST.

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