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Migrating from the MC9S08GT16 to the MC9S08GT16A

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1 Introduction

This document explains the differences to be aware of when migrating from the MC9S08GT16 MCU to the MC9S08GT16A MCU. For the remainder of this document, GT16 will refer to the original non-“A” device and GT16A will refer to the newer “A” suffix device.

To the largest extent, the functionality and performance of the GT16 and the GT16A will be identical. However, there are several differences designers should understand when migrating to the GT16A.

2 Operating Temperature Range

The operating temperature range has been increased from –40°C to 85°C on the GT16 to –40°C to 125C on the GT16A.

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3 RAM Size

The GT16A has twice as much RAM as the GT16. The GT16 has 1024 bytes of RAM, ranging from addresses 0x0080 to 0x047F. The GT16A has 2048 bytes, ranging from addresses 0x0080 to 0x087F.

4 FLASH Programming Voltage

The GT16 has a minimum V_{DD} requirement of 2.1 V for erasing and programming the FLASH. The GT16A reduces this minimum V_{DD} requirement. On the GT16A, the FLASH can be programmed and erased across the full operating voltage range of the MCU, or 1.8 V to 3.6 V when the temperature is between –40°C and 85°C. Above 85°C, the minimum V_{DD} for programming is 2.1 V.

5 In-Application FLASH Programming

To program the FLASH memory from within the application, e.g., to use FLASH as data storage, a small programming routine must be copied into RAM and executed from RAM while the FLASH array is being programmed or erased. The number of steps that must be executed from RAM is reduced on the GT16A.

Refer to Figure 1, the FLASH program and erase flowchart. On the GT16, the steps starting with “write to FLASH to buffer address and data” and ending with “FCCF?” must all be executed from RAM.

On the GT16A, execution from RAM is not required until the step, “write 1 to FCBEF to launch command and clear FCBEF.” Execution from RAM still concludes with “FCCF?”.

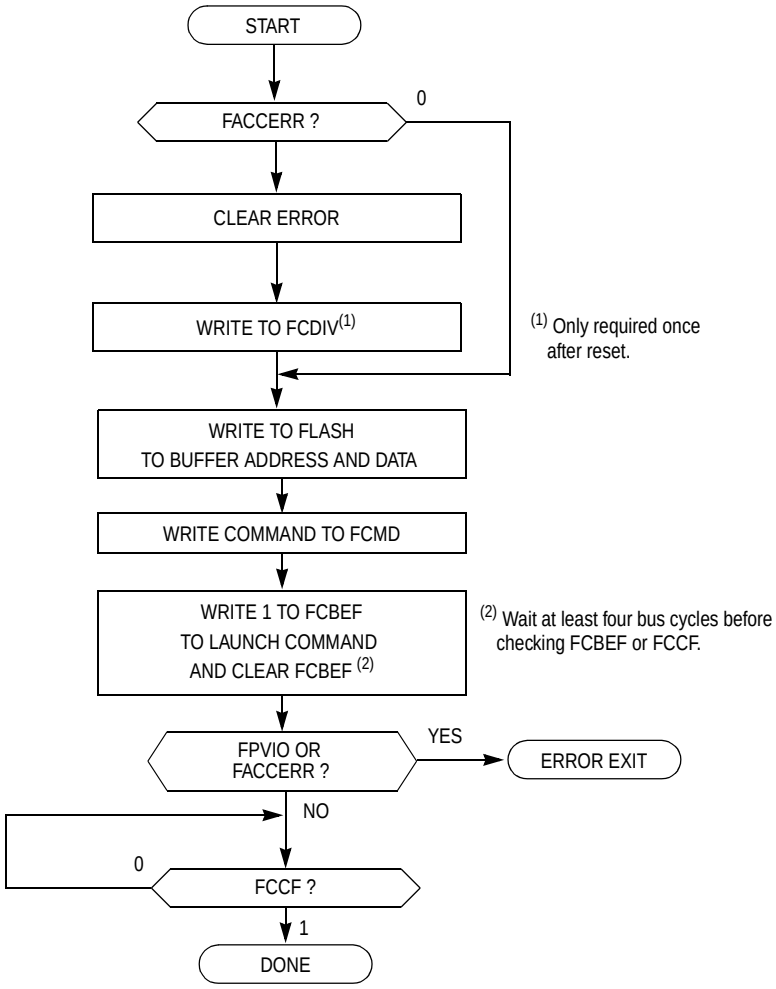

Figure 1. FLASH Program and Erase Flowchart

6 FLASH Block Protection

The GT16 FLASH block protection is limited to seven different options. Figure 2 shows the FLASH protection register (FPROT) for the GT16 and Table 1 shows the GT16 block protection options based on the FPROT register settings.

	Bit 7	6	5	4	3	2	1	Bit 0
FPROT	FPOPEN	FPDIS	FPS2	FPS1	FPS0	0	0	0

Figure 2. GT16 FLASH Protection Register (FPROT)

Table 1. GT16 FLASH Block Protection Settings

FPDIS	FPS2:FPS1:FPS0	Protected Address Range	Protected Block Size
1	x:x:x	none	0 bytes
0	0:0:0	0xFE00–0xFFFF	512 bytes
0	0:0:1	0xFC00–0xFFFF	1024 bytes
0	0:1:0	0xF800–0xFFFF	2048 bytes
0	0:1:1	0xF000–0xFFFF	4096 bytes
0	1:0:0	0xE000–0xFFFF	8192 bytes
0	1:0:1	0xC000–0xFFFF	16384 bytes
0	1:1:0	0xC000–0xFFFF	16384 bytes
0	1:1:1	0xC000–0xFFFF	16384 bytes

On the GT16A, the block protection has been modified to offer much more flexibility and resolution in the amount of FLASH protected. Figure 3 shows the GT16A's FLASH protection register (FPROT). The FLASH protect select bits has increased from 3 bits on the GT16 to 7 bits on the GT16A, creating 128 distinct settings. However, the way in which the protection works on the GT16A, there are effectively 33 actual protection options.

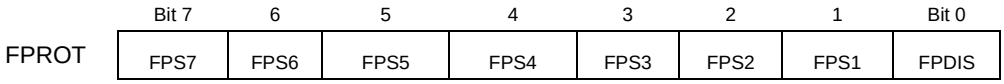

Figure 3. GT16A FLASH Protection Register (FPROT)

Table 2 shows just a few of the protection options available on the GT16A.

Table 2. Sample of GT16A FLASH Block Protection Settings

FPDIS	FPS[7:1]	Protected Address Range	Protected Block Size
1	xxxxxxx	none	0 bytes
0	1111111	none	0 bytes
0	1111110	0xFE00–0xFFFF	512 bytes
0	1111101	0xFC00–0xFFFF	1024 bytes
0	1110000	0xE200–0xFFFF	7584 bytes
0	1100100	0xCA00–0xFFFF	13824 bytes
0	1100000	0xC200–0xFFFF	15872 bytes
0	1011111	0xC000–0xFFFF	16384 bytes
0	0000000	0xC000–0xFFFF	16384 bytes

When protection is enabled by clearing FPDIS, FPS[7:1] form the seven most significant bits of the address of the last *unprotected* byte. The nine least significant bits are read as 0x1FF. Therefore, to protect

addresses 0xCA00–0xFFFF, write 0xC8 to FPROT register. This forms the last unprotected address as 0xC9FF.

	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
FPROT	FPS7	FPS6	FPS5	FPS4	FPS3	FPS2	FPS1	1	1	1	1	1	1	1	1	1
0xC9FF	1	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1

Figure 4. FPROT Example for protecting addresses 0xCA00–0xFFFF.

This new protection method is useful for protecting the main user program area while leaving a smaller section of memory available for data storage.

7 FLASH Security: Backdoor Access Key

On the GT16, when FLASH security is enabled and the KEYACC bit is set, the FLASH memory cannot be read. Therefore the eight backdoor key bytes cannot be stored in FLASH; instead, they must be loaded into and read from RAM.

On the GT16A, this restriction is eliminated. The eight backdoor key bytes can be stored in and read from FLASH.

8 Illegal Address Reset

The GT16 does not support illegal addresses. Reading a reserved memory location will return an indeterminate value. Writing to a reserved location will result in an indeterminate value being stored at that location. Executing code from a reserved location will result in a random opcode execution.

The GT16A supports illegal address resets for any address labeled “unimplemented.” Any read, write or execution access to an unimplemented address will result in a chip reset. The ILAD bit in the system reset status (SRS) register will be set after this reset occurs. Addresses labeled “reserved” will not cause an illegal address reset.

On the GT16A, the unimplemented addresses are from 0x0880 to 0x17FF and from 0x182C to 0xBFFF.

9 Internal Clock Generator: High Gain Oscillator Option

The GT16 has only a low power external oscillator, designed for the low current consumption. The GT16A adds a second external oscillator option: a high gain external oscillator, which provides improved noise immunity in the oscillator circuit. The low power oscillator is also available for power sensitive applications.

This new oscillator option is selected by a new control bit in the ICG control register 1 (ICGC1): the HGO bit. HGO is bit 7 of the ICGC1 register, formerly an unimplemented bit that always read 0. The reset value is 0, which selects the low power oscillator option. This reset value is consistent with the GT16 external oscillator.

Setting HGO to 1 selects the high gain external oscillator, which increases the voltage swing across the external crystal or resonator, making it more immune to external noise.

The values of the feedback and series resistors for the external oscillator will be different in most cases between HGO = 0 and HGO = 1. Consult the ICG DC Electrical Specifications table in the MC9S08GT16A data sheet for the proper values.

10 Internal Clock Generator: Low Power Oscillator Maximum Frequency

On the GT16, the external oscillator's maximum frequency is 10 MHz when in FEE mode and 16 MHZ when in FBE mode.

On the GT16A, when HGO = 1, the same maximum frequencies apply. However, when HGO = 0, the maximum frequency is 8 MHz in FEE and FBE modes.

11 Internal Clock Generator: Loss-of-Clock Disable Option

The ICG module has a clock monitor that will generate a loss-of-clock signal when either the reference clock or the DCO clock does not meet minimum frequency requirements. This signal is used to generate either a reset or an interrupt depending on the settings in the ICGC2 register.

On the GT16, this clock monitor cannot be turned on or off by the user. The on/off status of the clock monitor is determined by the state of the ICG module.

On the GT16A, an option has been added to allow the user to disable the clock monitor. A new control bit, LOCD, has been added to the ICGC1 register at bit position 1 (formerly an unimplemented bit). The reset state is '0', which enables the clock monitor. Setting LOCD = 1 will disable the clock monitor and thereby eliminate any loss-of-clock resets or interrupts.

The advantage of disabling the clock monitor is the reduction of the current draw of the ICG module. Disabling the clock monitor when running in stop3 mode with a low range (e.g., 32-kHz) external oscillator enabled will save approximately 9 µA of current. With LOCD = 0 in this configuration, the stop3 I_{DD} is about 14 µA. When LOCD = 1 in this configuration, the stop I_{DD} is about 5 µA.

For the best combination of power conservation and system protection, Freescale recommends setting the LOCD=0 whenever the MCU is in active run mode and then setting LOCD=1 just before entering stop3 mode when OSCSTEN=1. If OSCSTEN=0, then the LOCD bit will not make a difference in the stop3 current.

12 System Device Identification Registers

The system device identification registers (SDIDH and SDIDL) have a new value. On the GT16, the 12-bit value is 0x002. On the GT16A, the 12-bit value is 0x00D.

13 Eliminated Errata

Several errata from the GT16 have been addressed on the GT16A. Consult the document MSE9S08GB60_3L31R for details on each errata. Consult the document MSE9S08GT16A_2M70C for the most up-to-date errata list for the GT16A.

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