TEA2376DT

Digital configurable interleaved PFC controller

Rev. 1 — 10 August 2023   **Product data sheet**

1   General description

The TEA2376DT is a digital configurable two-phase interleaved PFC controller for high-efficiency power supplies. The PFC operates in discontinuous conduction mode or quasi-resonant mode with valley switching to optimize efficiency. The TEA2376DT enables the building of an interleaved power factor controller, which is easy to design with a low external component count.

The TEA2376DT is available in a low profile and narrow body-width SO14.

The digital architecture of the TEA2376DT is based on a high-speed configurable hardware state machine ensuring reliable real-time performance. To meet specific application requirements, many operation and protection settings of the PFC controller can be adjusted by loading new settings into the device with I^2C during power supply development.

For a high power factor and a low THD, input current shaping is used. A notch filter allows a faster transient response by suppressing the mains frequency component in the regulation loop, while maintaining a low THD.

For low-load operation with good efficiency, phase shedding and burst mode operation are included. To meet the efficiency and standby power regulations of Energy Star, the Department of Energy, the Eco-design directive of the European Union, the European Code of Conduct, and other guidelines, the power consumption of the IC is reduced in burst mode operation.

The TEA2376DT contains many protections, like internal and external overtemperature protection (OTP), overcurrent protection (OCP), dual overvoltage protection (OVP), inrush current protection (ICP), pin open, pin short protection, and phase fail protection. The protections can be configured independently and using programmable parameters.

The TEA2376DT allows an easy to design, highly efficient, and reliable interleaved PFC, for power levels up typically to 1000 W[1].

---

1   For high switching frequency and high power applications, IC package thermal limitations require attention.

2 Features and benefits

2.1 Distinctive features

• Interleaved PFC controller in an SO14 package
• Programmable phase shedding and burst mode operation
• Dual output over voltage protection
• Inrush current protection
• High power factor (PF) and low total harmonic distortion (THD), also at high input voltages
• Many parameters can be configured during evaluation with the use of a user-friendly graphical user interface (GUI)
• Good phase control over full input voltage range
• Low audible noise
• Power good output and a burst mode input pin
• Live monitoring of (internal) IC status values over time with the help of the user-friendly GUI similar to oscilloscope reading
• I^{2}C communication while in operation

2.2 Green features

• Valley/zero voltage switching for minimum switching losses
• High efficiency from high load to medium load and low load by phase shedding and burst mode operation

2.3 Protection features

• Protections can independently be set to latched, safe restart, or latched after several attempts to restart
• Dual output overvoltage protection (OVP)
• Supply undervoltage protection (UVP) and overvoltage protection (OVP)
• Internal and external overtemperature protection (OTP)
• Overcurrent protection (OCP)
• Inrush current protection (ICP)
• Brownin/brownout protection
• Open and short pin protection
• Coil short protection
• Output diode short protection
• Open control loop protection
• Phase fail protection

3 Applications

- HD and U-HD television
- Server
- Desktop and all-in-one PCs
- Gaming consoles
- High-power adapter
- 5G supplies
- Home audio

4 Ordering information
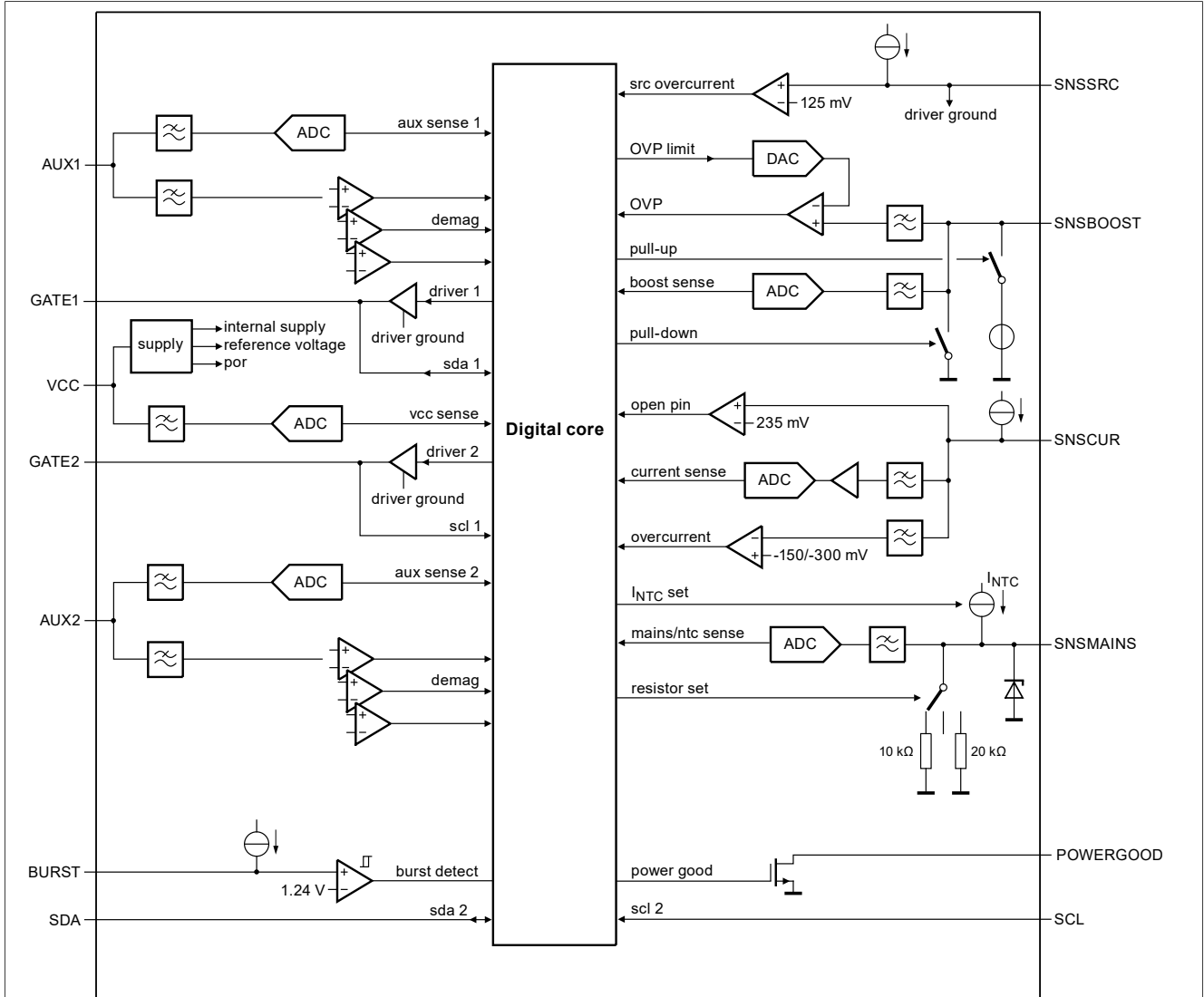
Table 1. Ordering information

Type number	Package			
	Name	Description		Version
TEA2376DT/1	SO14	plastic small outline package; 14 leads; body width 3.9 mm		SOT108-1

5 Marking

Table 2. Marking

Type number	Marking code
TEA2376DT/1	TEA2376DT

6 Block diagram

Figure 1. TEA2376DT block diagram

TEA2376DT   All information provided in this document is subject to legal disclaimers.

Product data sheet   **Rev. 1 — 10 August 2023**
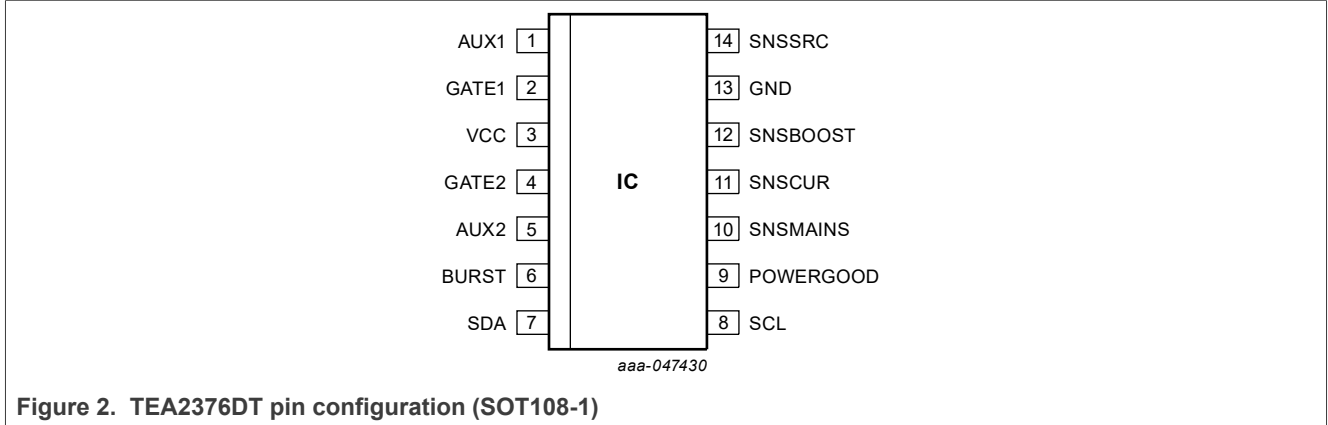
4 / 46

7 Pinning information

7.1 Pinning

Figure 2. TEA2376DT pin configuration (SOT108-1)

7.2 Pin description

Table 3. Pin description TEA2376DT

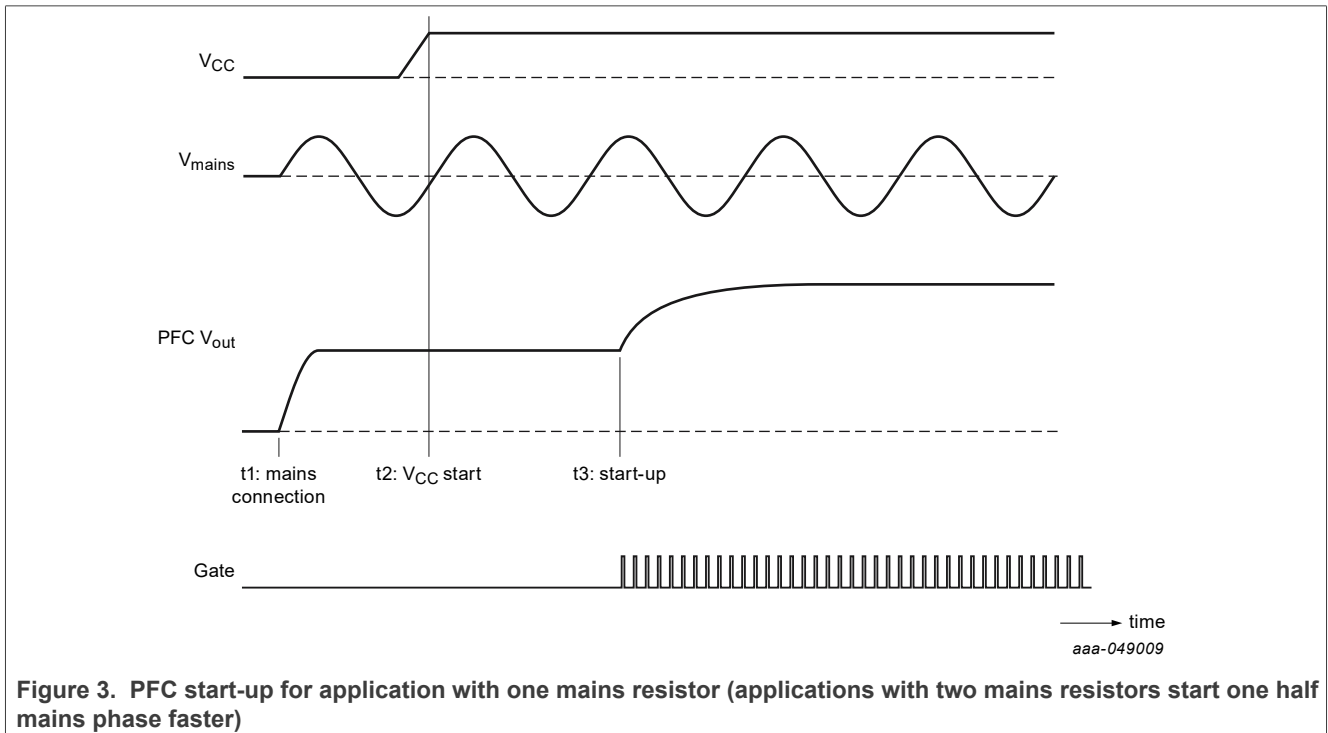| Symbol	Pin	Description
AUX1	1	sense input for auxiliary winding voltage 1
GATE1	2	gate driver output 1/I^{2}C data pin for programming, control, and status
VCC	3	supply voltage
GATE2	4	gate driver output 2/I^{2}C clock pin for programming, control, and status
AUX2	5	sense input for auxiliary winding voltage 2
BURST	6	burst control input
SDA	7	I^{2}C data pin for programming, control, and status
SCL	8	I^{2}C clock pin for programming, control, and status
POWERGOOD	9	power good output for downstream converter
SNSMAINS	10	sense input for mains voltage and external temperature
SNSCUR	11	sense input for inductor currents
SNSBOOST	12	sense input for boost voltage
GND	13	ground
SNSSRC	14	power ground and sense input for output diode short protection

8 Functional description

8.1 Start-up and supply voltage

The TEA2376DT is supplied via the VCC pin. If a voltage is supplied to the VCC pin, the IC first reads the multitime-programmable (MTP) parameters. When the (programmable) start-up voltage, $V_{start(VCC)}$, is reached and the input voltage measured via the SNSMAINS pin exceeds the brownin level (I_{bi}), the power converter starts up.

For a reliable start-up, the TEA2376DT starts on the second mains peak voltage above the brownin level. The PFC starts with a soft start and ramps the output voltage to the target level with a controlled slope to prevent audible noise.

8.2 PFC start-up

At start-up, the PFC output voltage increases according to an RC curve (see Figure 3).

Figure 3. PFC start-up for application with one mains resistor (applications with two mains resistors start one half mains phase faster)

At t1, the mains is connected and the PFC output voltage equals the peak voltage of the mains. At t2, the start-up voltage is reached on the VCC pin. At t3, the PFC starts switching and its output voltage increases according to an RC curve.

Increasing the PFC output voltage with an RC curve prevents that the OVP is triggered due to an output voltage overshoot. It also ensures that, at start-up, the on-time slowly increases from a minimum value to the regulation value, avoiding audible noise.

The RC time value can be programmed via the MTP.

8.3 Brownin and brownout

When the (filtered) mains-sense peak voltage exceeds the brownin level, the IC leaves the brownout state on the second mains peak. If no AC mains is detected, the brownout state is left after a timeout period when the (filtered) mains-sense peak voltage exceeds the brownin level. When the (filtered) mains-sense peak voltage drops to below the brownin level minus the hysteresis, $I_{bo(hys)}$, for at least the brownout delay time, $t_{d(det)bo}$, the IC enters the brownout state. When the PFC stops switching, a soft stop is made to prevent audible noise and overshoots on the rectified mains voltage caused by the energy in the differential mode filter inductor.

8.4 Overcurrent protection SNSCUR pin

The SNSCUR pin provides an overcurrent protection. The protection level is −150 mV for single-phase operation and −300 mV for two-phase operation ($V_{ocp(SNSCUR)}$). To prevent false triggering, a blanking time is included at the start of each switching cycle of either phase. The overcurrent protection circuit is also used for detection and protection for a shorted PFC coil condition.

8.5 Overcurrent protection SNSSRC pin

The SNSSRC pin can be connected to ground. It can also be used as an additional overcurrent protection by connecting it to an additional current sense resistor in series with the sources of the external MOSFETs. The protection level is 125 mV ($V_{ocp(SNSSRC)}$). To prevent false triggering, a blanking time is included at the start of each switching cycle of either phase. This overcurrent protection circuit is primarily intended for detection and protection for a shorted PFC output diode. Because the SNSSRC pin is also used as power ground for the internal gate drivers, the overcurrent signal is blanked when the gates of the external MOSFETs are discharged. To prevent damage to the IC due to inductive voltage spikes, a series resistor must be inserted between the SNSRC pin and the current sense resistor.

8.6 Gate drivers

The gate drivers can source 1.2 A ($I_{source(peak)}$) and sink 1.9 A ($I_{dch(GATEx)}$). To prevent disturbance of the internal signals connected to the ground pin, the discharge current from the external MOSFETs is through the SNSSRC pin. After the external MOSFET is turned off, the driver is connected to the ground pin to prevent that the driver signals cross couple via the SNSSRC pin.

8.7 Antialiasing filters

On the input of the internal ADCs, an antialiasing filter is added to restrict the bandwidth of the signal. The adding of the antialiasing filter complies with the Nyquist-Shannon sampling theorem over the band of interest.

8.8 Power good output

A power good signal that indicates if the output voltage of the PFC exceeds an MTP programmable minimum level, $V_{start(SNSBOOST)}$, is provided. The power good signal also gives an indication about if the controller is operating and not in a protection state. This output can be used to control a downstream converter that is connected to the output of the PFC or as signal to a microcontroller.

When the brownout is activated and the MTP programmable mask bit for this function is set, the power good signal is removed. It is also removed when $V_{SNSBOOST}$ drops to or is pulled to below a minimum level and the MTP programmable mask bit for this function is set.

The POWERGOOD pin is an open-drain output. The polarity of this signal is programmable.

TEA2376DT

Product data sheet Rev. 1 — 10 August 2023

7 / 46

8.9 Power factor correction (PFC) regulation

8.9.1 Power factor and THD

To achieve a high power factor (PF) and low total harmonic distortion (THD), the input current of the power supply must follow the mains input voltage. Because the filter capacitances cause a shift of 90° between the mains current and the mains voltage, the input filter disrupts PF and THD. To improve PF and THD, the average PFC current is in accordance with a shifted sine wave (see Figure 4).
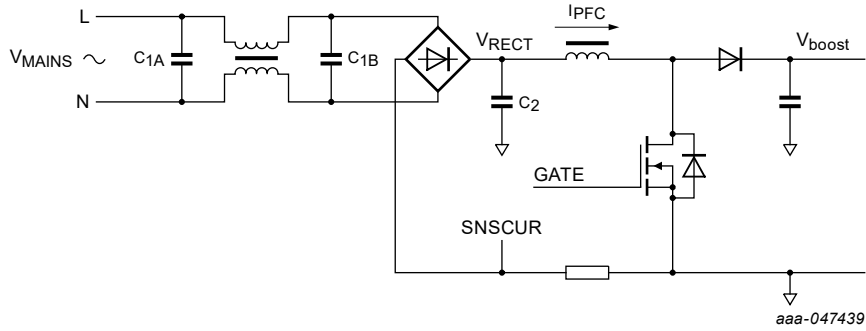
a. Circuit
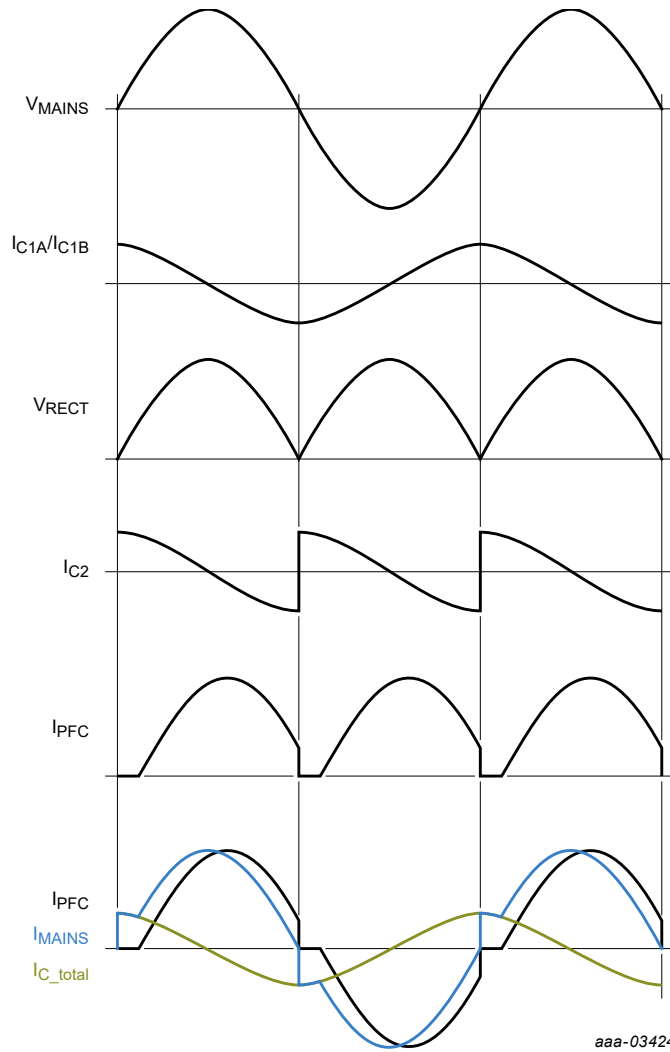
b. Timing diagram

Figure 4. Shifted sine wave

As the mains input current (I_{MAINS}) is the sum of the current through the filter capacitances (I_{C_total}) and the PFC current (I_{PFC}), the mains current approaches a sine waveform.

TEA2376DT

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Product data sheet

Rev. 1 — 10 August 2023

9 / 46

The output voltage control loop defines the amplitude of the shifted current sine wave. If more power is requested to the output, the amplitude of the shifted current sine wave increases.

If no AC mains voltage is detected, the PFC current is not sinusoidal. The voltage control loop controls it directly.

8.9.2 PFC switching frequency

The average PFC current is in accordance with a shifted sine wave. The PFC switching frequency is a function of this PFC current (see Figure 5), limited to a minimum frequency ($f_{sw(PFC)min}$) and a maximum frequency ($f_{sw(PFC)max}$). The minimum and maximum frequency can be set using an MTP parameter. The frequency the MTP sets is the maximum setpoint frequency the PFC can switch on. The actual switching frequency can be lower due to valley switching.
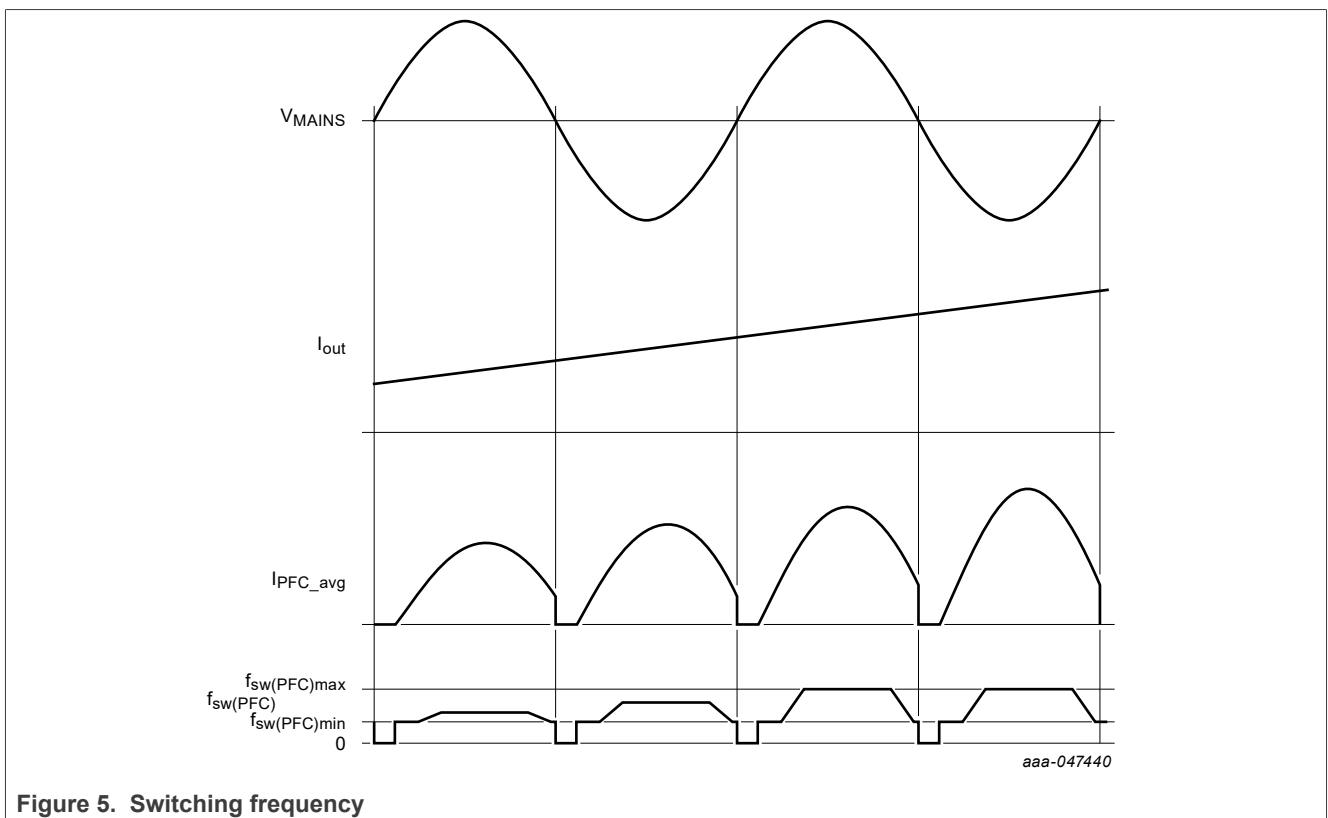

Figure 5. Switching frequency

At the zero crossing of a mains cycle, the PFC current is zero and the PFC does not switch. When the PFC starts switching, the current is initially low. The PFC switching frequency is at a minimum value. When the PFC current increases, the switching frequency increases as well until it reaches the maximum level.

Every switching cycle, the system calculates the PFC on-time such that its average current is in accordance with the desired PFC current. It also checks if the frequency is in accordance with the frequency curve as drawn above. The switching frequency control results in a high efficiency at low load, while keeping the ripple low at high load.

To minimize switching losses, each MOSFET is turned on when the voltage across the MOSFET is at its lowest value (valley switching). To achieve the lowest value, the voltage across the MOSFETs is monitored via the AUX pin inputs connect via a resistor to the auxiliary winding of the transformers.

TEA2376DT

Product data sheet

All information provided in this document is subject to legal disclaimers.

Rev. 1 — 10 August 2023

© 2023 NXP B.V. All rights reserved.

10 / 46

8.9.3 Frequency limitation

To optimize the transformer size and minimize switching losses, the PFC switching frequency is limited to $f_{sw(PFC)max}$.

To avoid audible noise, the minimum frequency is limited to $f_{sw(PFC)min}$.

To ensure correct control of the PFC MOSFET under all circumstances, the minimum off-time is limited.

The minimum and maximum frequency limitation values are adjustable.

8.9.4 Multimode operation (DCM/QR)

At the zero crossing of a mains cycle, the desired PFC current is low and the PFC switching frequency is at a minimum level in DCM mode. When the desired PFC current increases toward the peak of the mains, the PFC switching frequency increases as well. Depending on the load conditions, the system enters QR mode (see Figure 6).
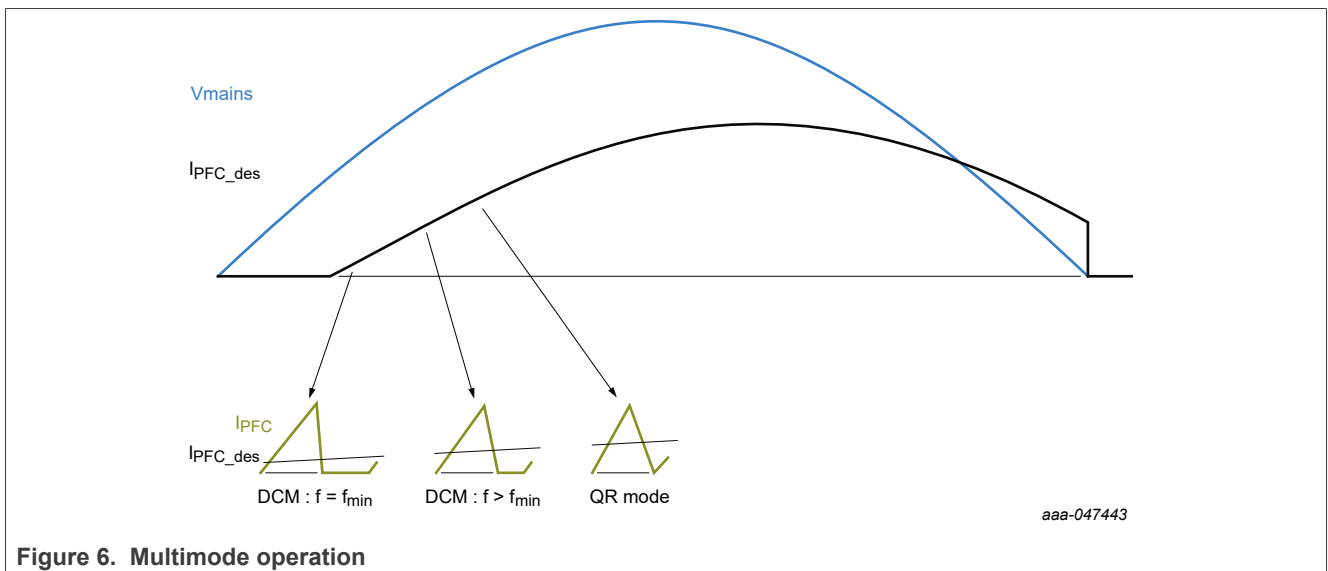
Figure 6. Multimode operation

To minimize switching losses, each MOSFET is turned on when the voltage across the MOSFET is at its lowest value (valley switching). To achieve the lowest value, the voltage across the MOSFETs is monitored via the AUX pin inputs connected via a resistor to the auxiliary windings of the transformers.

If the auxiliary winding voltage during the secondary stroke is too low (for example during start-up when the peak input voltage is close to the output voltage), the PFC can operate in continuous conduction mode (CCM) for a short time. CCM is allowed in this situation to avoid low-frequency switching operation, resulting in audible noise.

8.10 Output voltage regulation

The PFC output voltage is measured using a high-ohmic resistive divider connected to the SNSBOOST pin. To regulate the amplitude of the desired PFC current, the internal digital control loop compares the SNSBOOST voltage with an accurate trimmed reference voltage ($V_{reg(SNSBOOST)}$ at continuous operation).

The PFC current is measured via an external sense resistor connected to the SNSCUR pin. To ensure proper switching, the measured PFC current is internally filtered. The regulation system contains a voltage control loop and a current control loop.

8.10.1 Output voltage control loop

To stabilize the voltage control loop, a digital PI regulator is used. Figure 7 shows the transfer function of the PI controller.
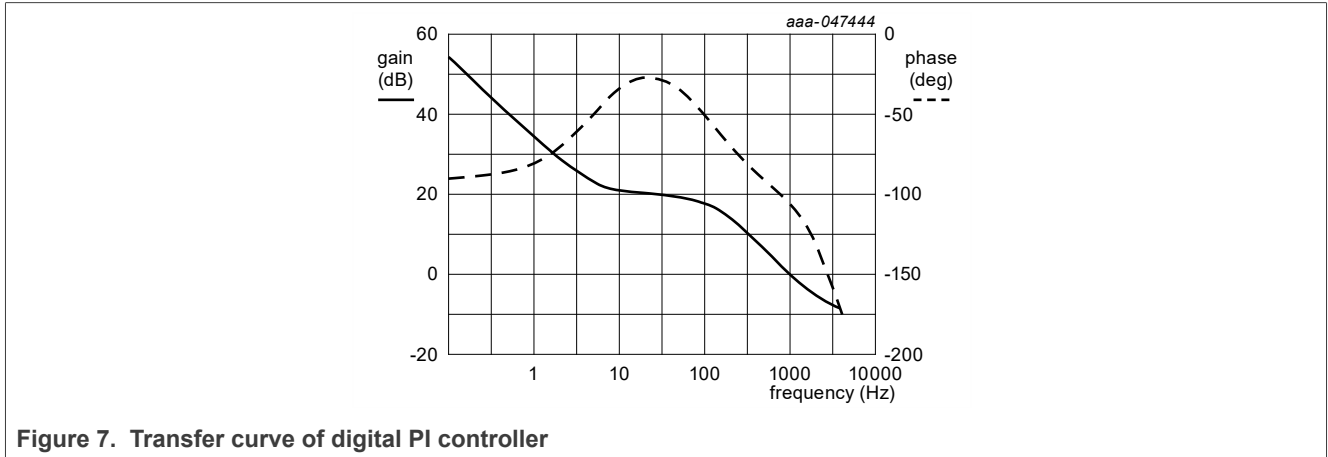

Figure 7. Transfer curve of digital PI controller

The zero at 5 Hz and the pole at 100 Hz are fixed in the design. To optimize the loop dependent on the implemented current sense resistor and output capacitor in the application, an MTP parameter can adjust the gain.

For a constant total loop gain, the mains input voltage information is included in the transfer function. An uncompensated transfer has a low bandwidth at low mains voltages, while at high mains voltages the mains harmonic reduction (MHR) requirements may be hard to meet.

The mains input voltage for the loop compensation is measured via the SNSMAINS pin.

To reduce overshoots and undershoots, the loop gain is increased (gm-increase) when the output voltage is outside the normal regulation range. If the output voltage exceeds the output overvoltage level minus 30 mV ($\Delta V_{gain(high)u}$) or the output voltage is below 2.5 V minus 200 mV (MTP selectable level $\Delta V_{gain(high)l}$), the loop gain is increased. The gain increase for overshoots and undershoots can be programmed independently. During start-up, the gain increase for undershoots is disabled until the regulation level has been reached. The gain increase for overshoots tracks the RC start-up curve.

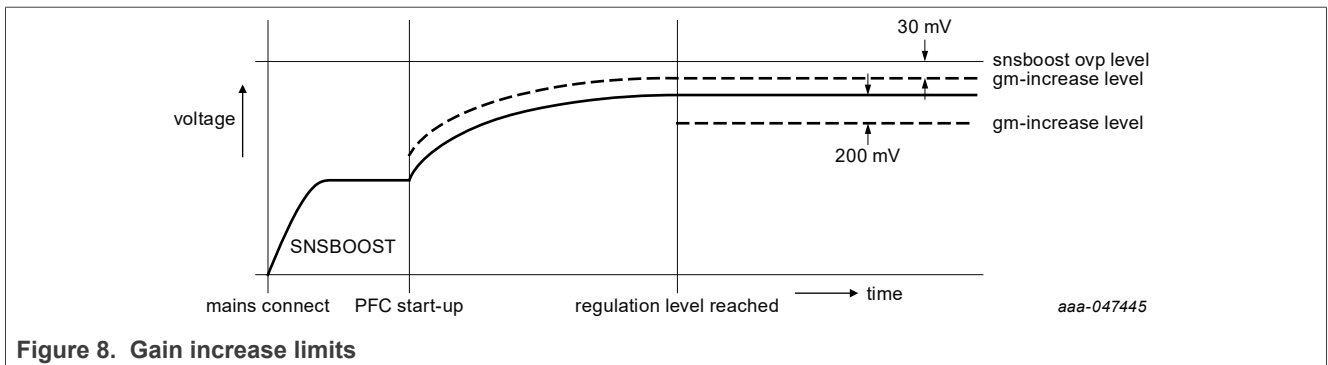An MTP setting can disable the gain increase for undershoots.

Figure 8. Gain increase limits

8.10.2 Notch filter

To improve the THD performance with good transient response, a digital notch filter is added to the voltage regulation loop. The notch filter automatically follows the measured mains frequency. The band stop is set at two times the measured mains frequency.
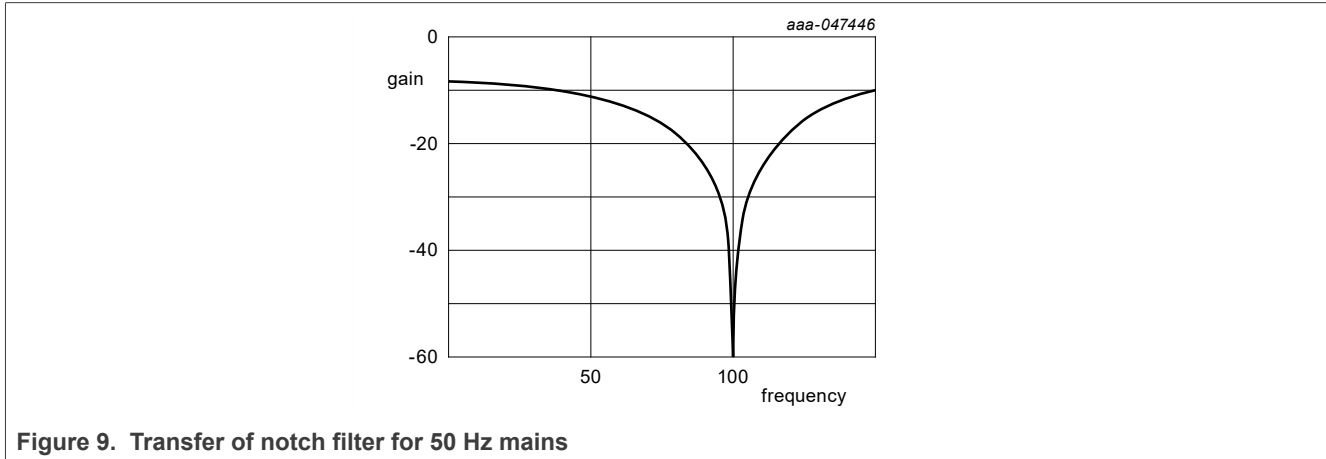

Figure 9. Transfer of notch filter for 50 Hz mains

An MTP memory setting can disable the notch filter.

8.11 Current control

To regulate the PFC current to the desired current from the output voltage regulation, a current control block is used which generates an on-time signal, t-on, for the converters. The actual PFC current is measured via the SNSCUR pin. An ADC digitizes it. The digital value is scaled such that it matches with the maximum desired PFC current without triggering an overcurrent protection. Assuming the current limiter does not limit the desired PFC current, a gain stage with an MTP selectable gain amplifies the difference between the actual and the desired PFC current. The gain must be adapted according to the sense resistor and the PFC inductor value. The desired PFC current can be limited in specific conditions, which are described Section 8.11.1.

The on-time control block also uses the information from the AUX pins for gain enhancement. The phase control block for the two phases adapts the t-on signal (see Section 8.13).
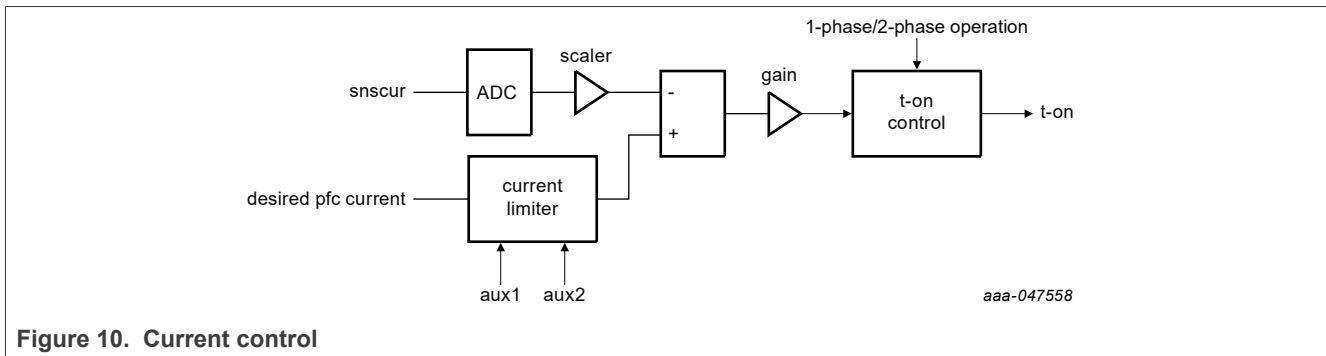

Figure 10. Current control

8.11.1 Current limiter

The current limiter can reduce the desired PFC current. When the input voltage becomes too high or when the input voltage is close to the output voltage, the current limit is automatically activated.

8.11.2 Input voltage-dependent current limit

The PFC input current limit depends on the momentary input voltage. It prevents that, when the input voltage is stepped from a low to a high value while the output voltage is out of regulation, the input power surges. The momentary input voltage is measured via the AUX1 pin. The input voltage at which the current reduction starts, can be set using an MTP parameter. The current limiter can also be disabled.

8.12 CCM operation

In CCM operation, the switching frequency is regulated to a minimum value and the phase of the two converter channels is fixed to 180 degrees. During CCM operation, the currents in the two converter channels may become unequal.

8.13 Phase control

To regulate the phase difference of the two PFC channels to 180 degrees, the period time and the switch-on moment of the MOSFETs are used. The error regarding the target of 180 degrees adjusts the on-time of the two phases. To be able to stay in regulation over the complete input voltage range, the error is compensated for the measured mains voltage. A selectable value can adjust the gain of the phase control. To keep the output power the same while regulating the phase difference, one on-time is reduced when the other on-time is increased.
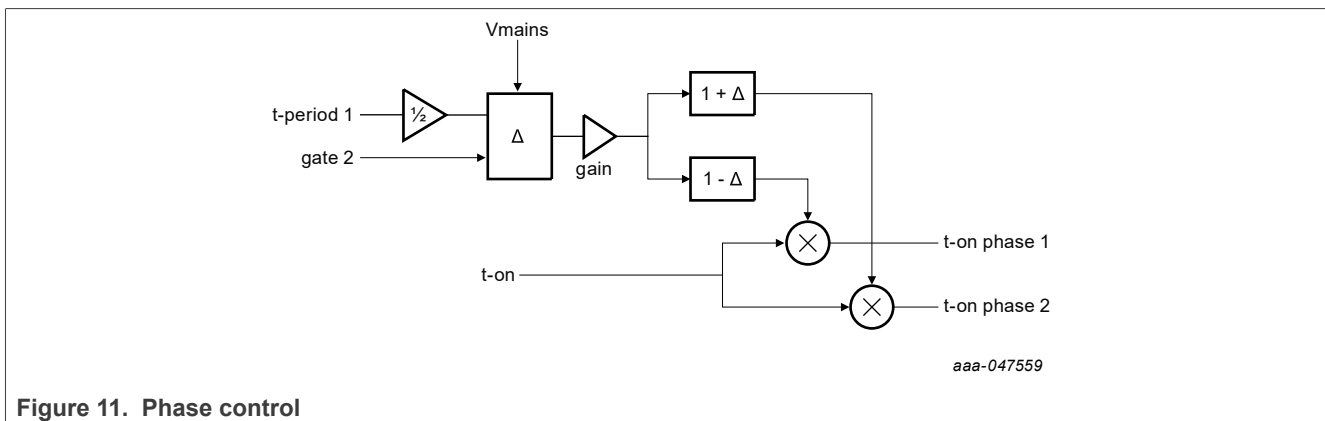

Figure 11. Phase control

8.14 Valley switching and demagnetization

When the TEA2376DT operates in discontinuous conduction mode or quasi-resonant mode, the PFC MOSFET is switched on after the transformer is demagnetized. To reduce switching losses and electromagnetic interference (EMI), the next stroke is started when the PFC MOSFET drain-source voltage is at its minimum value (valley switching). The demagnetization and valley detection are measured via the SNSCUR and the AUX1/AUX2 pins.

If no valley signal can be detected due to a low ringing amplitude after demagnetization on the AUX1 or AUX2 pins, valley switching is disabled temporarily. The amplitude of the ringing is measured every gate cycle on the AUX1 and AUX2 pins. The ringing amplitude can change due to damping or at different input voltages. When the ringing amplitude is low and drops below the high demagnetization voltage level ($V_{demag(high)}$), valley switching is disabled. If valley switching is disabled, the phase difference is forced to 180 degrees, which avoids the use of an unpredicted valley timeout. It also improves the noise insensitivity. Noise can cause incorrect phase control and audible noise. When the ringing amplitude on the AUX pin is higher than the high demagnetization level plus the hysteresis for 4 repetitive switching cycles, valley switching is enabled again. The high demagnetization level can be selected using MTP. To ensure continuous switching operation, a valley timeout is implemented.

8.15 Phase shedding

To improve efficiency, phase two can be programmed to switch off in light load conditions. For a stable switchover, the on-time of the MOSFET connected to pin GATE1 is adjusted when switching to single phase operation. When switching back to two-phase operation, the current control adjusts the on-time to ensure a constant mains input current.

To maintain a good phase margin of the regulation loop, the gain of the internal regulator is adapted, depending on single-phase or two-phase operation. To prevent that the output voltage drops when the load is increased, switching from single-phase operation to two-phase operation is done without a delay. To prevent a condition of continuous toggling between single-phase operation and two-phase operation if loads vary, hysteresis is added. Switching over from two-phase operation to single-phase operation is done with a delay, $t_{d(deact)GATE2}$. If the IC operates in AC mode and is locked to the mains, switchover from two phases to one phase is done at the first mains zero crossing after the delay. The phase shedding level can be programmed as a percentage of the full load (P_{act}/P_{max}). The hysteresis, $P_{act(hys)}/P_{max}$ is programmable. Phase shedding can also be programmed to be disabled.

Number of phases versus output power

Figure 12. Phase shedding
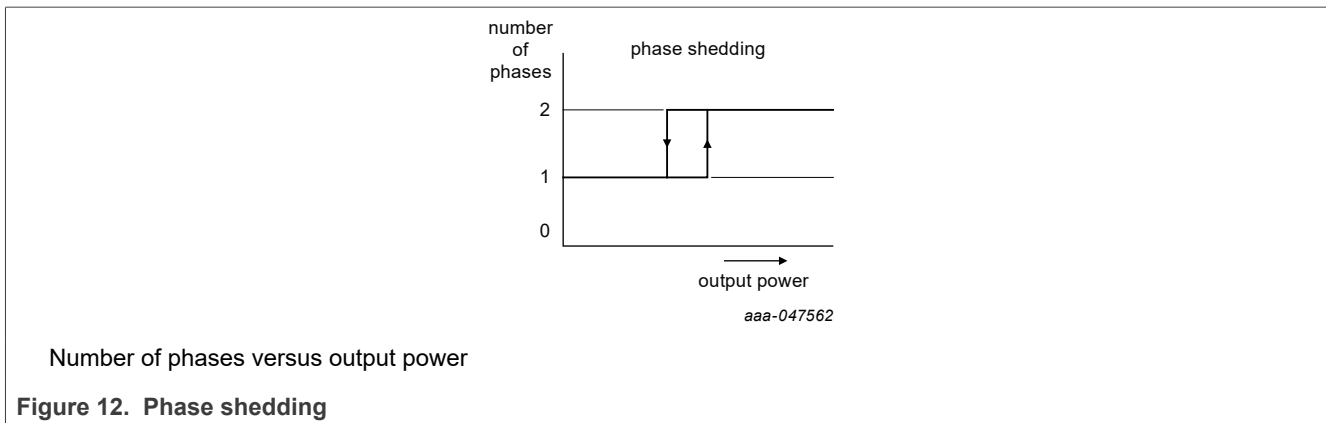
After switching from single-phase operation to two-phase operation, the phase of the two converters is not at 180 degrees initially. To regulate back to 180 degrees, several switching cycles for the phase control loop are required.

8.16 Burst mode

Burst-mode operation is included in the TEA2376DT to improve the light load efficiency.

The burst-mode power threshold can be programmed between 1.6 % and 25 % of the maximum power in 16 steps.

Three operation modes can be selected using MTP memory programming:

- Follow mode
- Ripple mode
- Autonomous mode

Burst mode can be programmed to single-phase operation only or independent of the phase-shedding mechanism.

Burst mode operation can be controlled externally via the VCC pin, the SNSBOOST pin, or the BURST pin, depending on the programmed settings.

To prevent irregular burst-mode operation with repetitive load steps in autonomous mode, the entering of burst mode can be delayed with a programmable delay.

TEA2376DT

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Product data sheet

Rev. 1 — 10 August 2023

15 / 46

To prevent audible noise, entering and exiting a burst active cycle is done with a soft start and a soft stop.

8.16.1 Burst mode with VCC pin control

If VCC-controlled burst mode is enabled in the MTP settings, the VCC pin voltage controls the burst mode. When the VCC pin voltage exceeds the programmable threshold voltage, $V_{burst(VCC)}$, continuous PFC switching is enabled. When the VCC pin voltage is below the threshold voltage, $V_{burst(VCC)}$, burst mode is entered. Burst mode with VCC control operates in follow mode or ripple mode.

8.16.2 Burst mode BURST pin control

If BURST pin-controlled burst mode is enabled in the MTP settings, the BURST pin voltage control the burst mode. When the BURST pin voltage exceeds 1.34 V, $V_{burst(u)}$, continuous PFC switching is enabled. When the BURST pin voltage is below 1.24 V, $V_{burst(l)}$, burst mode is entered. Burst mode with BURST pin control operates in follow mode or ripple mode. The polarity of the BURST input pin can be reversed using MTP programming. If the pin is left unconnected, a 100 nA ($I_{prot(BURST)}$) current source drives the pin to the continuous switching, nonburst mode state.

8.16.3 Follow mode burst operation

In follow mode, switching starts when the BURST input pin is made high[2] or the VCC pin voltage is increased to a value exceeding the burst threshold level.

The switching stops when the BURST input pin is made low or the VCC pin voltage is changed to a value below the burst threshold level and the SNSBOOST pin exceeds 2.475 V ($V_{reg(SNSBOOST)}$ at burst mode operation).

A downstream converter can control follow mode. When the downstream converter is in burst mode and switching starts, the TEA2376DT can also start switching by applying a burst signal from the downstream converter to it.

When the boost-recover MTP bit is set, switching also resumes if the SNSBOOST pin drops below a programmed voltage level.
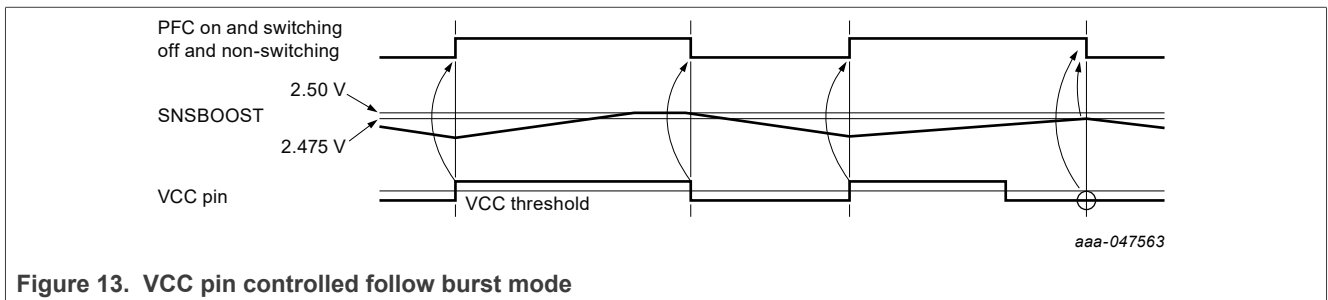

Figure 13. VCC pin controlled follow burst mode

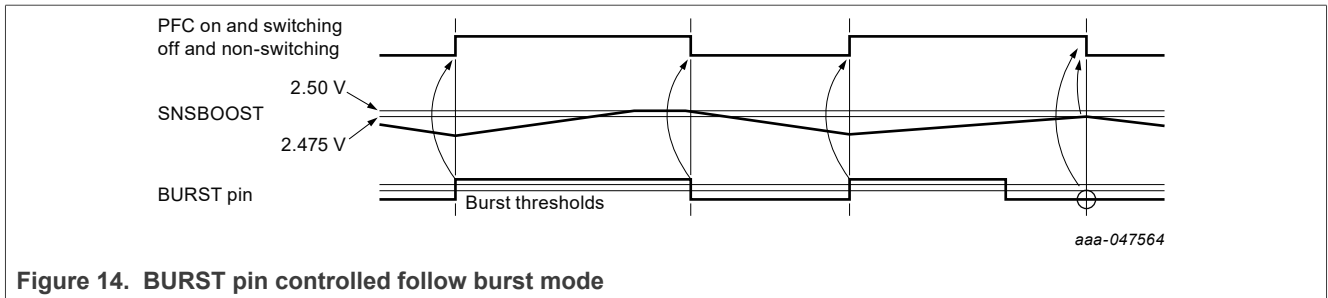2 The polarity of the BURST pin is programmable.

Figure 14. BURST pin controlled follow burst mode

8.16.4 Ripple mode burst operation

In ripple mode, switching starts when the BURST input pin is high[3] or when the VCC pin voltage is increased to a value exceeding the burst activation level and the voltage on the SNSBOOST pin drops to below the ripple level. The SNSBOOST ripple voltage amplitude can be selected using an MTP parameter.

In ripple mode, the switching stops when the BURST input pin is made low or when the VCC pin voltage is decreased to a value below the burst threshold level and the SNSBOOST pin exceeds 2.475 V. This stop criterion equals the follow mode.

When the boost-recover MTP bit is set, switching also resumes if the SNSBOOST pin drops to below a programmed voltage level.
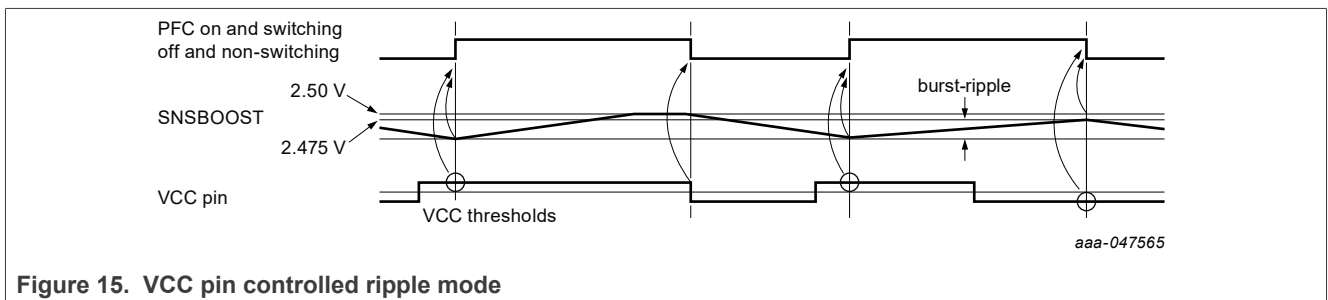

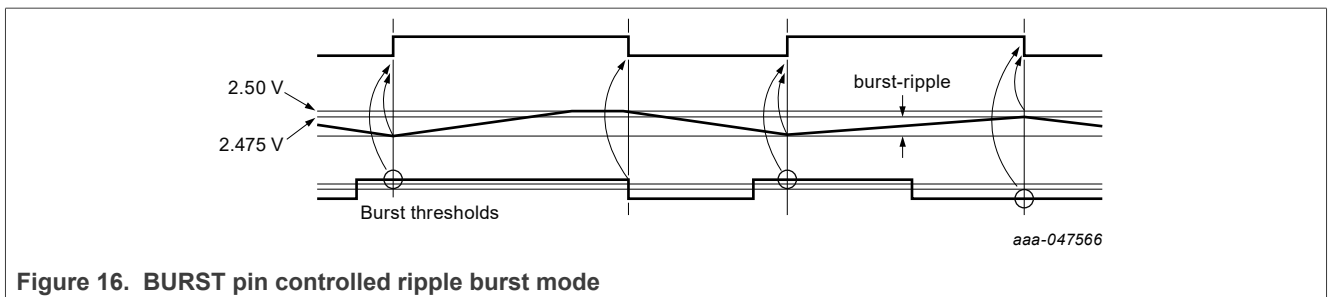**Figure 15. VCC pin controlled ripple mode**

Figure 16. BURST pin controlled ripple burst mode

3 The polarity of the BURST pin is programmable.

8.16.5 SNSBOOST pull-up

With the TEA19161 LLC converter, a defined pull-up of the SNSBOOST pin can also activate the ripple mode or the follow mode. The TEA19161 sources 6.4 µA to the SNSBOOST pin connection requiring a 100 kΩ lower resistor in the output voltage divider to the SNSBOOST pin. To distinguish between an output overvoltage and a pull-up, the SNSBOOST pin pull-up must be done within 245 µs ($t_{d(ovp)}$). When the voltage has dropped 75 mV (typically about 12 V PFC output voltage drop), the TEA19161 releases the SNSBOOST pin.

Figure 17. Follow mode and ripple mode SNSBOOST pull-up burst mode control
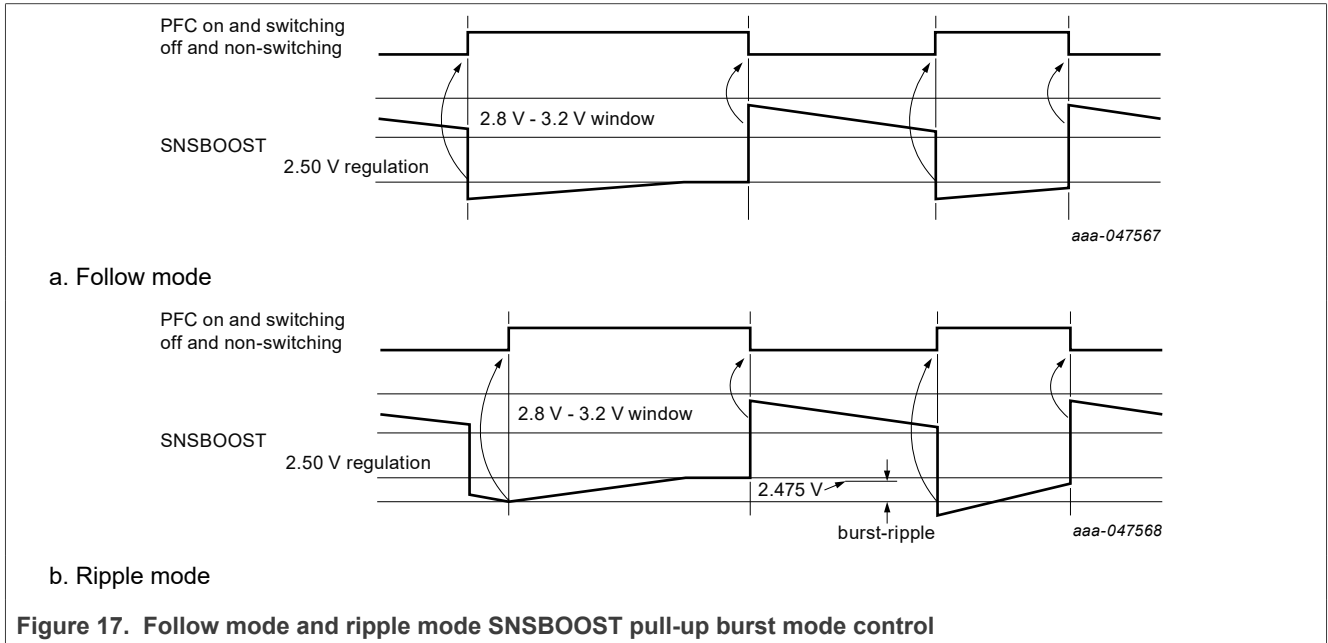
8.16.6 Autonomous mode burst operation

In autonomous burst mode, a burst cycle starts when the voltage on the SNSBOOST pin drops to below the ripple level that can be selected using an MTP parameter. Switching continues until the voltage on the SNSBOOST pin has reached 2.475 V and the output power is below the programmed burst level.

Figure 18. Autonomous burst mode operation
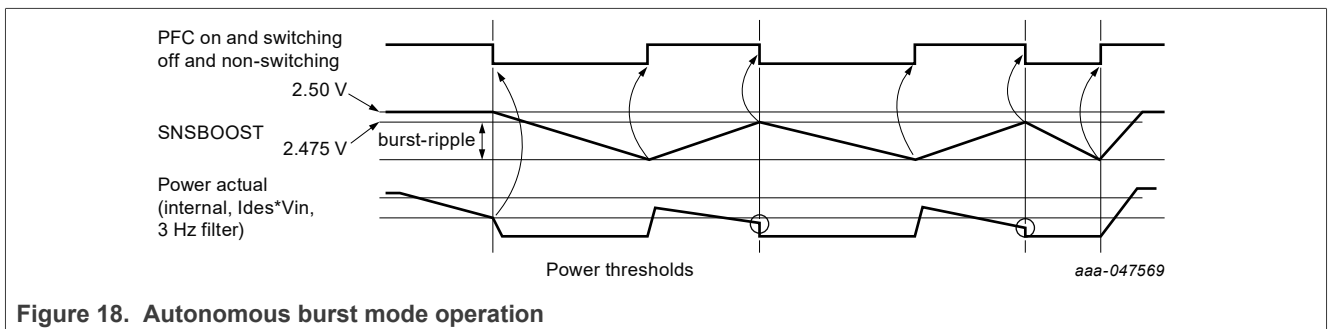
8.16.7 Burst mode soft start/soft stop

To reduce the audible noise, a soft start and a soft stop can be added to the PFC burst mode using an MTP setting. During a soft start, the average PFC current starts at zero and increases to the required level. A soft stop decreases the average PFC current from the regulation level down to zero. The rates of increase and decrease can be adjusted independently.

8.17 Protections

Table 4 gives an overview of the available protections.

Table 4. Protections overview

Protection	Description	Action	Protection register
General protections			
UVP VCC	undervoltage protection VCC	stop switching; restart when $V_{CC} > V_{start(VCC)}$	no
OVP VCC	overvoltage protection VCC	latched; latched after n restarts or restart when $V_{CC} < V_{ovp(VCC)}$ [1]	yes
MTP fail	reading of the internal MTP failed	continue reading until the data is valid; only checked once at start-up	yes
OTP int	internal overtemperature protection	latched; latched after n restarts or restart [1]	yes
OTP ext	external overtemperature protection	latched; latched after n restarts or restart [1]	yes
inrush	inrush current protection	PFC MOSFET switched off; PFC switching postponed	no
brownout-mains	undervoltage protection mains	restart when the mains voltage exceeds the brownin level	no
OVP mains	overvoltage protection mains	latched; latched after n restarts or restart [1]	yes
SCP SNSBOOST/fast disable	short-circuit protection/fast disable PFC	restart when $V_{SNSBOOST} > V_{start(scp)}$	yes
OVP SNSBOOST	overvoltage protection boost voltage	restart when $V_{SNSBOOST} < V_{reg(SNSBOOST)}$	yes
OVP AUX	overvoltage protection measured via AUX pins	latched; latched after n restarts or restart [1]	yes
maximum on-time	maximum on-time of the PFC MOSFET	PFC MOSFET switched off; continue operation	no
OCP SNSCUR	overcurrent protection SNSCUR pin	PFC MOSFET switched off; continue operation	no
OCP SNSSRC	overcurrent protection SNSSRC	PFC MOSFET switched off; continue operation	no
SCP coil	short-circuit protection PFC coil	latched; latched after n restarts or restart [1]	yes
SCP diode	short-circuit protection boost diode	latched; latched after n restarts or restart [1]	yes
SCP SNSCUR	SNSCUR pin is (partially) shorted to ground	latched; latched after n restarts or restart [1]	yes

Table 4. Protections overview...*continued*

Protection	Description	Action	Protection register
phase fail	phase fail protection (signals measured via AUX pins deviate from each other.)	latched; latched after n restarts or restart [1]	yes

[1]   Can be selected using an MTP parameter.

8.17.1 Undervoltage protection VCC (UVP VCC)

When the voltage on the VCC pin is below the undervoltage level $V_{uvp(VCC)}$, the PFC stops switching. When the VCC supply voltage exceeds its start level $V_{start(VCC)}$, the system restarts.

8.17.2 Overvoltage protection VCC (OVP VCC)

The voltage on the VCC pin is continuously monitored via an internal analog-to-digital converter.

To protect the application from being damaged, a first VCC overvoltage protection is implemented. When the voltage on the VCC pin exceeds the $V_{ovp(VCC)triggering\_delay}$ level for $t_{d(ovp)VCC}$, the overvoltage protection is triggered. The VCC overvoltage protection level and the delay time can be selected using an MTP parameter.

To protect the IC from being damaged, a second VCC overvoltage protection is implemented. When the voltage on the VCC pin exceeds the $V_{ovp(VCC)immediate\_triggering}$ level, the overvoltage protection is triggered without a delay.

8.17.3 MTP fail

Before starting up, the system reads the parameters from the internal MTP. If reading the MTP fails, the system retries after 500 ms. During this time, the PFC controller remains off. After 4 failed reads, a latched protection is triggered.

To restart the system after 4 failed MTP reads, a brownout/brownin cycle is required.

8.17.4 Undervoltage protection mains (brownout mains)

In the TEA2376DT, the mains measurement and external temperature are combined at the SNSMAINS pin (see Figure 19).

a. Circuit

b. Timing diagram

Figure 19. Mains and external OTP management
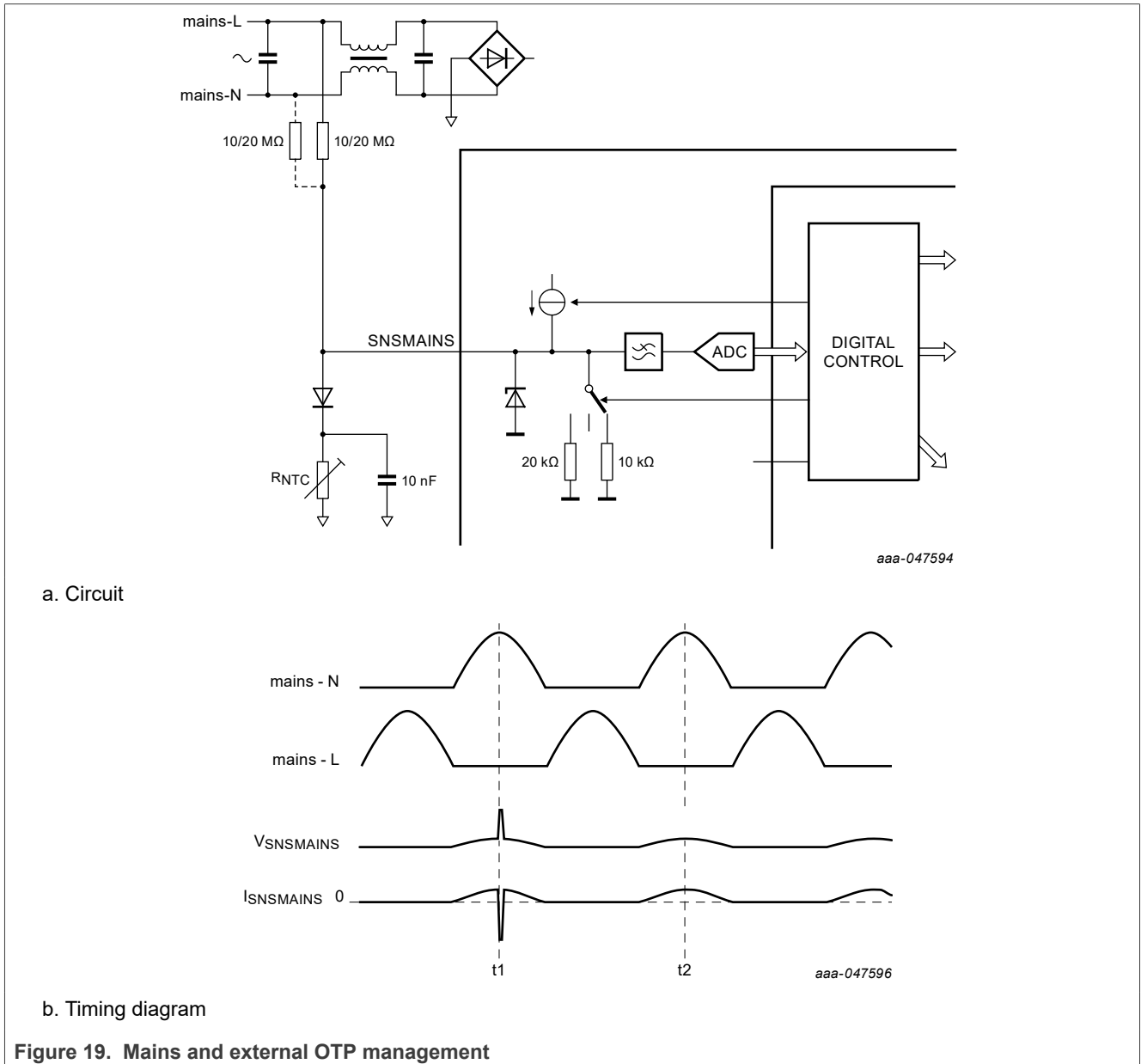
The SNSMAINS pin is connected to mains-L and mains-N via a 10 MΩ or 20 MΩ resistor. Alternatively, one resistor can be used connected to L or N. The value and the number of mains resistors must be set in MTP.

While measuring the mains voltage, the 10 kΩ/20 kΩ resistor is connected to the SNSMAINS pin to the external 10 MΩ/20 MΩ resistor as a resistive divider. Because the peak voltage on the SNSMAINS pin is below the forward voltage threshold of the (low leakage) diode connected to the NTC resistor, these components do not influence the mains measurement.

The TEA2376DT measures the SNSMAINS voltage via an analog-to-digital converter for brownin and brownout detection. The mains voltage amplitude, measured at t = t2, is stored and also used for the mains compensation.

To prevent that the PFC operates at very low mains input voltages, the PFC stops switching with a soft stop when the measured mains voltage drops to below the brownout level ($I_{bi} − I_{bo(hys)}$). When the mains voltage exceeds the brownin level (I_{bi}), the PFC restarts with a soft start. To avoid that the system is interrupted during a short mains interruption, a delay can be set before the brownout function is active. The levels and delay can be selected using MTP parameters.

8.17.5 Internal overtemperature protection (OTP int)

An accurate internal temperature protection is provided in the circuit. When the junction temperature exceeds the thermal shutdown temperature (T_{otp}), the converter stops switching.

The internal OTP can be programmed as either latched or safe restart.

8.17.6 External overtemperature protection (OTP ext)

To measure a temperature in the application with an external NTC, the SNSMAINS pin is connected to an NTC resistor in series with a (low leakage) diode. Using a low leakage diode like BAS416 is essential because the forward voltage drop of a fast recovery diode can be too low causing an inaccurate mains measurement.

During the NTC measurement, the 10kΩ/20kΩ resistor is disconnected from the SNSMAINS pin and the internal current source is switched on. After a settling time, the SNSMAINS pin voltage is measured via the analog-to-digital converter.

The actual value of the resistance of the NTC resistor is determined in a search loop:

If the NTC has a low resistance, the measured value will be low and for the next NTC measurement the current sourced from the SNSMAINS pin will be increased. If the NTC has a high resistance, the measured value will be high and for the next NTC measurement the current sourced from the SNSMAINS pin will be decreased. When the measured voltage is within the targeted range of 1.1 V to 2.4 V, the current is not changed anymore. The measured NTC resistance value is used to determine if the external temperature is within the specified maximum value. The current from the 10 MΩ/20 MΩ resistor connected to the mains is compensated.

An MTP parameter sets the maximum allowed external temperature. The MTP parameter sets the maximum allowed conductance (=1/resistance). Also the delay time before a protection is triggered when an overtemperature is detected ($t_{d(otp)}$), can be set with an MTP parameter.

The measurement is done at the peak of the input mains voltage or, if no AC mains is detected, every 100 ms. The SNSMAINS pin outputs a current and measures the pin voltage after 350 μs settling time. In low-power mode, the settling time is extended to 450 μs ($t_{det(NTC)}$) to match the internal ADC that is also operating in low power consumption mode.

TEA2376DT
Product data sheet

All information provided in this document is subject to legal disclaimers.

Rev. 1 — 10 August 2023

© 2023 NXP B.V. All rights reserved.

22 / 46

8.17.7 Short-circuit protection/fast disable (SCP SNSBOOST)

The PFC does not start switching until the voltage on the SNSBOOST pin exceeds $V_{start(scp)}$. This function acts as short-circuit protection for the boost voltage.

When the SNSBOOST pin is shorted to ground or the SNSBOOST upper resistor of the divider is disconnected, this protection inhibits switching.

This function can also be used as a fast disable. If this pin is shorted to ground via an external MOSFET, the system either stops switching or enters the protection mode followed by a safe restart protection or a latched protection. In this way, an additional external protection can be added or the SNSBOOST pin can be used as an enable/disable function of PFC operations.

8.17.8 Overvoltage protection boost voltage (OVP SNSBOOST)

To prevent output overvoltage during load steps and mains transients, a PFC output overvoltage protection circuit is built in. When the voltage on the SNSBOOST pin exceeds the $V_{ovp(SNSBOOST)}$ level, switching of the power factor correction circuit is inhibited. When the SNSBOOST pin voltage drops to below the regulation level ($V_{reg(SNSBOOST)}$) again, the switching of the PFC recommences.

8.17.9 Overvoltage protection measured via AUX pins (OVP AUX)

If the SNSBOOST pin does not provide overvoltage information on the PFC output voltage, a second overvoltage protection is provided via the AUX pins. During the primary and secondary stroke, the currents flowing out of and into the AUX pins are monitored. If the sum of the currents of the primary stroke and secondary stroke exceeds the programmable overvoltage level, a protection is triggered after a programmable number of switching cycles. The OVP level, $V_{ovp(AUXx)(p-p)}$, can be programmed.

8.17.10 Overcurrent protection, inrush protection (OCP SNSCUR)

The PFC current is measured via an external sense resistor (R_{SENSE}) connected to the SNSCUR pin (see Figure 21). If the voltage drops to below $V_{ocp(SNSCUR)}$, the PFC MOSFET is turned off. It resumes switching at the next cycle, if the voltage at the SNSCUR is above the $V_{ocp(SNSCUR)}$ level. The SNSCUR overcurrent protection also prevents the PFC MOSFET from turning on during an inrush situation.

To ensure that the OCP level is not exceeded due to disturbance caused by a turn-on of the PFC MOSFET, the OCP level is filtered via an internal 3 MHz filter.

8.17.11 Current sense resistor short protection (SCP SNSCUR)

To detect a (partially) shorted current sense resistor, the SNSCUR information is compared to the information retrieved from the AUX pins. If the current sense resistor is (partially) shorted, a protection is triggered after a programmable number of cycles and if the deviation is too great and the current is above a minimum level.

8.17.12 PFC coil short protection (SCP coil, SNSCUR pin)

If the PFC coil is shorted, the overcurrent protection on the SNSCUR pin is triggered continuously. To avoid overheating, the system enters the protection state when the OCP is continuously triggered for a selectable number of switching cycles.

8.17.13 PFC output diode short protection (SCP diode)

To enable the output diode short protection, a resistor must be placed in series with the source of the external MOSFETs to ground. To protect the IC against currents caused by parasitic inductance in the MOSFET current

TEA2376DT

Product data sheet **Rev. 1 — 10 August 2023**

23 / 46

path, the SNSSRC pin is connected to the series resistor via a resistor (typical resistor value: 1.5 Ω; see Section 13).

If the PFC output diode is shorted, the overcurrent protection on the SNSSRC pin is triggered continuously ($V_{ocp(SNSSRC)}$). To avoid overheating, the system enters the protection state when the OCP is continuously triggered for a selectable number of switching cycles.

8.17.14 Phase fail protection (AUX1/AUX2 pin)

If one of the PFC phases fails, the converter can still maintain its output voltage in low-load situations. To protect the application from overheating or damage, the input and output voltage information measured via the AUX pins is compared. If deviations greater than a programmable threshold are detected, a protection is triggered.

8.17.15 Overvoltage protection mains (OVP mains)

If a mains overvoltage occurs ($I_{ovp(SNSMAINS)}$), the PFC operation can be suspended. Although the PFC output voltage is still equal to the peak of the rectified mains voltage, for the SO14 version, the POWERGOOD output can signal the downstream converter to suspend switching. Especially when the downstream converter is a flyback type converter, this protection is useful. The mains overvoltage protection requires one mains sense resistor to be connected. If two mains sense resistors are connected, the mains overvoltage protection may trigger unintentionally. The reason is that, at low loads and also during load steps, the SNSMAINS pin voltage may increase due to (stray) capacitance across the rectifier bridge diodes.

8.17.16 Latched, safe restart, or latched after safe restart

When a protection is set to be a latched protection, the system stops switching when this protection is triggered. The system only restarts after a fast latch reset (see Section 8.17.17) or when the VCC supply voltage drops to below the latch-reset level ($V_{rst(VCC)}$).

When a protection is selected to be safe restart, the system continuously restarts after a predefined safe restart time ($t_{d(restart)}$). This safe restart time is the same for all protection functions. It can be set using MTP parameter.

When selecting "latched after safe restart", a protection is initially a safe restart protection. If the failure occurs again within a specific time, it latches.
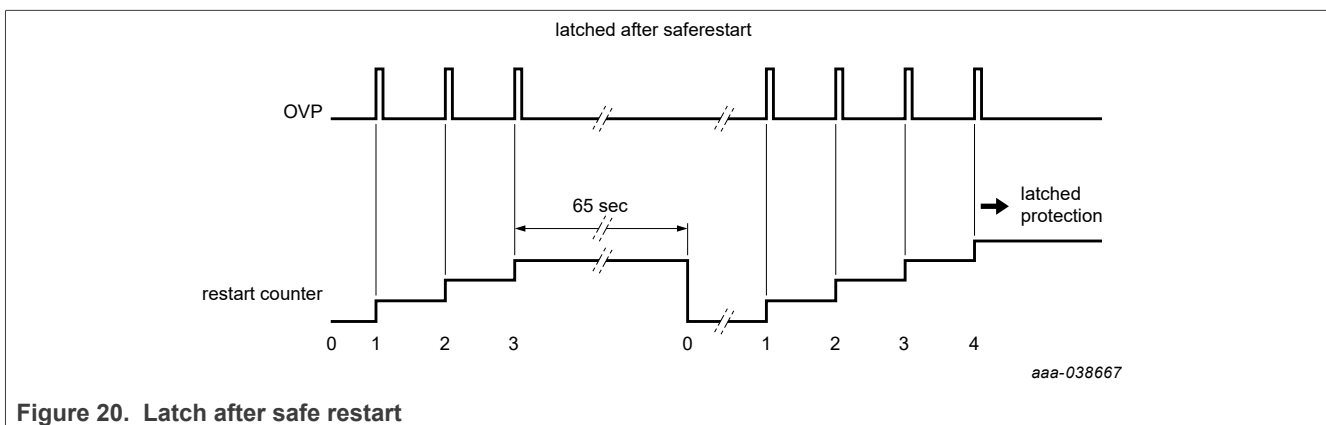
Figure 20. Latch after safe restart

Figure 20 shows an example of when the VCC OVP is set to latched after safe restart. Initially, at an OVP, the system restarts after the safe restart time. An internal counter is then set to '1'. If the protection is triggered again, the counter is increased. If the counter reaches the number as set with a parameter, the system latches. If the protection is not triggered within 65 seconds ($t_{rst(cnt)restart}$), the counter is reset.

TEA2376DT

Product data sheet

All information provided in this document is subject to legal disclaimers.

Rev. 1 — 10 August 2023

© 2023 NXP B.V. All rights reserved.

24 / 46

8.17.17 Fast latch reset

If a protection is triggered, the system enters the protection state. To reset a latched protection, the mains voltage can be kept below the brownout level for a specified time. This fast latch reset functionality is useful during production testing. The time before reset ($t_{d(flr)}$) can be set using a parameter. Resetting of a latched protection in the TEA19161 LLC downstream converter can be done by enabling the option of a fast latch reset pulse on the common SNSBOOST node. After the brownout and a delay time, the TEA2376DT forces a 2 V pulse ($V_{pu(rst)SNSBOOST}$) of 200 μs ($t_{pu(rst)SNSBOOST}$) on the SNSBOOST pin when the brownin level has been exceeded again.

The TEA19161 recognizes this fast latch reset pulse and resets the latched protection.

8.18 Settings

The TEA2376DT has an internal MTP memory where different settings can be programmed.

Disclaimer:

The MTP parameter settings can be changed using the "Ringo" GUI software of NXP Semiconductors. Before the user can change any MTP parameters using the GUI, the terms and conditions in the start-up pop-up screen must be accepted.

8.18.1 General settings

8.18.1.1 Protection register

When the TEA2376DT triggers a protection, the protection information is stored and can be read via I^{2}C. The protection information can be read or cleared using the Ringo GUI.

8.18.1.2 Read lock

To verify settings and for debugging, the MTP memory can be read if the read-lock bit is not programmed. When the read-lock bit in the MTP memory is set, MTP memory is protected from reading. Using the MTP erase function also resets the read-lock bit.

8.18.1.3 Write lock

To prevent that the MTP memory is overwritten accidentally, a write-lock bit can be set. Using the MTP erase function also resets the read-lock bit.

8.18.1.4 Reset to the default values

When the MTP memory is reset, all parameter bits are set to a default value. The default values are suitable for the reference application to work properly.

8.18.1.5 Customer MTP code

If the read-lock bit is set, the content of the MTP memory is unreadable. To still identify the customer MTP coding version, a customer code can be programmed.

The read-lock bit does not mask this customer code.

8.18.2 PFC settings

8.18.2.1 Start-up time

The PFC start-up times that can be selected are 12.8 ms, 25.6 ms, 51.2 ms, or 102.4 ms. During the start-up time, the PFC output voltage follows an RC curve until the target output voltage is reached.

8.18.2.2 Mains measurement

The SNSMAINS input impedance that can be chosen is 10 kΩ for 10 MΩ external resistors to the mains or 20 kΩ for 20 MΩ external resistors to the mains.

The input resistance value is set with an MTP setting.

8.18.2.3 Number of mains resistors

To achieve the lowest no-load input power, a single mains sense resistor can be used. If continuously measuring the mains voltage is necessary, two mains resistors can be used.

For proper functionality, the resistor value and number of resistors in the application are required to correspond to the IC MTP settings.

8.18.2.4 PFC minimum and maximum frequency

The minimum switching frequency of the PFC ($f_{sw(PFC)min}$) can be set within a range from 25 kHz to 80 kHz. The maximum switching frequency ($f_{sw(PFC)max}$) can be set within a range from 75 kHz to 300 kHz.

8.18.3 Protection settings

8.18.3.1 Safe restart time

When the system is in protection mode and the triggered protection is programmed as safe restart, it restarts after a safe-restart time ($t_{d(restart)}$). This time can be set at different values ranging from 0.5 s to 10 s. It is applicable for all related protections.

8.18.3.2 Fast latch reset delay time

When the system does not detect a mains voltage for a programmed period, it assumes that the mains is disconnected and resets all protections. When the mains voltage exceeds the brownin level again, the system restarts. The delay between detecting a brownout ($t_{d(flr)}$; including the brownout delay time) and resetting all protections can be programmed to different values ranging from 0 s to 10 s.

8.18.3.3 Fast disable

When the SNSBOOST voltage is pulled below the $V_{stop(scp)}$ level, the system stops switching. When the voltage on the SNSBOOST pin exceeds the $V_{start(scp)}$ again, level switching resumes.

8.18.3.4 Brownin/brownout level

For the brownin level (I_{bi}), several values can be selected ranging from 67 V (AC) to 185 V (AC). For the hysteresis between the brownin and brownout level ($I_{bo(hys)}$), several values can be selected from 2 V (AC) to 17 V (AC). The given values depend on the resistor values in the application and their tolerances.

When the mains voltage is below the brownout period for a time, the system enters the brownout state. For the time ($t_{d(det)bo}$), several values can be selected ranging from 50 ms to 1.2 s.

8.18.3.5 VCC OVP

The VCC OVP limit ($V_{ovp(VCC)}$) can be set from 10 V to 25 V in steps of 1 V steps. The delay until protection ($t_{d(ovp)VCC}$) can be set to 10 µs, 50 µs, 100 µs, 500 µs, 1000 µs, 5000 µs, or 10,000 µs. This function can also be disabled.

If VCC exceeds 25 V, the protection is triggered without delay.

8.18.3.6 Internal OTP level

The internal OTP (T_{otp}) is fixed at 150 °C. When the internal OTP is triggered, it follows the same response as selected for the external OTP, either latched, safe restart, or latched after safe restart.

8.18.3.7 SNSCUR OCP level

The PFC OCP level is fixed to $V_{ocp(SNSCUR)(two-phase)}$ or $V_{ocp(SNSCUR)(single-phase)}$. It depends on if the converter runs in one-phase operation or two-phase operation. The corresponding current value can be selected using the external sense resistor.

8.18.3.8 PFC maximum on-time

The maximum on-time of the PFC equals 1 / minimum frequency. The minimum frequency ($f_{sw(pfc)min}$) set with the MTP defines the minimum frequency.

8.18.3.9 Coil short protection

When the PFC continuously triggers the SNSCUR OCP for a selectable number of switching cycles, the system enters the protection state. The number of switching cycles can be set to 500 cycles, 2500 cycles, 5000 cycles, or 12,500 cycles. This function can also be disabled.

8.18.3.10 Output diode short protection

When the PFC continuously triggers the SNSSRC OCP for a selectable number of switching cycles, the system enters the protection state. The number of switching cycles can be set to 500 cycles, 2500 cycles, 5000 cycles, or 12,500 cycles. This function can also be disabled.

8.18.3.11 Output OVP

The PFC output voltage is measured via the SNSBOOST pin and the AUX pins. For the OVP at the SNSBOOST pin ($V_{ovp(SNSBOOST)}$), the following values can be selected: 2.60 V, 2.63 V, 2.66 V, or 2.70 V.

When an OVP is detected at the SNSBOOST pin, the PFC stops switching. When its voltage drops below the regulation level, switching continues.

For the OVP at the AUX pins ($V_{ovp(AUXx)(p-p)}$), the following values can be selected: 573 µA, 606 µA, 639 µA, and 671 µA. To avoid false triggering, filtering is added.

The response of an OVP at the AUX pins can be latched, safe restart, or latched after safe restart. This function can also be disabled.

8.18.3.12 Valley detection timeout

When the PFC MOSFET is off and the current through the PFC coil becomes zero, the coil is demagnetized. Normally, shortly after the demagnetization, the drain voltage starts to ring and a valley is detected. When the system detects demagnetization but does not detect a valley shortly after, the ringing is too small to detect a valley. A valley detection timeout is selected. The values can be: 2 µs, 3 µs, 5 µs, or 7 µs.

8.18.3.13 PFC minimum off-time in CCM operation

To ensure a minimum off-time of the drivers and a stable switching operation, a minimum off-time of the PFC driver output can be selected. The available values are 500 ns, 750 ns, 1000 ns, or 1500 ns.

8.18.3.14 PFC minimum secondary stroke time

To avoid false triggering of the demagnetization and valley detection, a minimum secondary stroke of the PFC driver output can be selected using an MTP parameter.

9 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{VCC}	voltage on pin VCC		−0.4	+26	V
$V_{POWERGOOD}$	voltage on pin POWERGOOD		−0.4	+26	V
V_{GATEx}	voltage on GATE pins	pins GATE1 and GATE2	−0.4	+14	V
V_{AUXx}	voltage on AUX pins	pins AUX1 and AUX2	−0.4	+12	V
V_{SNSCUR}	voltage on pin SNSCUR	t < 0.1 s; voltage at external series resistance of 100 Ω; connected to pin SNSCUR	−18	+12	V
		DC; maximum	−0.4	+12	V
$V_{SNSBOOST}$	voltage on pin SNSBOOST		−0.4	+12	V
$V_{SNSMAINS}$	voltage on pin SNSMAINS		−0.4	+12	V
V_{SNSSRC}	voltage on pin SNSSRC		−0.4	+3	V
V_{BURST}	voltage on pin BURST		−0.4	+12	V
V_{SDA}	voltage on pin SDA		−0.4	+12	V
V_{SCL}	voltage on pin SCL		−0.4	+12	V
General					
T_j	junction temperature		−40	+150	°C
T_{stg}	storage temperature		−55	+150	°C
Latch-up					
I_{lu}	latch-up current	all pins; according to JEDEC standard 78D	−100	+100	mA
Electrostatic discharge					
V_{ESD}	electrostatic discharge voltage	human body model (HBM)			
		all pins	−2000	+2000	V
		charge device model (CDM)			
		all pins	−500	+500	V

TEA2376DT

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Product data sheet

Rev. 1 — 10 August 2023

29 / 46

10 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VCC}	supply voltage		0	-	22	V
T_j	junction temperature		−25	-	+125	°C

11 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	In free air; JEDEC test board	93	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	In free air; JEDEC test board	63	K/W

12 Characteristics

Table 8. Characteristics

T_{amb} = 25 °C; V_{VCC} = 12 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC pin						
$V_{start(VCC)}$	start voltage on pin VCC		10.5	11	11.5	V
$V_{uvp(VCC)}$	undervoltage protection voltage on pin VCC		7.6	8	8.4	V
$V_{rst(VCC)}$	reset voltage on pin VCC		5.7	6	6.3	V
$I_{CC(VCC)}$	supply current on pin VCC	brownout state and burst off-state	290	390	490	µA
		operating mode; driver pins open	2.4	3.2	4.0	mA
Protection VCC pin						
$V_{ovp(VCC)}$	overvoltage protection on pin VCC	with programmable triggering delay	23.3	24	24.7	V
		immediate triggering	24.3	25	25.7	V
$t_{d(ovp)VCC}$	overvoltage protection delay time on pin VCC		0.9	1	1.1	ms
Burst mode control VCC pin						
$V_{burst(VCC)}$	burst mode voltage on VCC pin	burst control by VCC pin	9.5	10.0	10.5	V
SNSMAINS pin						
Protections SNSMAINS pin						
$I_{clamp(max)}$	maximum clamp current	$V_{SNSMAINS}$ = 12 V	0.9	1.2	1.5	mA
$I_{ovp(SNSMAINS)}$	overvoltage protection current on pin SNSMAINS	20 MΩ mains resistor [1]	20.2	21.0	21.8	µA
I_{bi}	brownin current	20 MΩ mains resistor	5.34	5.64	5.94	µA
I_{bo}	brownout current	20 MΩ mains resistor	4.67	4.97	5.27	µA
$t_{d(det)bo}$	brownout detection delay time		45	50	55	ms
External overtemperature measurement						
$I_{o(max)SNSMAINS}$	maximum output current on pin SNSMAINS		−210	−200	−190	µA
$t_{det(NTC)}$	NTC detection time		405	450	495	µs
$t_{d(dch)SNSMAINS}$	discharge delay time on pin SNSMAINS	after NTC measurement	450	500	550	µs
$t_{d(otp)}$	overtemperature protection delay time		3.6	4.0	4.4	s

TEA2376DT

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Product data sheet

Rev. 1 — 10 August 2023

31 / 46

Table 8. Characteristics...*continued*

T_{amb} = 25 °C; V_{VCC} = 12 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SNSBOOST pin						
Regulation						
$V_{reg(SNSBOOST)}$	regulation voltage on pin SNS BOOST	continuous operation	2.475	2.500	2.525	V
		burst mode operation	2.450	2.475	2.500	V
$f_{lpf(SNSBOOST)}$	low-pass filter frequency on pin SNSBOOST	ADC input	4.5	5.0	5.5	kHz
Protections SNSBOOST pin						
$V_{ovp(SNSBOOST)}$	overvoltage protection voltage on pin SNSBOOST		2.59	2.63	2.67	V
$V_{stop(scp)}$	short-circuit protection stop voltage		0.37	0.39	0.41	V
$V_{start(scp)}$	short-circuit protection start voltage		0.40	0.45	0.50	V
$I_{prot(SNSBOOST)}$	protection current on SNS BOOST	$V_{SNSBOOST}$ = 0.4 V	5	25	45	nA
Burst mode control SNSBOOST pin						
$V_{det(H)SNSBOOST}$	HIGH-level detection voltage on pin SNSBOOST	burst control by SNSBOOST pull-up	3.17	3.23	3.29	V
$V_{det(L)SNSBOOST}$	LOW-level detection voltage on pin SNSBOOST	burst control by SNSBOOST pull-up	2.74	2.80	2.86	V
$t_{d(ovp)}$	overvoltage protection delay time	burst control not by SNSBOOST pull-up	38	45	52	µs
		burst control by SNSBOOST pull-up	220	245	270	µs
Communication SNSBOOST pin						
$V_{pu(rst)SNSBOOST}$	reset pull-up voltage on pin SNSBOOST	TEA19161 communication; $C_{SNSBOOST} \leq$ 1.5 nF	1.94	2.00	2.06	V
$I_{pu(rst)SNSBOOST}$	reset pull-up current on pin SNSBOOST	TEA19161 communication; $V_{SNSBOOST}$ = 1.8 V	−245	−210	−175	µA
$t_{pu(rst)SNSBOOST}$	reset pull-up time on pin SNSBOOST	TEA19161 communication; $C_{SNSBOOST} \leq$ 1.5 nF; after $V_{SNSBOOST}$ > 1.8 V	160	200	240	µs
$I_{pd(SNSBOOST)}$	pull-down current on pin SNSBOOST	UVP or OTP active; $V_{SNSBOOST}$ = 0.4 V	85	100	115	µA
AUX1 and AUX2 pins						
$V_{demag(high)}$	high demagnetization voltage	input voltage of 33 kΩ AUX resistance	723	850	977	mV
$V_{demag(low)}$	low demagnetization voltage	input voltage of 33 kΩ AUX resistance	60	100	140	mV

Table 8. Characteristics...*continued*

T_{amb} = 25 °C; V_{VCC} = 12 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Protections AUX pins						
$V_{ovp(AUXx)(p-p)}$	peak-to-peak overvoltage protection voltage on AUX pins	pins AUX1 and AUX2; [1] input voltage of 33 kΩ AUX resistance	19.6	21.0	22.4	V
$I_{clamp(AUXx)max}$	maximum clamp current on AUX pins	pins AUX1 and AUX2; V_{AUX} = 12 V	0.9	1.2	1.5	mA
SNSCUR pin						
Protections SNSCUR pin						
$V_{ocp(SNSCUR)}$	overcurrent protection voltage on pin SNSCUR	two-phase operation	−330	−305	−280	mV
		phase-shedding single-phase operation	−175	−150	−130	mV
$V_{det(SNSCUR)}$	detection voltage on pin SNSCUR	open-pin detection level	190	235	280	mV
$I_{o(min)SNSCUR}$	minimum output current on pin SNSCUR	for open pin protection; V_{SNSCUR} = 500 mV	−0.8	−0.6	−0.4	µA
SNSSRC pin						
$V_{ocp(SNSSRC)}$	overcurrent protection voltage on pin SNSSRC		100	125	150	mV
t_{leb}	leading-edge blanking time	on pins SNSSRC and SNSCUR	220	250	280	ns
$I_{prot(SNSSRC)}$	protection current on pin SNSSRC		−1.2	−1.0	−0.8	µA
GATE1 and GATE2 pin						
Drivers						
$I_{source(peak)}$	peak source current	V_{VCC} ≥ 12 V [2]	−1.4	−1.2	−0.9	A
$I_{dch(GATEx)}$	discharge current on GATE pins	pins GATE1 and GATE2; [2] during $t_{dch(GATE)}$; V_{VCC} ≥ 12 V	1.5	1.9	2.3	A
$t_{dch(GATEx)}$	discharge time on GATE pins	pins GATE1 and GATE2; to SNSSRC pin	220	250	280	ns
$R_{OH(GATEx)}$	HIGH-level output resistance on GATE pins	pins GATE1 and GATE2; I_O = −90 mA to −100 mA; V_{VCC} ≥ 12 V	5.5	7.0	8.5	Ω
$R_{OL(GATEx)}$	LOW-level output resistance on GATE pins	pins GATE1 and GATE2; after $t_{dch(GATE)}$; I_O = −90 mA to −100 mA; V_{VCC} ≥ 12 V	4.4	5.7	7.0	Ω
$V_{OH(GATEx)}$	HIGH-level output voltage on GATE pins	pins GATE1 and GATE2; I_O = −10 µA; V_{VCC} ≥ 12 V	9.8	10.2	10.6	V

Table 8. Characteristics...*continued*

T_{amb} = 25 °C; V_{VCC} = 12 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OL(GATEx)}$	LOW-level output voltage on GATE pins	pins GATE1 and GATE2; I_O = 10 µA; $V_{VCC} \geq$ 12 V	0.00	0.01	0.04	V
$t_{r(GATEx)}$	rise time on GATE pins	pins GATE1 and GATE2; [2] 10 % to 90 %; C_{load} = 1 nF; $V_{VCC} \geq$ 12 V	12	21	30	ns
$t_{f(GATEx)}$	fall time on GATE pins	pins GATE1 and GATE2; [2] 90 % to 10 %; C_{load} = 1 nF; $V_{VCC} \geq$ 12 V	5	8	11	ns
$I_{clamp(GATEx)}$	clamp current on GATE pins	pins GATE1 and GATE2; V_{GATE} = 14 V	3	4.5	6	mA
Switching frequency						
$f_{sw(PFC)max}$	maximum PFC switching frequency	configurable up to 300 kHz	117	130	143	kHz
$f_{sw(PFC)min}$	minimum PFC switching frequency		36	40	44	kHz
BURST pin						
$V_{burst(u)}$	upper burst-mode voltage		1.31	1.34	1.37	V
$V_{burst(l)}$	lower burst-mode voltage		1.21	1.24	1.27	V
$I_{prot(BURST)}$	protection current on pin BURST		−150	−100	−50	nA
POWERGOOD pin						
$V_{start(SNSBOOST)}$	start voltage on pin SNSBOOST	for power good	2.23	2.30	2.37	V
$I_{pd(POWERGOOD)}$	pull-down current on pin POWERGOOD	$V_{POWERGOOD}$ = 0.5 V [3]	5	-	-	mA
System protection						
$t_{d(restart)}$	restart delay time		0.9	1.0	1.1	s
$t_{d(flr)}$	fast latch reset delay time		45	50	55	ms
$t_{rst(cnt)restart}$	restart counter reset time	for latched protection	57	63	69	s
I²C communication						
V_{IH}	HIGH-level input voltage	pins SDA, SCL, GATE1, GATE2	1.4	-	5.0	V
V_{IL}	LOW-level input voltage	pins SDA, SCL, GATE1, GATE2	0.0	-	0.8	V
$V_{act(I2C)SNSMAINS}$	I²C activation voltage on pin SNSMAINS	V_{VCC} > 8 V; for I²C via pin GATE1, GATE2	10	16	22	mV

Table 8. Characteristics...*continued*

T_{amb} = 25 °C; V_{VCC} = 12 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{pd}	pull-down current	pins GATE1, SDA; [3] To ensure proper operation, the external pull-up current must always be lower than 15 mA.	15	-	-	mA
Internal overtemperature protection						
T_{otp}	overtemperature protection trip		147	150	153	°C

[1] Available when enabled via MTP modification.
[2] Covered by correlating measurement.
[3] As the minimum limit determines the application design, the maximum limit is not relevant.

13 Application information

aaa-048720
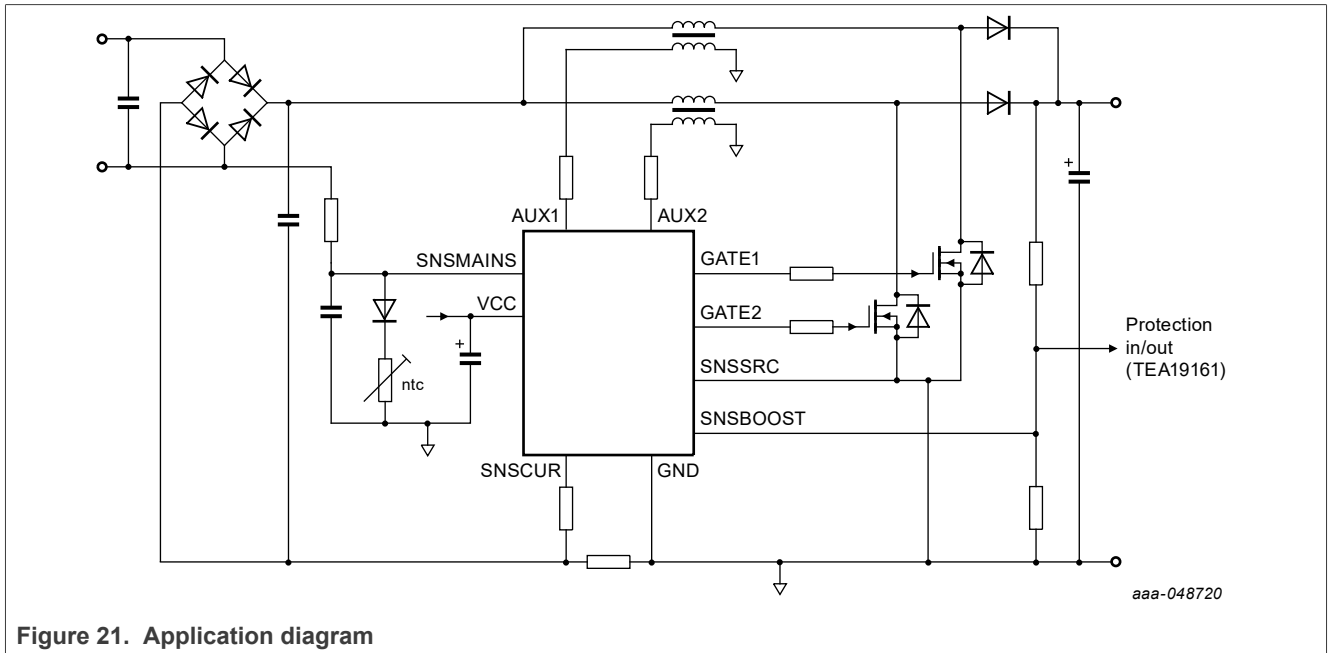
Figure 21. Application diagram

TEA2376DT

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Product data sheet

Rev. 1 — 10 August 2023

35 / 46

14 Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm   **SOT108-1**
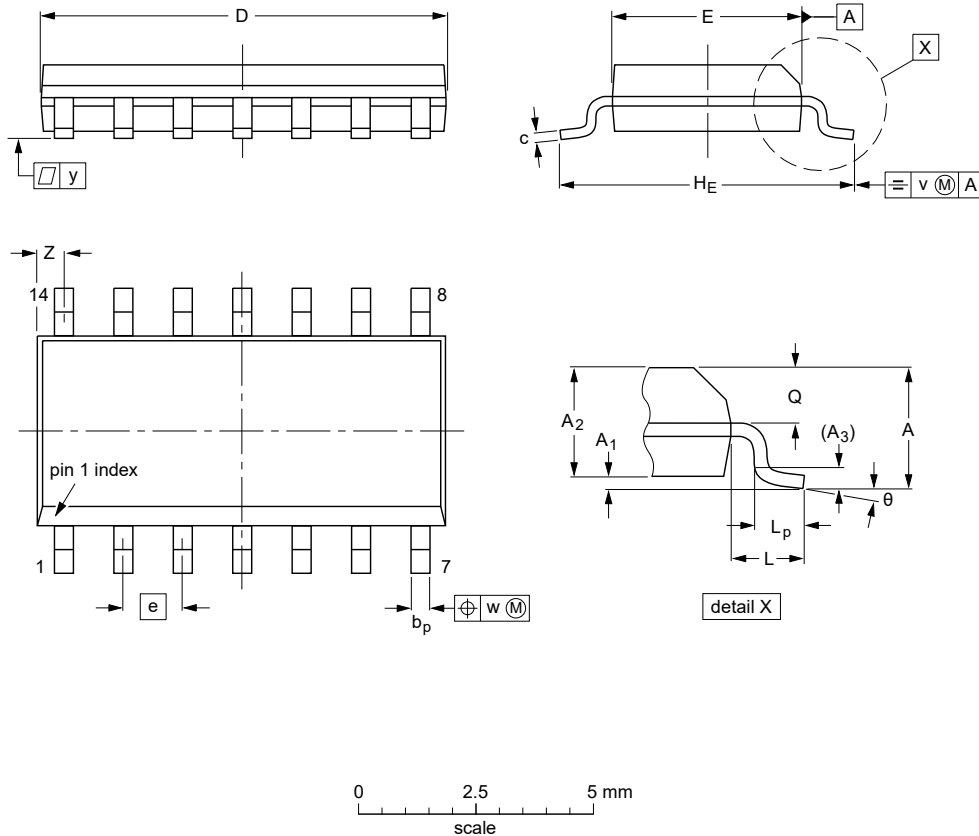
DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D[1]	E[1]	e	H_E	L	Lₚ	Q	v	w	y	Z[1]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				99-12-27 03-02-19

Figure 22. Package outline SO14 (SOT108-1)

Product data sheet   **Rev. 1 — 10 August 2023**

15 Appendix: Ringo parameter settings

Table 9. Ringo parameter/IC parameter settings

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
1	VCC OVP	mtp_vcc_ovp	OK	-	0
2	AUX OVP	mtp_aux_ovp	OK	-	0
3	SNSBOOST short	mtp_snsboost_short	OK	-	0
4	SNSMAINS OVP	mtp_mains_ovp	OK	-	0
5	SNSSRC OCP	mtp_snssrc_ocp	OK	-	0
6	SNSCUR OCP	mtp_snscur_ocp	OK	-	0
7	SNSCUR short	mtp_snscur_short	OK	-	0
8	DIFF PHASE	mtp_diff_phase_fail	OK	-	0
9	POSAUX	mtp_posaux_fail	OK	-	0
10	NEGAUX	mtp_negaux_fail	OK	-	0
11	External OTP	mtp_eotp	OK	-	0
12	Internal OTP	mtp_iotp	OK	-	0
13	MTP read failure	mtp_read_fail	OK	-	0
14	Start up soft start time	mtp_t_start	25.6	ms	0
15	PFC voltage loop gain	mtp_vgain	0.4375	-	9
16	I2C ending delay on GATE	mtp_i2c_mode_to_sel	100	ms	0
17	Protection register logging	mtp_prot_reg_mtp_en	disabled	-	0
18	MTP writing	write_lock	enabled	-	0
19	MTP reading	read_lock	enabled	-	0
20	Brownin Level	mtp_brown_in_lvl	5.7	µA	5
21	Brownin/brownout hysteresis	mtp_brown_in_hys	0.7	µA	4
22	Brownout delay	mtp_brown_out_delay	50	ms	0
23	PFC valley switching	mtp_valleysw	enabled	-	1
24	Filter delay compensation	mtp_t_filt_delay	277	µs	0
25	Mains sensitivity	mtp_mains_sensitivity	low	-	0
26	Mains sensing resistor value	mtp_rmains	20	MΩ	1
27	Notch filter in regulation loop	mtp_notch_en	enabled	-	1
28	PFC gamma value	mtp_pfc_gamma	36	-	36
29	Mains peak zero crossing detection	mtp_pk_pos_detect	enabled	-	1
30	Mains sense wait time after NTC	mtp_t_snsmains_discharge	500	µs	0
31	Disable NTC during startup	mtp_ntc_chk_en	enabled	-	1
32	SNSMAINS phase factor	mtp_phase_factor	0.9375	-	0
33	SNSBOOST level low gain increase	mtp_level_gm_low	off	-	0
34	SNSBOOST low gain increase	mtp_gain_gm_low	2x	-	0

TEA2376DT

Product data sheet

All information provided in this document is subject to legal disclaimers.

Rev. 1 — 10 August 2023

© 2023 NXP B.V. All rights reserved.

37 / 46

Table 9. Ringo parameter/IC parameter settings...*continued*

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
35	VCC stop level	mtp_vcc_stop	8	V	0
36	Mains sensing resistors	mtp_nr_resistors	1 resistor	-	0
37	VCC start level	mtp_vcc_start	11	V	0
38	AUX sensing filter	mtp_fc_aux	5	MHz	0
39	AUX blanking time	mtp_t_aux_blank	600	ns	0
40	AUX high time for sec stroke	mtp_t_wait_aux_high	750	ns	0
41	Time slot for measuring NTC	mtp_t_meas_ntc	450	µs	0
42	NTC circuit diode voltage drop	mtp_udiode_dig0	460	mV	0
43	Number of phases controller	mtp_phase1_only	2	phase	0
44	Startup delay for AC/DC detection	mtp_wait_for_acdc	wait AC/DC det	-	1
45	Phase when no valley switching	mtp_force_phase_valley_dis	phase 180	-	0
46	Min switch on delay between phases	mtp_min_tps_diff_delay	204	ns	0
47	Max switch on delay between phases	mtp_max_tps_diff_delay	2	µs	0
48	Ipfc_peak for Fmin	mtp_vrsense_fmin	55	-	0
49	Delta Ipfc_peak for Fmax-Fmin	mtp_vrsense_fmax_fmin	110	-	0
50	Min PFC freq phase value	mtp_phi_imin	0.18	-	0
51	Max-min PFC freq phase value	mtp_phi_imin_imax	0.14	-	0
52	Minimum switching frequency	mtp_fmin	40	kHz	0
53	Maximum switching frequency	mtp_fmax	130	kHz	0
54	Power level for leaving Shedding	mtp_pshed_high_perc	30	%	3
55	Hysteresis for entering Shedding	mtp_pshed_hys_perc	10	%	0
56	Time delay for entering Shedding	mtp_time_shed	140	ms	0
57	Value of AUX measurement resistor	mtp_raux	33	kΩ	0
58	Duty cycle reduction at OCP	mtp_ocp_red	0.75	-	0
59	Soft start time BM	mtp_softstart_time	normal	-	0
60	Ton steps in soft stop CCM	mtp_softstop_tonstep	normal	-	0
61	Initial on time at startup	mtp_scale_duty_init	normal	-	0
62	Slope current	mtp_cur_limit_dc	0.75	-	0
63	Proportional loop gain	mtp_pgain	10	-	0
64	Regulation Vin compensation	mtp_vincomp	enabled	-	1
65	Regulation Vin current compensation	mtp_cur_vincomp	enabled	-	1
66	Regulation Tring compensation	mtp_tringcomp	enabled	-	1
67	QR mode switching	mtp_en_qr	enabled	-	1
68	CCM allowed	mtp_sel_ipfc_ok	when needed	-	0

TEA2376DT

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Product data sheet **Rev. 1 — 10 August 2023**

38 / 46

Table 9. Ringo parameter/IC parameter settings...*continued*

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
69	AUX min oscillation level	mtp_osc_amin	17	V	0
70	AUX scaling oscillation to valley	mtp_osc_scale	1	-	0
71	AUX delay compensation	mtp_osc_offset	93	ns	0
72	AUX valley detection time out	mtp_osc_timeout	3	µs	0
73	AUX valley detection hysteresis	mtp_osc_hys	2	-	0
74	AUX demag time out	mtp_wait_mag	3	µs	0
75	Minimum GATE off time	mtp_toffmin	1	µs	0
76	Notch filter for mains frequency	mtp_ton_fir_filt	enabled	-	1
77	PFC current loop gain	mtp_igain	35	-	35
78	PFC current scaler	mtp_kdes	2.013	-	13
79	Limit the power at start	mtp_pwr_limit_start	255; no limit	-	0
80	Minimum secondary stroke time	mtp_minsecstroke	1	µs	0
81	Minimum stretch time	mtp_stretchmin	200	ns	0
82	Minimum Ides clamp level	mtp_idesmax_min	13	%	0
83	Ides clamp slope K	mtp_k_idesclamp	1	-	2
84	Ipfc clamp function	mtp_idesclamp_en	enabled	-	1
85	Slope clamp value	mtp_slope_clamp	512	-	0
86	SNSBOOST high gain increase	mtp_gain_gm_high	4x	-	0
87	3ms blanking BI after BO	mtp_bi_blank	enabled	-	1
88	External OTP protection Level	mtp_gotp_limit	88	-	0
89	External OTP delay time	mtp_t_eotp	4	s	0
90	FLR only when protection	mtp_flr_only_at_prot	disabled	-	0
91	SNSBOOST low clears all protections	mtp_snsb_short_clr_prots	disabled	-	0
92	Fast latch reset delay time	mtp_flr_delay	50	ms	0
93	External OTP level multiplier	mtp_mult_gntc	32x	-	0
94	Safe Restart Time	mtp_restart_time	1	s	0
95	VCC OVP delay	mtp_vcc_ovp_delay	1000	µs	0
96	AUX OVP level	mtp_aux_ovp_value	215	-	0
97	SNSMAINS OVP level	mtp_snsmains_ovp_value	420	mV	0
98	SNSBOOST OVP level	mtp_snsboostovp	2.63	V	0
99	VCC OVP level	mtp_vcc_ovp_limit	24	V	0
100	Max pos AUX voltage difference	mtp_min_auxpos_value	12	(dig)	1
101	Fast Latch Reset function	mtp_fast_latch_reset	disabled	-	0
102	PFC shortwinding delay cycles	mtp_max_drain_short_count	2500	-	0

Table 9. Ringo parameter/IC parameter settings...*continued*

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
103	OCP blanking time	mtp_ocp_blanking_time	250	ns	0
104	SNSCUR short detection level	mtp_snscur_short_det_lvl	30	-	0
105	Max SNSCUR cycles to show short	mtp_nr_snscur_short_cycles	200	cycles	3
106	Max AUX voltage difference in phases	mtp_max_vout_diff	25	(dig)	3
107	AUX voltage measurement filter	mtp_aux_v_filt_setting	4	cycles	0
108	AUX min time for valid stroke	mtp_tmin_pk_hold	750	ns	0
109	Max missed AUX primary strokes	mtp_max_missed_prim_strokes	100	cycles	0
110	Max missed AUX secondary strokes	mtp_max_missed_sec_strokes	100	cycles	0
111	SNSCUR current ratio	mtp_snscur_ratio	128	-	0
112	SNSBOOST pulldown at brownout	mtp_snsboost_pulldown_brownout	0	ms	0
113	SNSMAINS OVP prot follow up	mtp_mains_ovp_mode	disabled	-	0
114	VCC OVP prot follow up	mtp_vcc_ovp_mode	safe restart	-	0
115	AUX OVP prot follow up	mtp_aux_ovp_mode	disabled	-	7
116	SNSBOOST short prot follow up	mtp_snsb_short_mode	auto continue	-	0
117	SNSSRC overcurrent prot follow up	mtp_snssrc_oc_mode	safe restart	-	0
118	Allow startup with mains DC	mtp_allow_startup_dc_load	disabled	-	0
119	SNSCUR overcurrent prot follow up	mtp_snscur_oc_mode	safe restart	-	0
120	SNSCUR short protect follow up	mtp_snscur_short_mode	safe restart	-	0
121	Internal OTP prot follow up	mtp_iotp_mode	safe restart	-	0
122	External OTP prot follow up	mtp_eotp_mode	safe restart	-	0
123	AUX phase fail prot follow up	mtp_pf_vout_diff_mode	safe restart	-	0
124	AUX pos phase fail prot follow up	mtp_pf_pos_aux_mode	safe restart	-	0
125	AUX neg phase fail prot follow up	mtp_pf_neg_aux_mode	safe restart	-	0
126	Duration soft start/stop operation	mtp_bm_end_soft_start_stop	infinite	-	0
127	Burst mode SNSBOOST ripple	mtp_bmripple	105	mV	0
128	BM soft start	mtp_skip_soft_start	softstart	-	0
129	BM soft stop	mtp_skip_soft_stop	softstop	-	0
130	Burst mode delay time	mtp_burstdelay	0	s	0
131	Burst mode level	mtp_bmpth_low	10.9	%	0
132	Burst on/off level on VCC	mtp_bmvccth	10	V	0
133	Burst mode type	mtp_bm	auto	-	0
134	BM boost recover	mtp_boostrecover	disabled	-	0
135	External BM control pin	mtp_bm_ctrl_sel	BURST normal	-	0
136	BM depending on shedding	mtp_bm1phase	1 phase only	-	1
137	Burst starts with 1 phase	mtp_single_phase_burst_restart	disabled	-	0

Table 9. Ringo parameter/IC parameter settings...*continued*

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
138	BM hysteresis	mtp_bmpth_hys	3.1	%	0
139	SNSBOOST level to stop PG	mtp_pwrgood_stop_pct	0.5	-	0
140	Power good at mains brownout	mtp_pwrgood_bo_stop	enabled	-	1
141	SNSBOOST level for power good	mtp_pwrgood_start_lvl	2.3	V	6
142	Power Good polarity	mtp_pwrgood_pol	normal	-	0
143	PG stopped by SNSBOOST	mtp_pwrgood_lvl_stop	enabled	-	1
144	Vendor code	mtp_code	0x0003	-	3

16 Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA2376DT v.1	20230810	Product data sheet	-	-

TEA2376DT

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Product data sheet

Rev. 1 — 10 August 2023

42 / 46

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

TEA2376DT
Product data sheet

All information provided in this document is subject to legal disclaimers.

Rev. 1 — 10 August 2023

© 2023 NXP B.V. All rights reserved.

43 / 46

17.4 Trademarks

TEA2376DT

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Product data sheet

Rev. 1 — 10 August 2023

44 / 46

Contents

TEA2376DT

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Product data sheet

Rev. 1 — 10 August 2023

45 / 46