Freescale Semiconductor, Inc.
Application Note

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Hardware Design Considerations for MKW40Z/30Z/20Z BLE and IEEE 802.15.4 Devices

1 Introduction

This application note describes Printed Circuit Board (PCB) design considerations for the MKW40Z and MKW20Z 48-pin Laminated QFN (LQFN) package as well as for the MKW30Z 32-pin LQFN package. Included are layouts of the component copper layer, solder mask, and solder paste stencil. These recommendations are guidelines only and may need to be modified depending on the assembly house used and the other components on the board.

Contents

2 48-pin LQFN component copper layer

Figure 1 shows a recommended component copper layer. This layer is also referred to as the top metal layer and is the layer to which the components are soldered. The footprint for the 48-pin LQFN package consists of 48 IC contact pads, and 16 centered ground pads. The copper pattern is shown in Figure 1. Use 0.25 mm via holes to connect to the ground plane layers. These are required for RF grounding and help to prevent solder float.

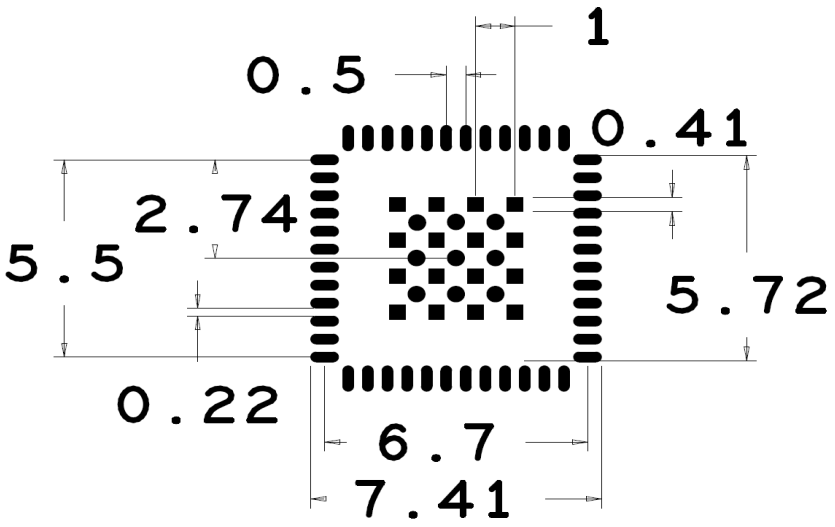

Figure 1. 48-pin LQFN component copper layer

2.1 48-pin LQFN solder mask

The solder mask limits the flow of the solder paste during the reflow process. Figure 2 shows a recommended solder mask pattern. The pattern represents openings in the solder mask.

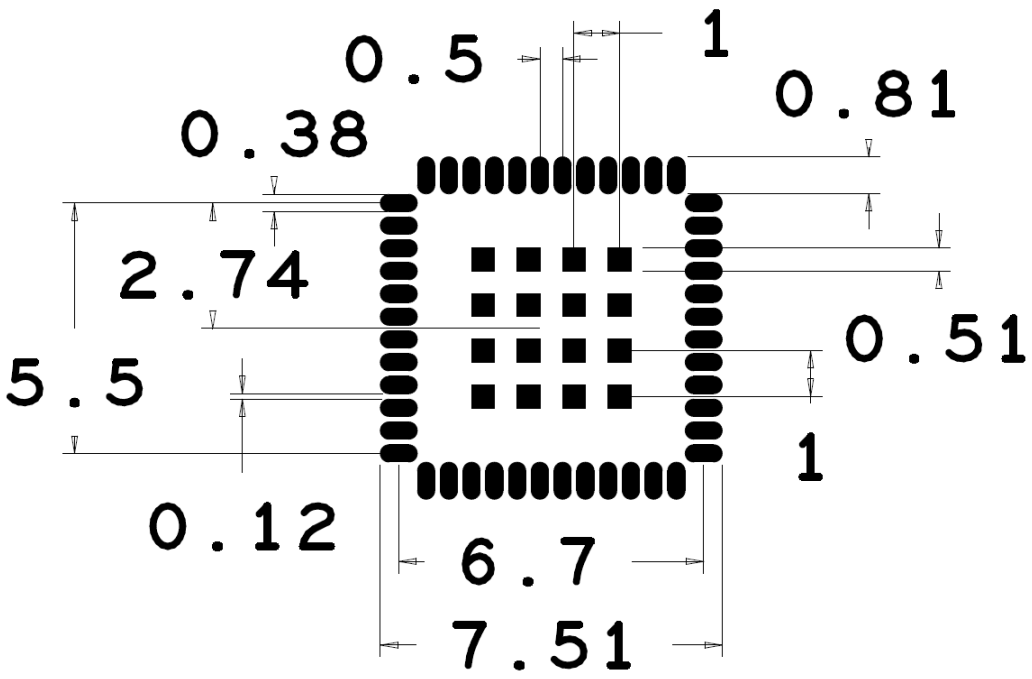

Figure 2. 48-pin LQFN solder mask pattern

2.2 48-pin LQFN solder paste stencil

The solder paste stencil controls the pattern and thickness of the solder paste dispensed on the board. Figure 3 shows a recommended solder stencil pattern. Stencil thickness should be approximately 0.1 mm.

Other patterns and opening sizes can be used if too much solder is being applied. See Section 2.2.1, "LGA problems with excess solder," for more information.

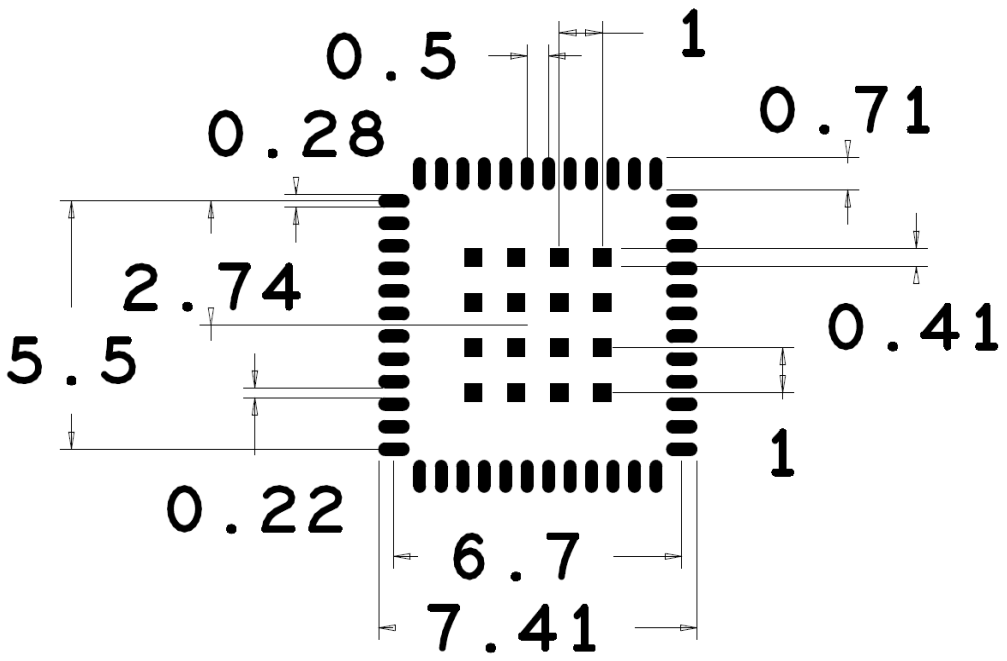

Figure 3. 48-pin LQFN solder stencil pattern

2.2.1 LGA problems with excess solder

Excess solder may cause the LGA to float or bridge between the package contacts. To use the correct amount of solder paste applied to the PCB, take into consideration the following:

- Stencil thickness
- Other components mounted on the PCB
- Manufacturing equipment
- Assembly house experience

3 48-pin LQFN package dimensions

Figure 4 shows the 48-pin LQFN package dimensions.

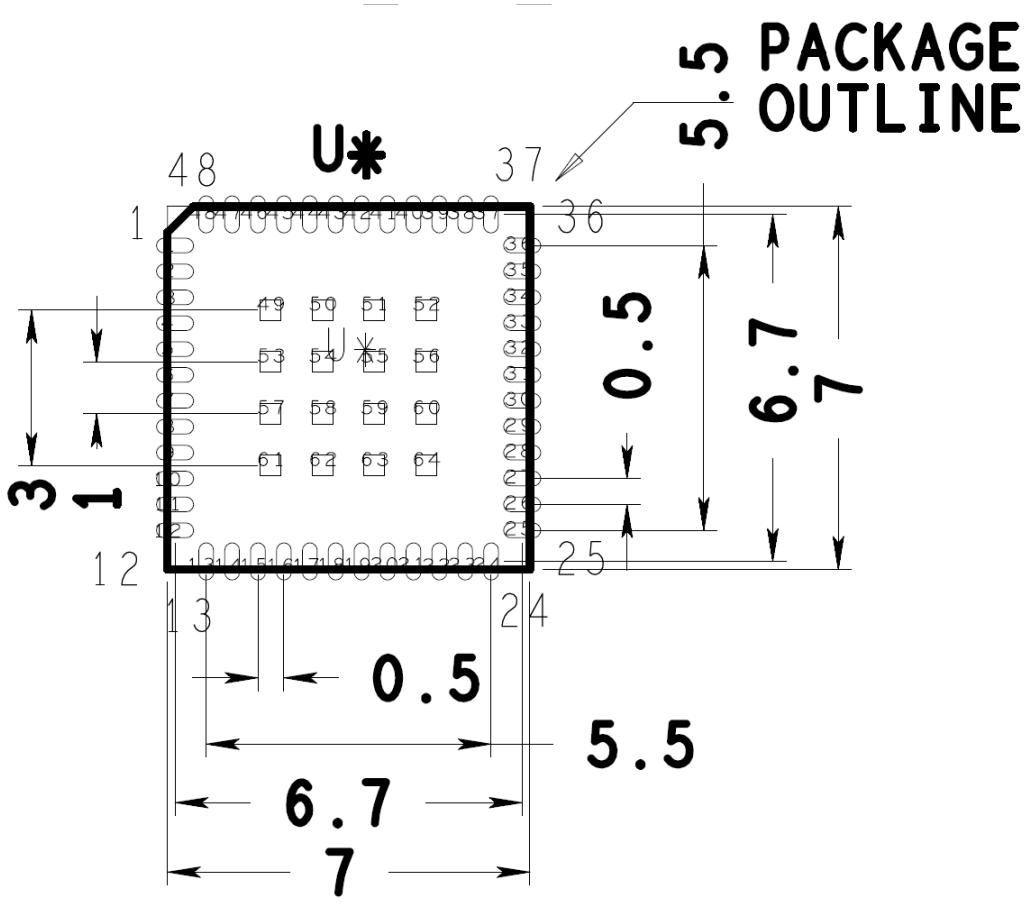

Figure 4. 48-pin LQFN package dimensions

3.1 48-pin LQFN device marking details

The MKW40Z and MKW20Z devices are in the 48-pin LQFN (7 × 7 mm). Figure 5 shows device marking examples for the LQFN device.

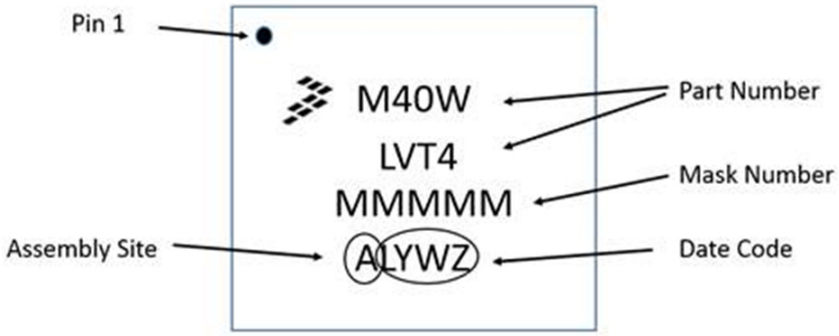

Figure 5. 48-pin LQFN device marking

4 48-pin LQFN soldering profile

Figure 6 shows the recommended soldering profile for the MKW40Z 48-pin LQFN package, in a board size approximately 3.20 inches × 2.10 inches.

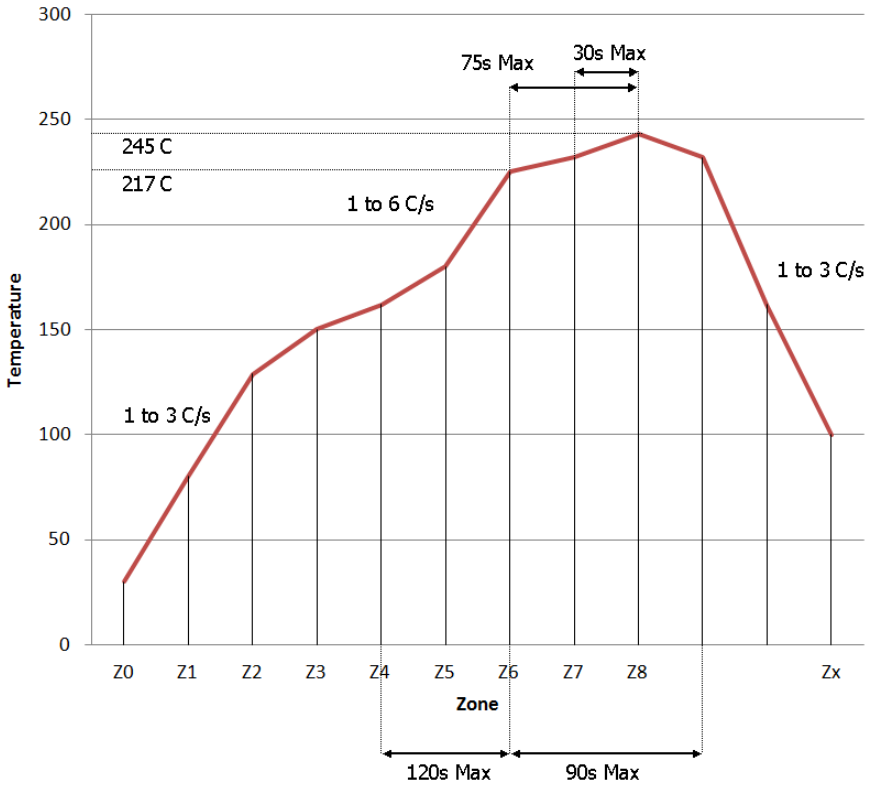

Figure 6. 48-pin LQFN soldering profile

5 32-pin LQFN component copper layer

Figure 7 shows a recommended component copper layer. This layer is also referred to as the top metal layer and is the layer to which the components are soldered. The footprint for the 32-pin LQFN package consists of 32 IC contact pads, and 9 centered ground pads. The copper pattern is shown in Figure 7. Use 0.30 mm via holes to connect to the ground plane layers. These are required for RF grounding and to help prevent solder float.

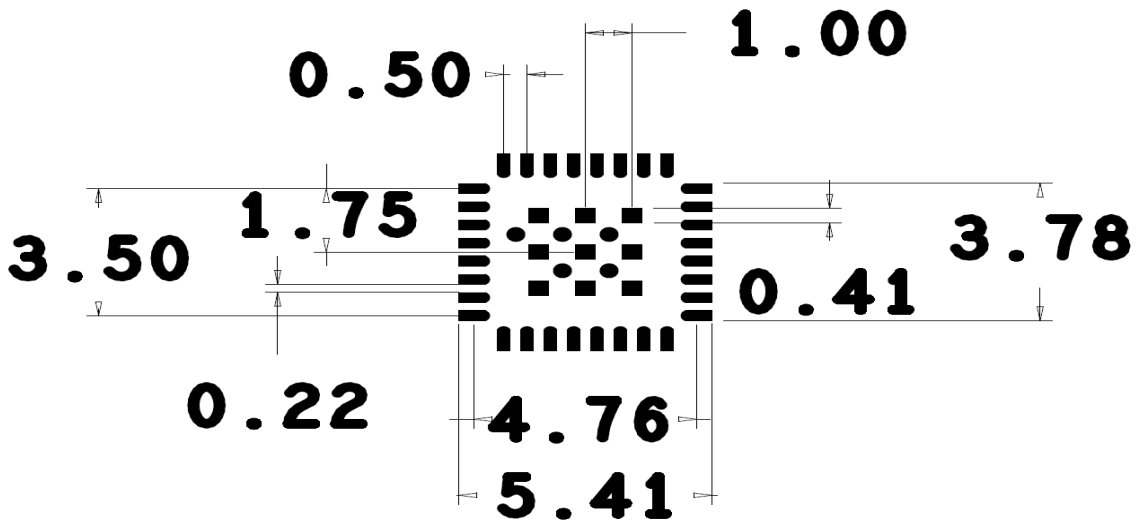

Figure 7. 32-pin LQFN component copper layer

5.1 32-pin LQFN solder mask

The solder mask limits the flow of the solder paste during the reflow process. Figure 8 shows a recommended solder mask pattern. The pattern represents openings in the solder mask.

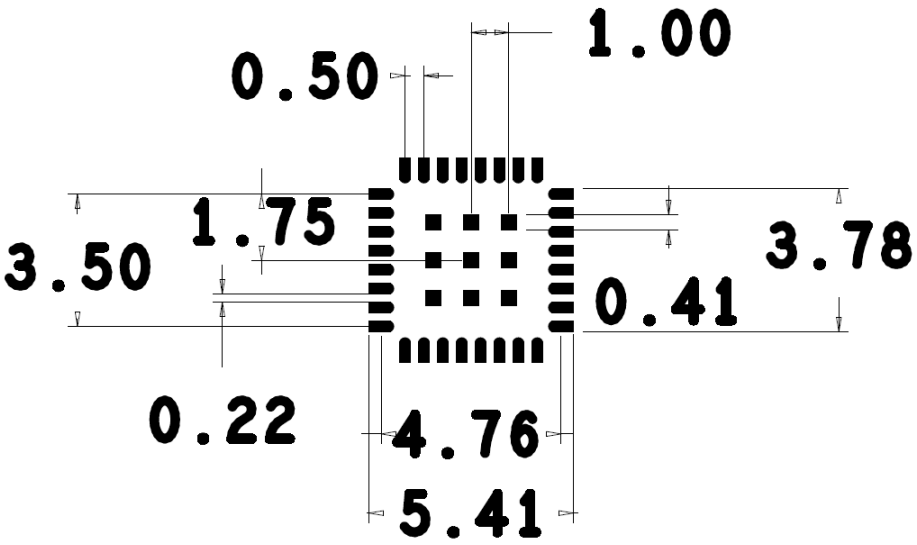

Figure 8. 32-pin LQFN solder mask pattern

5.2 32-pin LQFN solder paste stencil

The solder paste stencil controls the pattern and thickness of the solder paste dispensed on the board. Figure 9 shows a recommended solder stencil pattern. Stencil thickness should be approximately 0.1 mm.

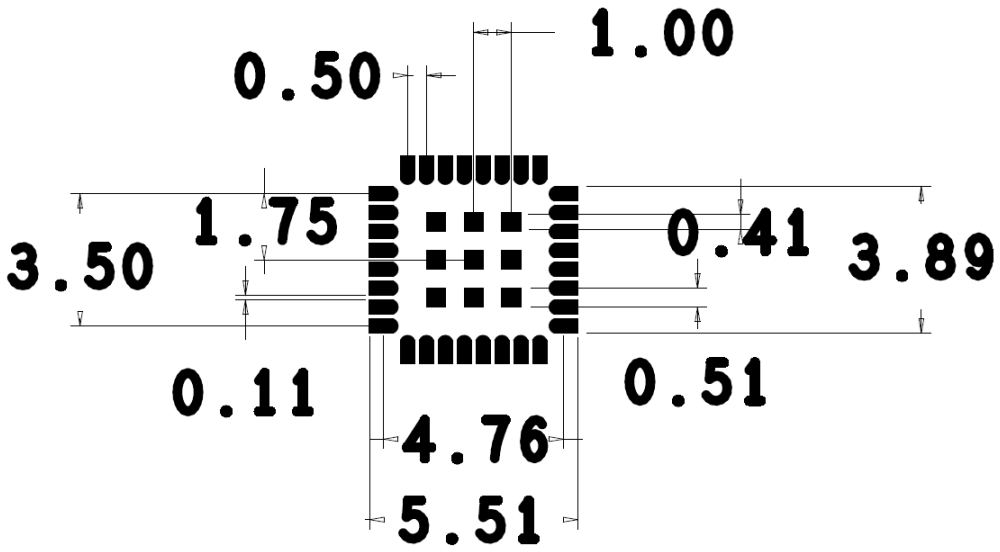

Figure 9. 32-pin LQFN solder stencil pattern

6 32-pin LQFN package dimensions

Figure 10 shows the 32-pin LQFN package dimensions.

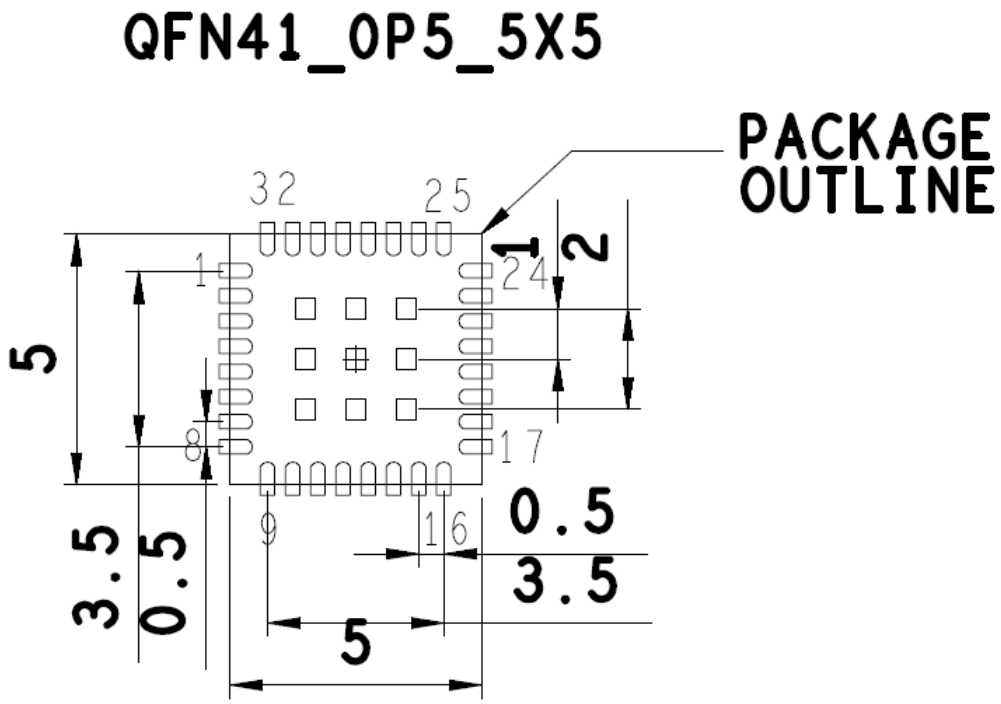

Figure 10. 32-pin LQFN package dimensions

6.1 32-pin LQFN device marking details

The MKW30Z devices are in the 32-pin LQFN (5 × 5 mm). Figure 11 shows device marking examples for the LQFN device.

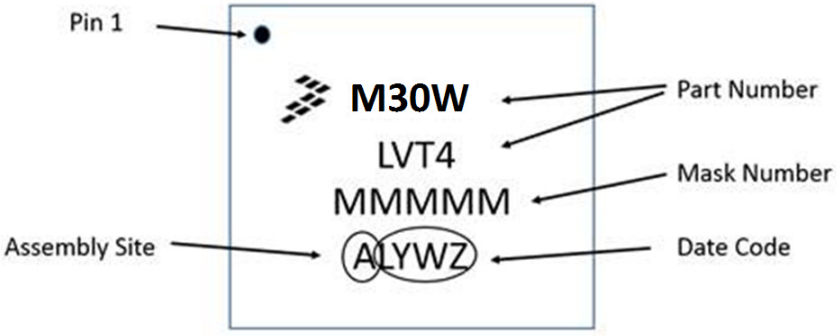

Figure 11. 32-pin LQFN device marking

7 Design and board layout considerations

To have successful wireless hardware development, the proper device footprint, RF layout, circuit matching, antenna design, and RF measurement capability are essential. RF circuit design, layout, and antenna design are specialties requiring investment in tools and experience. With available hardware reference designs from Freescale, RF design considerations, and the guidelines contained in this application note, hardware engineers can successfully design BLE and IEEE 802.15.4 radio boards with good performance levels. Figure 12 shows the FRDM-KW40Z development board. It contains the MKW40Z device and all necessary I/O connections.

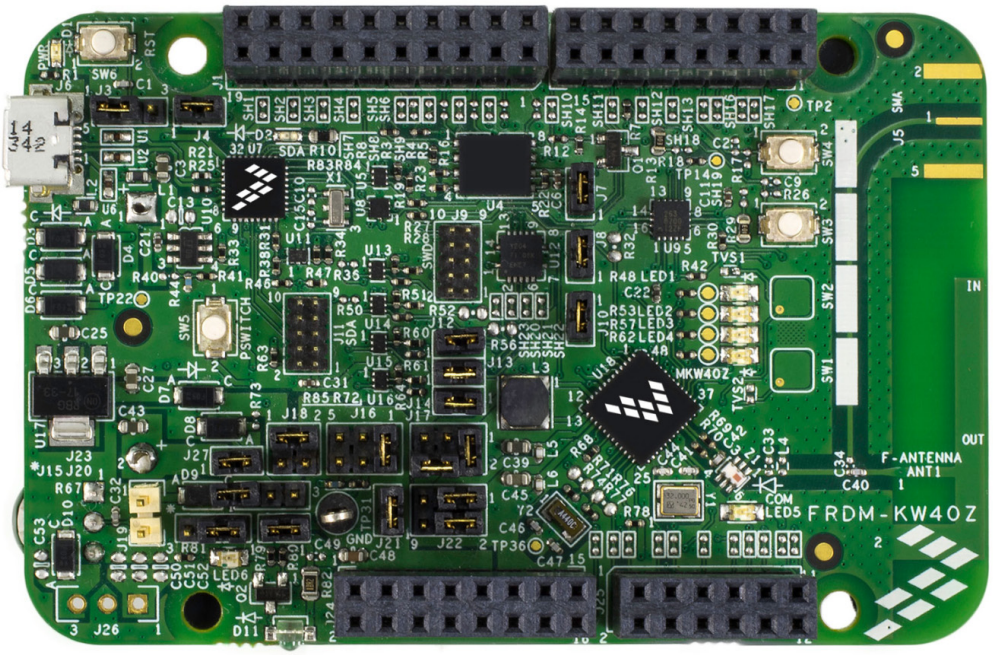

Figure 12. FRDM-KW40Z development board

The device footprint and layout are critical and the RF performance is affected by the design implementation. For these reasons, use of the Freescale recommended RF hardware reference designs are important for successful board performance. Additionally, the reference platforms have been optimized for radio performance. If the recommended footprint and design are followed exactly in the RF region of the board; sensitivity, output power, harmonic and spurious radiation, and range will have a high likelihood of first time success.

The following subsections describe important considerations when implementing a wireless hardware design starting with the device footprint, RF circuit implementation, and antenna selection. Figure 13 shows an example of a typical layout with the critical RF section which must be copied exactly for optimal radio performance. The less critical layout area can be modified without reducing radio performance.

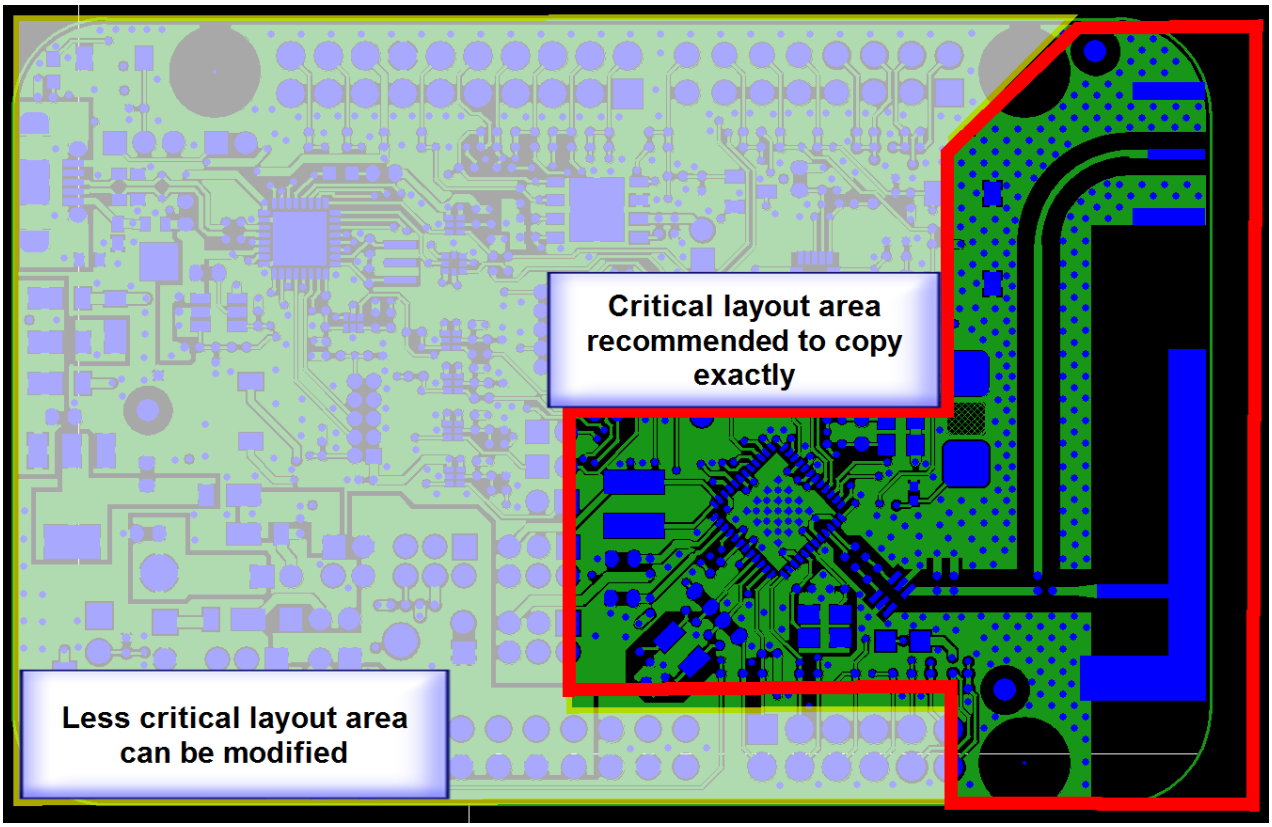

Figure 13. Critical layout areas

7.1 MKW40Z device footprint

The performance of the wireless link is largely influenced by the device's footprint. As a result, a great deal of care has been put into creating a footprint so that receiver sensitivity and output power are optimized to enable board matching and minimal component count. Freescale highly recommends copying the die flag exactly as it is shown in Figure 14; this includes via locations as well. Deviation from these parameters can cause performance degradation.

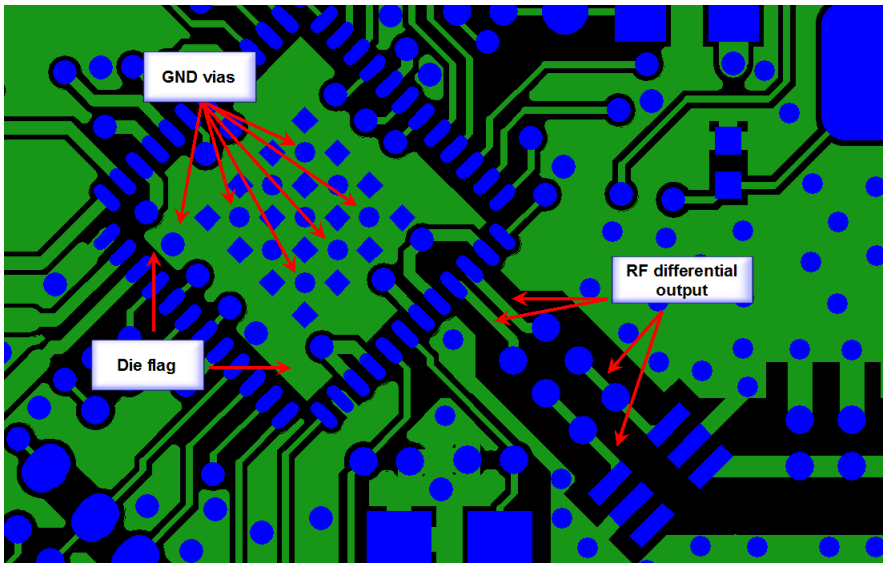

Figure 14. Critical layout of die flag area

Figure 14 shows the critical areas of the device die flag. These are the following:

- Ground vias and locations
- RF differential output and ground traces
- Die flag shape
- Test pins.

As shown in Fig.14, regarding transmission lines, it is important to copy not just the physical layout of the circuit, but also the PCB stackup. Any small change in the thickness of the dielectric substrate under the transmission line will have a significant change in impedance, all this information can be found on the fabrication notes for each board design. In the example above, a 50 ohm trace was 18 mils wide over the 10 mils of FR4. If that thickness of FR4 is changed from 10 to 6 mils, the impedance will only be about 36 ohms.

When the top layer dielectric becomes too thin, the layers will not act as a true transmission line; even though all the dimensions are correct. There is not universal industry agreement on which thickness at which this occurs, but Freescale prefers to use a top layer thickness of no less than 8-10 mils. The use of a correct substrate like the FR4 with a dielectric constant of 4.3 will assist you in achieving a good RF design.

7.2 RF circuit topology and matching

Transmission lines have several shapes such as microstrip, coplanar waveguide, and stripline. For BLE and 802.15.4 applications built on FR4 substrates, the types of transmission lines typically take the form of microstrip or coplanar waveguide (CPW). These two structures are defined by the dielectric constant of the board material, trace width, and the board thickness between the trace and the ground. Additionally for CPW, the transmission line is defined by the gap between the trace and the top edge ground plane. These parameters are used to define the characteristic impedance of the transmission line (trace) that is used to convey the RF energy between the radio and the antenna.

Typically, the RF ports from the BLE and 802.15.4 radios are differential or balanced. The impedances of the RF ports at the radio are in the range of 100 ohms. Freescale applications typically use a balun to transform the balanced signals to a single ended output with a characteristic impedance of 50 ohms. Therefore, Freescale recommends an antenna with a 50 ohm feed.

A good practice is to review all components in the RF section of a layout and remove all excess metal. In addition, avoid routing traces near or parallel to RF transmission lines or RF bias lines. RF signals will couple to these pieces of metal, which are usually connected to ground and can distort the signal. Maintaining a continuous ground under an RF trace is critical to maintaining the characteristic impedance of that trace. Avoid any routing on the ground layer that will result in disrupting the ground under the RF traces.

Complexity is the main factor that will determine whether the design of an application board can be two-layer, four-layer, or more. The recommended board stackup for either a two-layer or four-layer board design is as follows:

- Two-layer stackup:
  - Top: RF routing of transmission lines, signals, and ground
  - Bottom: RF reference ground, signal routing, and general ground
- 4-layer stackup:
  - Top: RF routing of transmission lines
  - L2: RF reference ground
  - L3: DC power
  - Bottom: signal routing

For more information, see Freescale application note Freescale IEEE 802.15.4 / ZigBee Package and Hardware Layout Considerations (ZHDCRM)

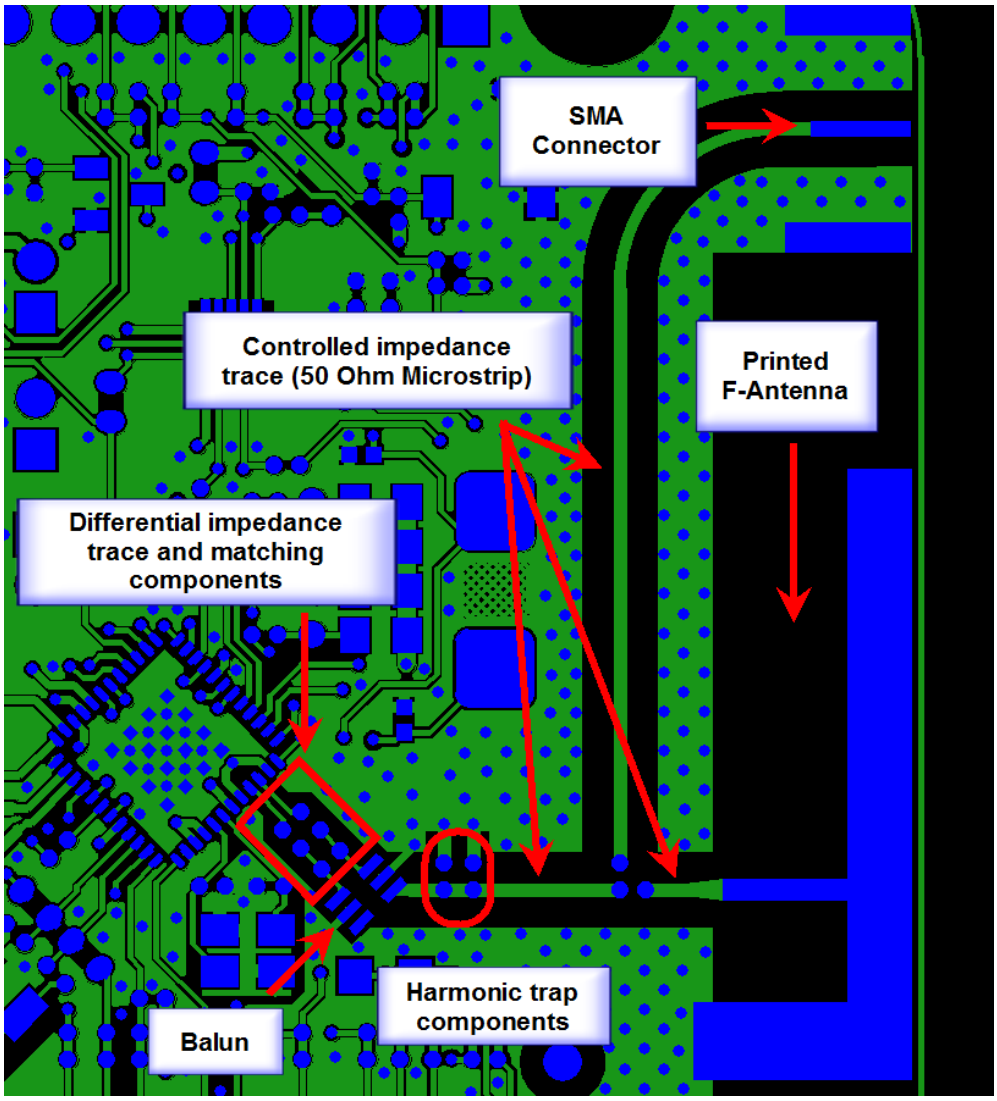

Figure 15. RF matching network

- Differential impedance traces should be kept as short as possible:
  - Length traces are lossy and inductive.
  - Keep trace lengths short between device differential port and balun.
- Notice how all traces and grounds are far away from the RF traces (both differential and single ended).
  - In Figure 15 the microstrip topology is used. In CPW, the gap to ground is integral in maintaining the characteristic impedance.
  - When a harmonic trap is used, it is easier to use a microstrip transmission line rather than CPW between the balun and antenna because the constant gap required for CPW is disrupted.
- Harmonic trap components
  - Lengths of trace are added between the component and ground to add effective inductance.
  - Notice the components' long trace length to ground, this creates a tuned resonance.

- Grounding is imperative
  - Vias are used to form ground planes for RF components.
  - Note antenna considerations in the next section.
  - Caution when routing traces near RF lines. PCB traces can act as effective radiators at RF frequencies.
- Examples of PCB parasitics:
  - At 2.4 GHz, a 10 mil wide PCB trace 275 mils long on 32 mil FR4 is equivalent to a 3.2 nH inductor, +j73 ohms.
  - A 10 mil via in 32 mil FR4 is about 0.5 to 1 nH.

7.3 Antenna considerations

There are a large variety of antenna types available to choose from when designing for a wireless system. These include small footprint chip antennas, trace antennas, loop monopole, and dipole, each with their own set of pros and cons depending on the goal of the application. Freescale recommends using one of the proven antenna implementations used in many of our hardware reference designs. Figure 16 shows a folded F antenna used in a small USB dongle. This is a low-cost trace implementation that performs very well. If a smaller board footprint is required, the use of a chip antenna is better suited with the trade off of cost, performance, and range. For more information on compact antenna designs, see Freescale application note *Compact Integrated Antennas* (AN2731).

For this illustration, Figure 16 uses the folded F trace antenna as an example of what the hardware engineer must be aware of when designing a board layout for a wireless node.

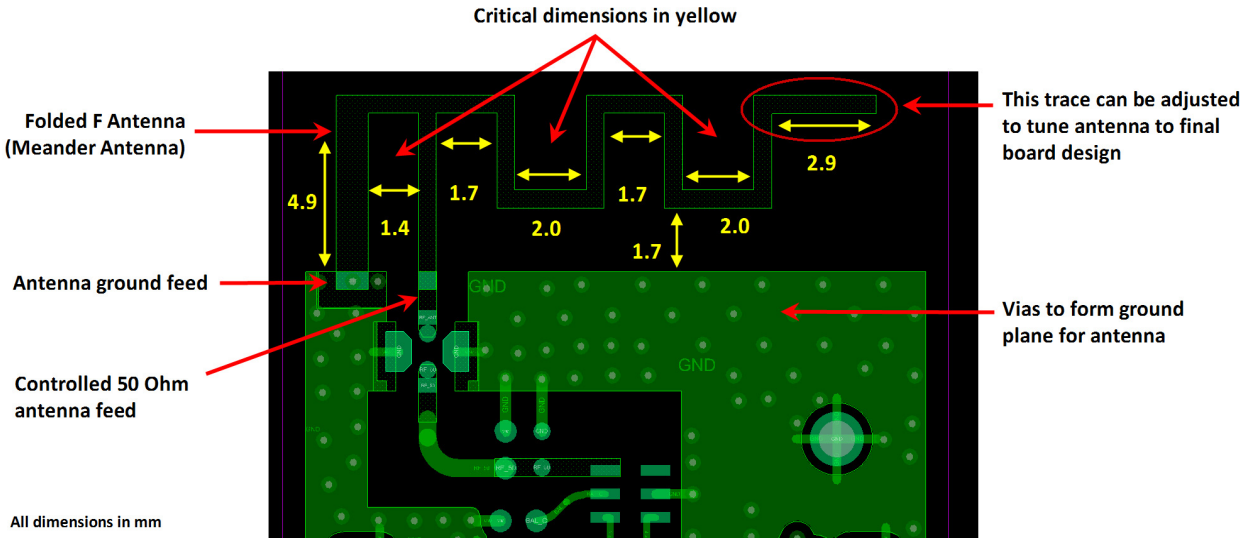

Figure 16. Antenna network

Steps for good antenna performance:

- Be mindful of critical dimensions:
  - Notice the critical dimensions of the trace antenna. These should be copied exactly.

- Customer final board sizes may differ from the Freescale reference designs. As a result, the last leg of the trace antenna should be made longer to allow for final board tuning.
- Antenna tuning may be required to operate at the proper frequency. Ideally, the minimum return loss needs to be centered at 2445 MHz. 10 dB return loss looking into the antenna at the band edges is sufficient to achieve good range and receive sensitivity.

- Antenna impedance is 50 ohm.
  - This is maintained from balun to antenna feed.
  - The example uses microstrip topology but co-planer waveguide with ground can also be used if desired. In this case the dimensions will change so care should be taken when changing from one topology to another.
- The antenna should be reasonably clear of metallic objects and oriented properly with the ground plane.
- Always check the antenna in its final environment, including the PCB, components, case enclosure, hand effects (if appropriate), and battery. Plastic and other materials in the near-field may cause detuning.
- Actual antenna performance can be evaluated in a variety of ways, such as range testing, measuring radiated signal level under controlled conditions, and characteristic testing in an anechoic chamber.

8 Revision history

Table 1. Revision history

Rev. number	Date	Substantive change(s)
0	10/2015	Initial release
1	10/2015	All references to QFN changed to LQFN in section 1, “Introduction, section 5, “32-pin LQFN component copper layer and section 6, “32-pin LQFN package dimensions.

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