Freescale Semiconductor, Inc.
Application Note

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PCI Express® Certification Guide for the i.MX 6SoloX

1. Introduction

This document provides a description of procedures, tools, and criteria for the PCI Express® (PCIe) Gen1 and Gen2 electrical compliance tests for the i.MX 6SoloX Applications Processor.

2. Test equipment

2.1. Test board

The test is performed on the MCIMX6SX-SDB board.

2.2. Measurement equipment

This equipment is used to measure signal quality:

- Oscilloscope: Agilent DSO91304
- Cables and Adapters:
  - 2 Rosenberger SMP-SMP cables P/N: 71L-19K2-19K2-00305C
  - 4 Agilent SMA-SMP cables P/N: N4235-61602
  - 4 Agilent BNC connectors: P/N:54855-67604
- Test Fixture: CLB3.0 X1/X16

Contents

- Mini-PCIe cover to PCIe board

Figure 1. SMP-SMP cable

Figure 2. SMA-SMP cable

Figure 3. BNC connector

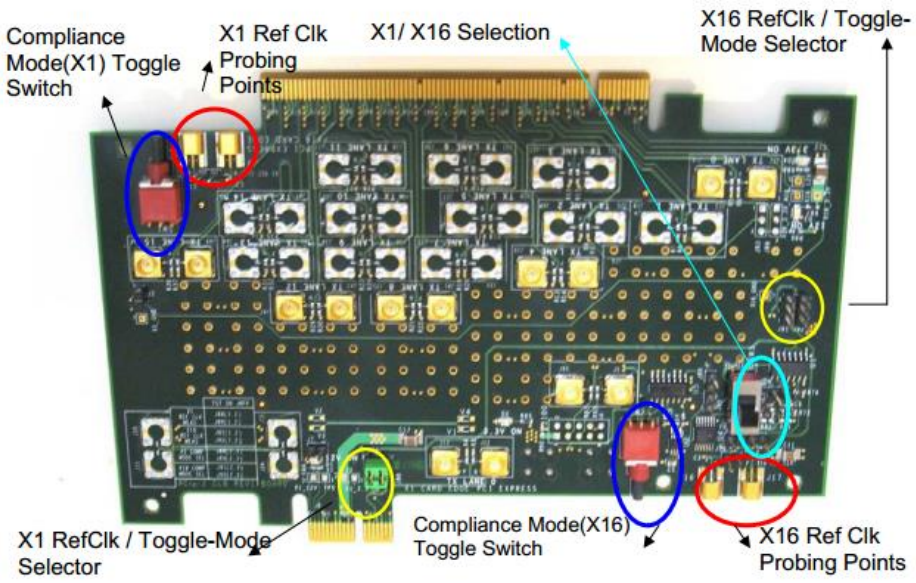

Figure 4. CLB3.0 X1X16 with key features

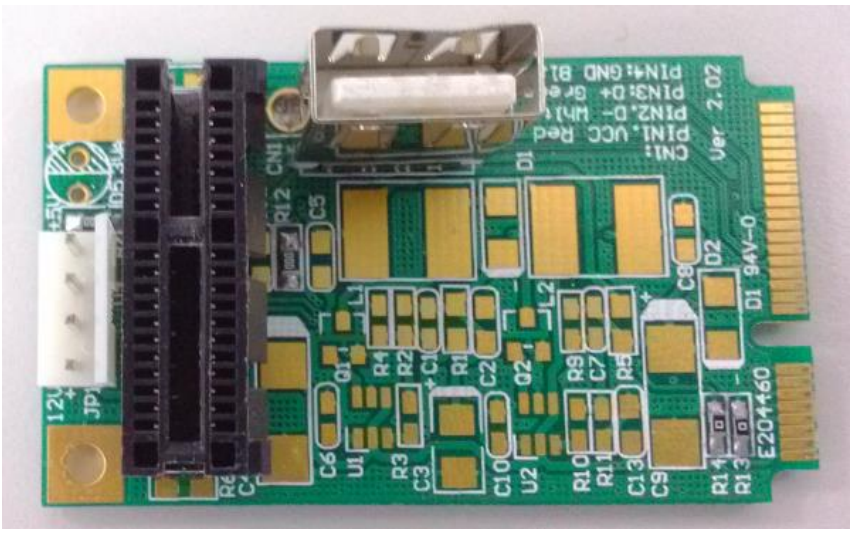

Figure 5. Mini-PCIe converter to PCIe board

2.3. Test environment

- Operation System: Linux® OS L3.10
- Additional software changes for PCIe compliance test based on L2.6.35_1.0.0 is required. To access software changes and updated test images, visit L3.10.53_1.1.0_iMX6QDLS_Bundle.

2.4. Analysis software

- N5393C PCI Express Test Application

2.5. Additional information

- Test items: only contains the electrical test.
- Test method and equipment operation:
  - See PCI Express® Architecture PHY Test Specification, Rev. 2.0. (PCI-SIG: 2008. Register at www.pcisig.com to download this document).
  - See PCI Express 2.0 CEM Signal Quality Testing for Add-in Cards using Agilent DSO/DSA91304A 13GHz and DSOX/DSAX93204A 16-32 GHz Real-Time Oscilloscopes, Version 1.2 (PCI-SIG, 20110. Register at www.pcisig.com to download this document).
- 100 MHz reference clock: internal PLL clock (default).
- 100 MHz reference clock: external PLL clock.

NOTE

The default clock source is the internal PLL clock. If the developer wants to use the external oscillator, rework on the i.MX 6SoloX SD board is required. See the PCIe clock notes in the i.MX 6SoloX SD board schematic for details.

3. PCIe Test basic procedures

The following is an overview of the test steps:

1. Perform scope calibration and cable de-skew, as explained in Appendix A.
2. Connect four BNC connectors to channel 1, 2, 3, and 4 of the oscilloscope.
3. Connect four SMA-SMP cables to the BNC connectors on the oscilloscope.
    a. Connect the SMP end of the SMA-SMP cable on channel 1 to the J13 on the CLB board, as it is the positive data line.
    b. Connect the SMP end of the SMA-SMP cable on channel 3 to the J12 on the CLB board, as it is the negative data line.
    c. Connect the SMP end of the SMA-SMP cable on channel 2 to the J16 on the CLB board, as it is the positive clock line (100 MHz).
    d. Connect the SMP end of the SMA-SMP cable on channel 4 to the J9 on the CLB board, as it is the negative clock line (100 MHz).
4. Insert the SD card (containing the PCIe test image) into the SD4 slot. Make sure the boot switches (SW10, SW11, and SW12) have been correctly set.
5. Connect the mini-PCIe converter to the PCIe daughter board. Proceed to connect that to the mini-PCIe connector (J15) on the i.MX6SX SDB board.
6. Connect the CLB board to the PCIe connector (CN3) on the mini-PCIe converter. Proceed to connect that to PCIe daughter board.

7. Configure the following on the CLB board:

   a. Change the slide switch SW3 to position the “x1 REF CLK” side as shown in the below figure.

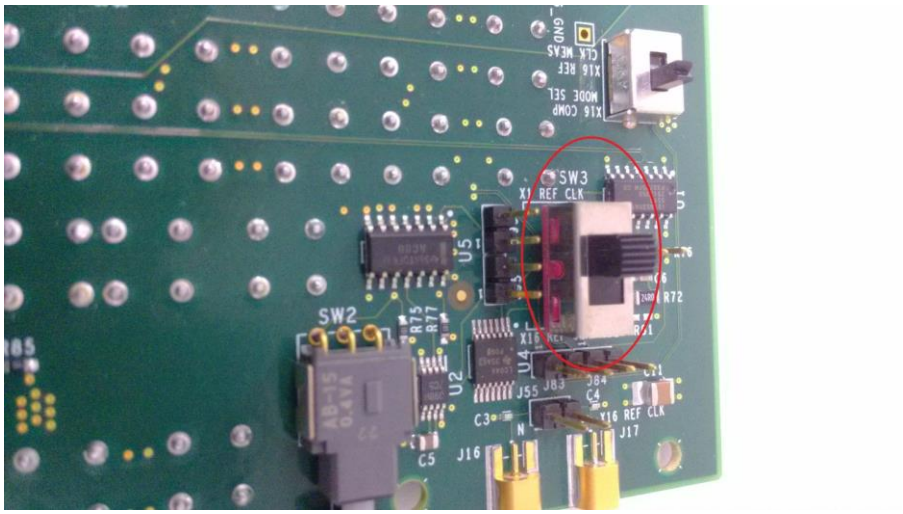

Figure 6. Switch SW3 setting

   b. Change the slide switch SW4 to position the “x1 REF CLK MEAS” side as shown in the below figure.

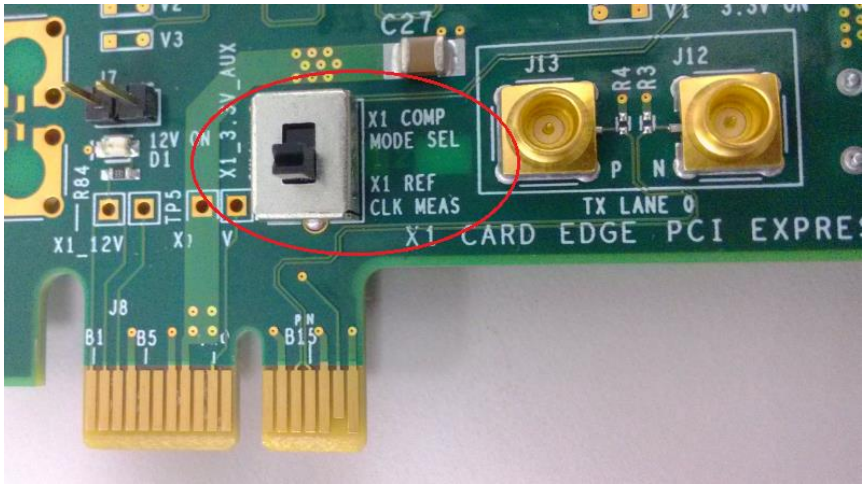

Figure 7. Switch SW4 setting

8. This figure displays the entire connection.

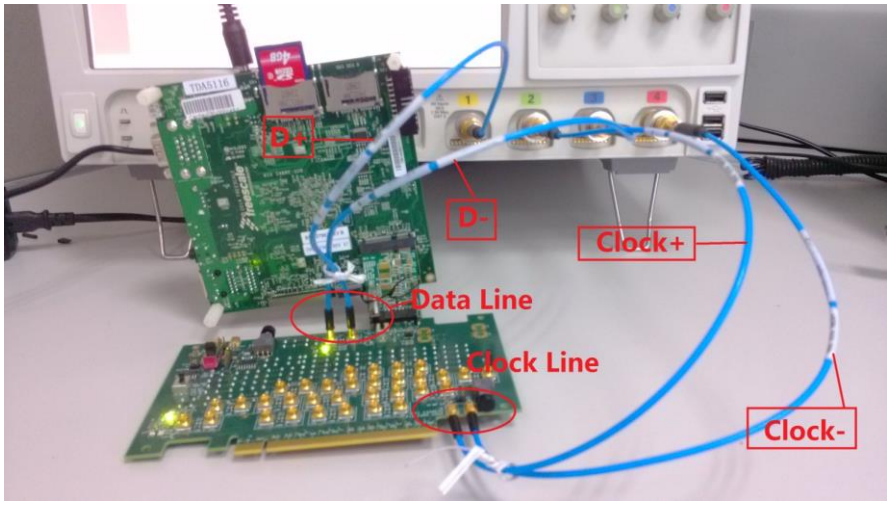

Figure 8. Whole connection

9. After all preparations are complete, power on the board and run the PCIe test software on the oscilloscope.

   Analyze->Automated Test Apps->N5393C PCIExpress Test App

   Choose the following options in the test software:

   a. In the ‘Device’ menu, choose the correct test mode. To perform the PCIe 1.1 tests, choose the ‘PCIe 1.1’ option.

   b. In the ‘Test Point’ menu, choose the ‘System Board Tests’ and ‘RefClk Tests’ options.

   c. In the ‘Test Information’ menu, choose the ‘Clean Clock’ option.

   d. In the ‘Data Lane’ menu, the x1 lane test is performed. There is no need to choose anything in this menu.

   e. For other options, keep the default value.

This figure displays all setup options.

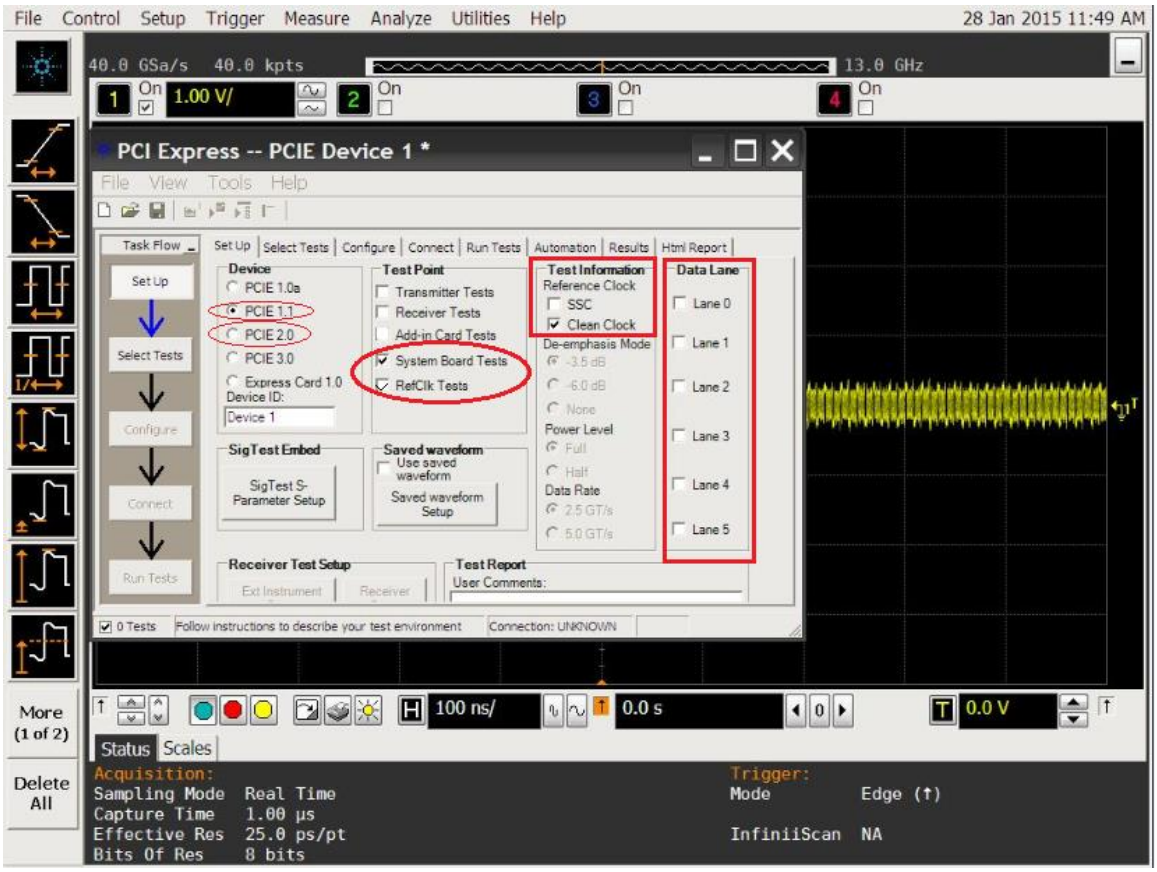

Figure 9. The setup configuration in the PCIe test software

10. In the “Select Tests’ option, choose ‘test all’.
11. In the ‘Connect’ option, check that all test cables have been connected properly.
12. If the developer wants to run the PCIe 1.1 test, select the ‘Run Tests’ option to begin the PCIe test.

13. If the developer wants to run the PCIe 2.0 test, other settings should be selected:

    a. Use the SMP-SMP cable to connect the J85 to J4. Use another SMP-SMP cable to connect the J5 to J87, as shown in this figure.

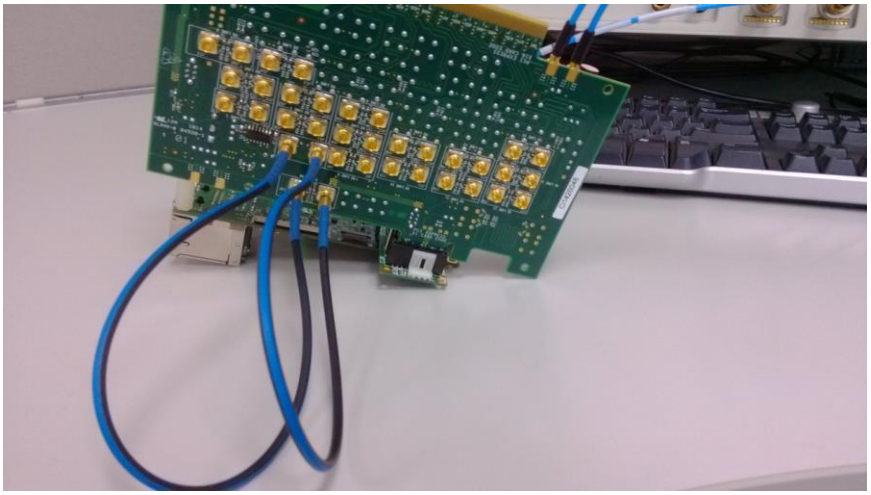

Figure 10. PCIe 2.0 test settings

    b. Change the slide switch SW4 to position “x1 COMP MODE SEL” and place with the side down, as shown in the figure below.

    c. Press SW1 switch to make sure distance between the closest-spaced adjacent crossover locations is around 200 ps (5 GT/s).

NOTE

Make sure the board is powered on before doing this configuration.

    d. Change the slide switch SW4 back to position “x1 REF CLK MEAS”.

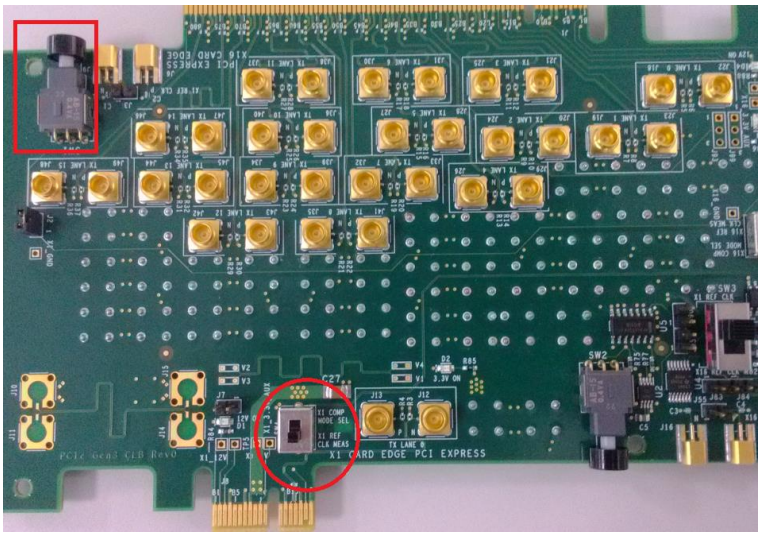

Figure 11. SW1 and SW4 settings at PCIe 2.0 test

4. PCIE Test results

On the i.MX6SX SDB board, the internal clock is the default. When performing the PCIe test, the developer needs to test the Eye-Width, Phase jitter, Rising Edge Rate, and so on. The test report provides detailed test results.

4.1. PCIE 1.1 test results – Internal clock

The detailed settings have been described in Section 3 of this document. After the test, the developer can see the test results, as shown in the figure below.

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	System Board Tx, Unit Interval (PCIE 1.1)	400.0730 ps	19.6 %	399.8800 ps <= VALUE <= 400.1200 ps
✓	0	1	System Board Tx, Template Tests (PCIE 1.1)	Pass	100.0 %	Pass/Fail
✓	0	1	System Board Tx, Median to Max Jitter (PCIE 1.1)	26.94 ps	65.0 %	VALUE <= 77.00 ps
✓	0	1	System Board Tx, Eye-Width (PCIE 1.1)	333.89 ps	35.7 %	VALUE >= 246.00 ps
✓	0	1	System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 1.1)	665.8 mV	42.3 %	274.0 mV <= VALUE <= 1.2000 V
✓	0	1	System Board Tx, Peak Differential Output Voltage (NonTransition)(PCIE 1.1)	683.4 mV	45.4 %	253.0 mV <= VALUE <= 1.2000 V
✓	0	1	Reference Clock, Phase Jitter (PCIE 1.1)	63.04 ps	26.7 %	VALUE <= 86.00 ps
✓	0	1	Reference Clock, Rising Edge Rate (PCIE 1.1)	750 mV/ns	4.4 %	600 mV/ns <= VALUE <= 4.00 V/ns
✓	0	1	Reference Clock, Falling Edge Rate (PCIE 1.1)	770 mV/ns	5.0 %	600 mV/ns <= VALUE <= 4.00 V/ns
✓	0	1	Reference Clock, Differential Input High Voltage (PCIE 1.1)	291 mV	94.0 %	VALUE >= 150 mV
✓	0	1	Reference Clock, Differential Input Low Voltage (PCIE 1.1)	-296 mV	97.3 %	VALUE <= -150 mV
✓	0	1	Reference Clock, Average Clock Period (PCIE 1.1)	77 ppm	37.2 %	-300 ppm <= VALUE <= 300 ppm
✓	0	1	Reference Clock, Duty Cycle (PCIE 1.1)	51.0 %	45.0 %	40.0 % <= VALUE <= 60.0 %
✓	0	1	Reference Clock, Variation of VCross (PCIE 1.1)	33.8 mV	75.9 %	VALUE <= 140.0 mV
✓	0	1	Reference Clock, Absolute Max Input Voltage (PCIE 1.1)	233.5 mV	79.7 %	VALUE <= 1.1500 V
✓	0	1	Reference Clock, Absolute Min Input Voltage (PCIE 1.1)	-68.3 mV	77.2 %	VALUE >= -300.0 mV
✓	0	1	Reference Clock, Rise-Fall Matching (PCIE 1.1)	7.15 %	64.3 %	VALUE <= 20.00 %

Figure 12. PCIe 1.1 test results

The developer can access the main results of the PCIe 1.1 test. More detailed information is available in the test report from https://community.freescale.com/docs/DOC-106210.

4.2. PCIE 1.1 test results – External clock

Some rework is required on the i.MX6SX SDB board to be able to choose the external clock for the PCIe test. This is shown in the figure below.

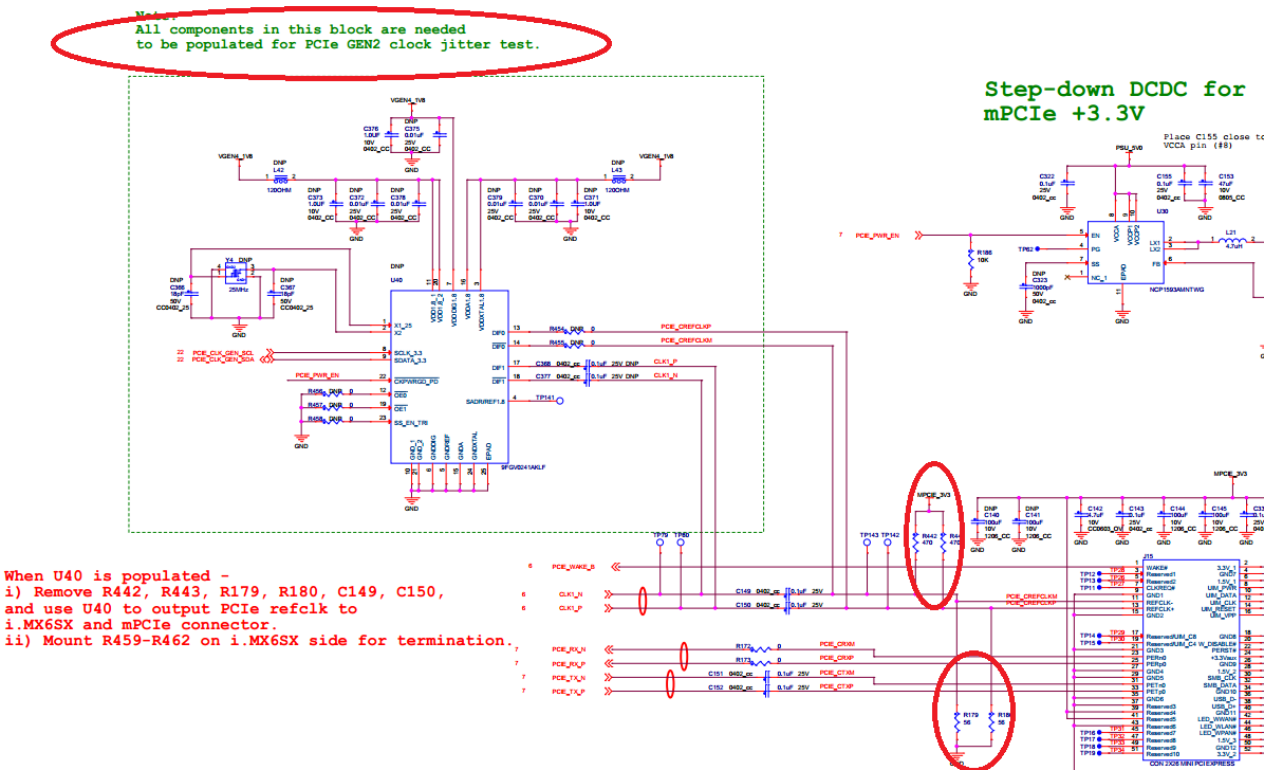

Figure 13. Rework when using external clock

The rework instructions (located on page 16 of the schematic revision C):

1. The area outlined in green defines all components that need to be populated.
2. Remove R442, R443, R179, R180, C149, and C150.
3. Populate the R459, R460, R461, and R462 for termination resistors (HCSL-to-LVDS). Directions are located on page 6 of the schematic.

The other settings are the same with the PCIe 1.1 test – Internal clock configuration. The test result is shown in the figure below.

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	System Board Tx, Unit Interval (PCIE 1.1)	400.0710 ps	20.4 %	399.8800 ps <= VALUE <= 400.1200 ps
✓	0	1	System Board Tx, Template Tests (PCIE 1.1)	Pass	100.0 %	Pass/Fail
✓	0	1	System Board Tx, Median to Max Jitter (PCIE 1.1)	22.92 ps	70.2 %	VALUE <= 77.00 ps
✓	0	1	System Board Tx, Eye-Width (PCIE 1.1)	343.42 ps	39.6 %	VALUE >= 246.00 ps
✓	0	1	System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 1.1)	706.8 mV	46.7 %	274.0 mV <= VALUE <= 1.2000 V
✓	0	1	System Board Tx, Peak Differential Output Voltage (NonTransition)(PCIE 1.1)	1.0594 V	14.8 %	253.0 mV <= VALUE <= 1.2000 V
✓	0	1	Reference Clock, Phase Jitter (PCIE 1.1)	25.24 ps	70.7 %	VALUE <= 86.00 ps
✓	0	1	Reference Clock, Rising Edge Rate (PCIE 1.1)	1.60 V/ns	29.4 %	600 mV/ns <= VALUE <= 4.00 V/ns
✓	0	1	Reference Clock, Falling Edge Rate (PCIE 1.1)	1.56 V/ns	28.2 %	600 mV/ns <= VALUE <= 4.00 V/ns
✓	0	1	Reference Clock, Differential Input High Voltage (PCIE 1.1)	410 mV	173.3 %	VALUE >= 150 mV
✓	0	1	Reference Clock, Differential Input Low Voltage (PCIE 1.1)	-410 mV	173.3 %	VALUE <= -150 mV
✓	0	1	Reference Clock, Average Clock Period (PCIE 1.1)	53 ppm	41.2 %	-300 ppm <= VALUE <= 300 ppm
✓	0	1	Reference Clock, Duty Cycle (PCIE 1.1)	49.9 %	49.5 %	40.0 % <= VALUE <= 60.0 %
✓	0	1	Reference Clock, Variation of VCross (PCIE 1.1)	34.4 mV	75.4 %	VALUE <= 140.0 mV
✓	0	1	Reference Clock, Absolute Max Input Voltage (PCIE 1.1)	407.1 mV	64.6 %	VALUE <= 1.1500 V
✓	0	1	Reference Clock, Absolute Min Input Voltage (PCIE 1.1)	-12.4 mV	95.9 %	VALUE >= -300.0 mV
✓	0	1	Reference Clock, Rise-Fall Matching (PCIE 1.1)	16.90 %	15.5 %	VALUE <= 20.00 %

Figure 14. PCIe 1.1 – External clock test result

The developer can access the main results of the PCIe 1.1 test. Additional information is available in the test report from PCIE 1.1 test report_External Clock.pdf.

4.3. PCIe 2.0 test results – External clock

When performing the PCIe 2.0 test, make sure the board rework is the same as the rework for the PCIe 1.1 - External clock case.

NOTE

To perform the PCIe 2.0 test, follow step 13 in Section 3.

The figure below displays the test results after performing the PCIe 2.0 test.

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	System Board Tx, Unit Interval (PCIE 2.0, 5.0 GT/s)	200.0110 ps	40.8 %	199.9400 ps <= VALUE <= 200.0600 ps
✓	0	1	System Board Tx, Template Tests (PCIE 2.0, 5.0 GT/s)	Pass	100.0 %	Pass/Fail
✓	0	1	System Board Tx, Peak Differential Output Voltage (Transition) (PCIE 2.0, 5.0 GT/s)	467.8 mV	18.6 %	300.0 mV <= VALUE <= 1.2000 V
✓	0	1	System Board Tx, Peak Differential Output Voltage (Non Transition)(PCIE 2.0, 5.0 GT/s)	923.2 mV	30.8 %	300.0 mV <= VALUE <= 1.2000 V
✓	0	1	System Board Tx, Eye-Width with crosstalk (PCIE 2.0, 5.0 GT/s)	133.56 ps	40.6 %	VALUE >= 95.00 ps
✓	0	1	System Board Tx, RMS Random Jitter with crosstalk (PCIE 2.0, 5.0 GT/s)	3.006 ps	93.7 %	VALUE <= 48.000 ps
✓	0	1	System Board Tx, Maximum Deterministic Jitter with crosstalk (PCIE 2.0, 5.0 GT/s)	24.148 ps	57.6 %	VALUE <= 57.000 ps
✓	0	1	System Board Tx, Total Jitter at BER-12 with crosstalk (PCIE 2.0, 5.0 GT/s)	66.443 ps	36.7 %	VALUE <= 105.000 ps
✓	0	1	System Board Tx, Eye-Width without crosstalk (PCIE 2.0, 5.0 GT/s)	133.56 ps	23.7 %	VALUE >= 108.00 ps
✓	0	1	System Board Tx, RMS Random Jitter without crosstalk (PCIE 2.0, 5.0 GT/s)	3.006 ps	93.7 %	VALUE <= 48.000 ps
✓	0	1	System Board Tx, Maximum Deterministic Jitter without crosstalk (PCIE 2.0, 5.0 GT/s)	24.148 ps	45.1 %	VALUE <= 44.000 ps
✓	0	1	System Board Tx, Total Jitter at BER-12 without crosstalk (PCIE 2.0, 5.0 GT/s)	66.443 ps	27.8 %	VALUE <= 92.000 ps
✓	0	1	Reference Clock, High frequency > 1.5MHz RMS Jitter (Common Clk) (PCIE 2.0, 5.0 GT/s)	1.77 ps	42.9 %	VALUE <= 3.10 ps
✓	0	1	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Common Clk) (PCIE 2.0, 5.0 GT/s)	480 fs	84.0 %	VALUE <= 3.00 ps
✓	0	1	Reference Clock, High frequency > 1.5MHz RMS Jitter (Data Clk) (PCIE 2.0, 5.0 GT/s)	2.05 ps	48.8 %	VALUE <= 4.00 ps
✓	0	1	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Data Clk) (PCIE 2.0, 5.0 GT/s)	460 fs	93.9 %	VALUE <= 7.50 ps

Figure 15. PCIe 2.0 test report

The developer can access the main results of the PCIE 1.1 test. More detailed information is available in the test report from https://community.freescale.com/docs/DOC-106210.

5. Revision history

This table provides a revision history for the document.

Table 1. **Revision history**

Revision number	Date	Substantive changes
0	07/2015	Initial release

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