Freescale Semiconductor
Application Note

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Hardware Design Considerations for MC12311 and MKW01x Sub-GHz Devices

1 Introduction

This application note describes Printed Circuit Board (PCB) design considerations for the MC12311 and MKW01x 60-pin LGA package. Included are layouts of the component copper layer, solder mask, and solder paste stencil. These recommendations are guidelines only and may need to be modified depending on the assembly house used and the other components on the board.

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2 60-Pin LGA Component Copper Layer

Figure 1 shows a recommended component copper layer. This layer is also referred to as the top metal layer and is the layer to which the components are soldered. The footprint for the 60-pin LGA package consists of 60 IC contact pads and a centered ground pad. The centered ground pad has the copper pattern as shown in Figure 1. Use 0.23 mm via holes to connect to the ground plane layers. These are required for RF grounding and help prevent solder float.

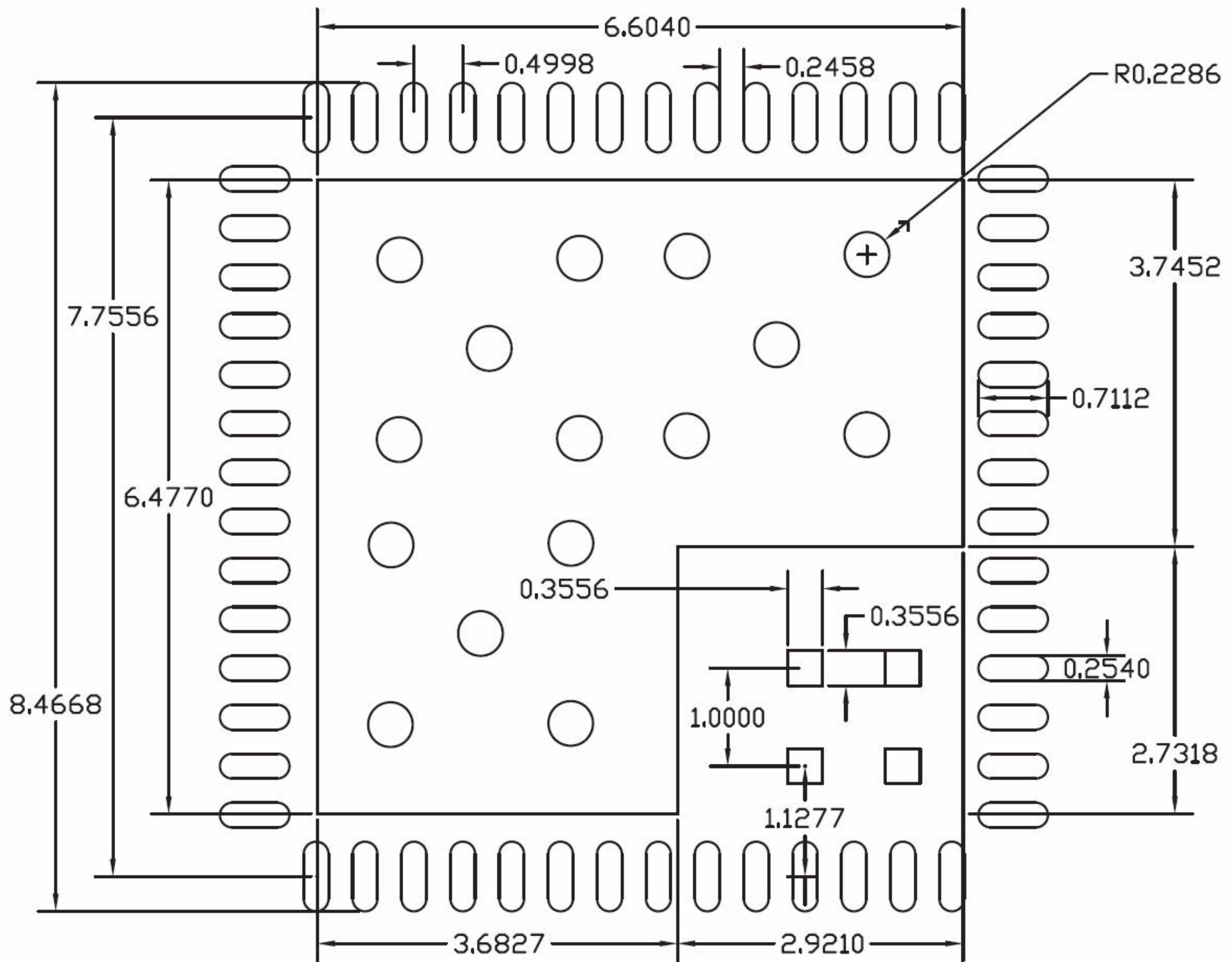

Figure 1. LGA Component Copper Layer

2.1 60-Pin LGA Solder Mask

The solder mask limits the flow of the solder paste during the reflow process. Figure 2 shows a recommended solder mask pattern. The pattern represents openings in the solder mask.

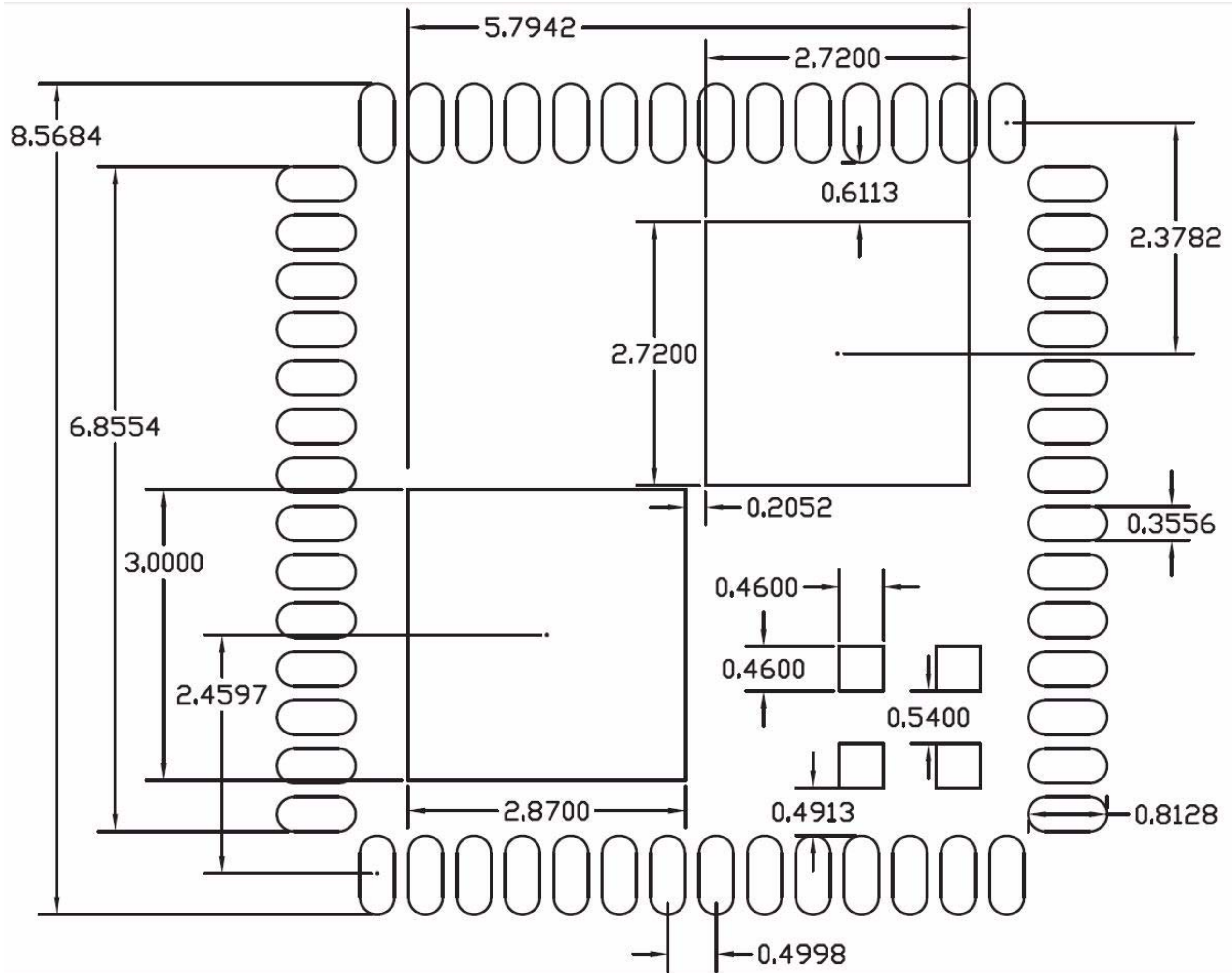

Figure 2. 60-Pin LGA Solder Mask Pattern

2.2 60-Pin LGA Solder Paste Stencil

The solder paste stencil controls the pattern and thickness of the solder paste dispensed on the board. Figure 3 shows a recommended solder stencil pattern. Stencil thickness should be approximately 0.1 mm.

Other patterns and opening sizes can be used if too much solder is being applied. See Section 2.2.1, “LGA Package Problems with Excess Solder,” for more information.

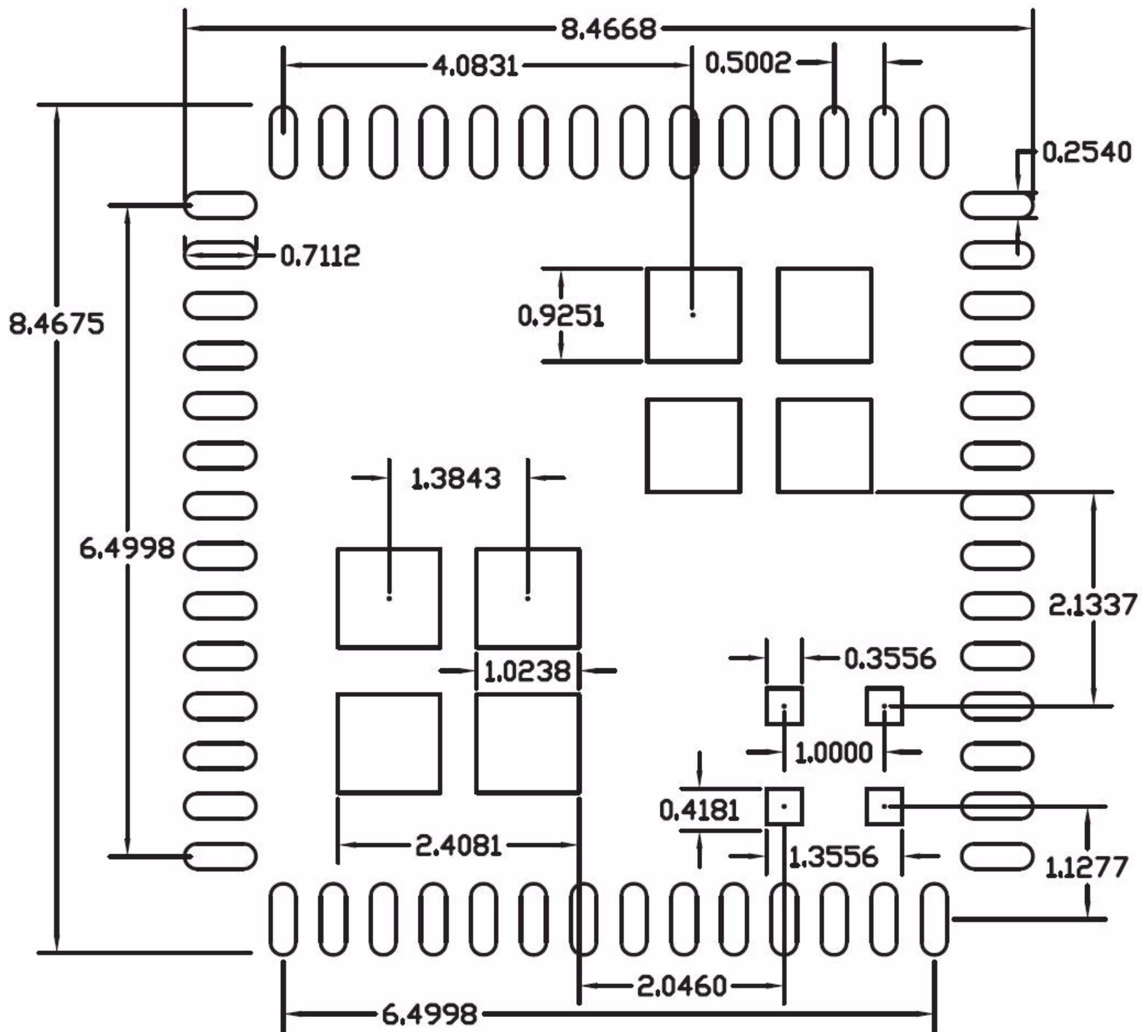

Figure 3. 60-Pin LGA Solder Stencil Pattern

2.2.1 LGA Package Problems with Excess Solder

Excess solder may cause the LGA package to “float” or bridge between the package contacts. To use the correct amount of solder paste applied to the PCB, take into consideration the following:

- Stencil thickness
- Other components mounted on the PCB
- Manufacturing equipment
- Assembly house experience

3 60-Pin LGA Package Dimensions

Figure 4 shows the 60-pin LGA package dimensions.

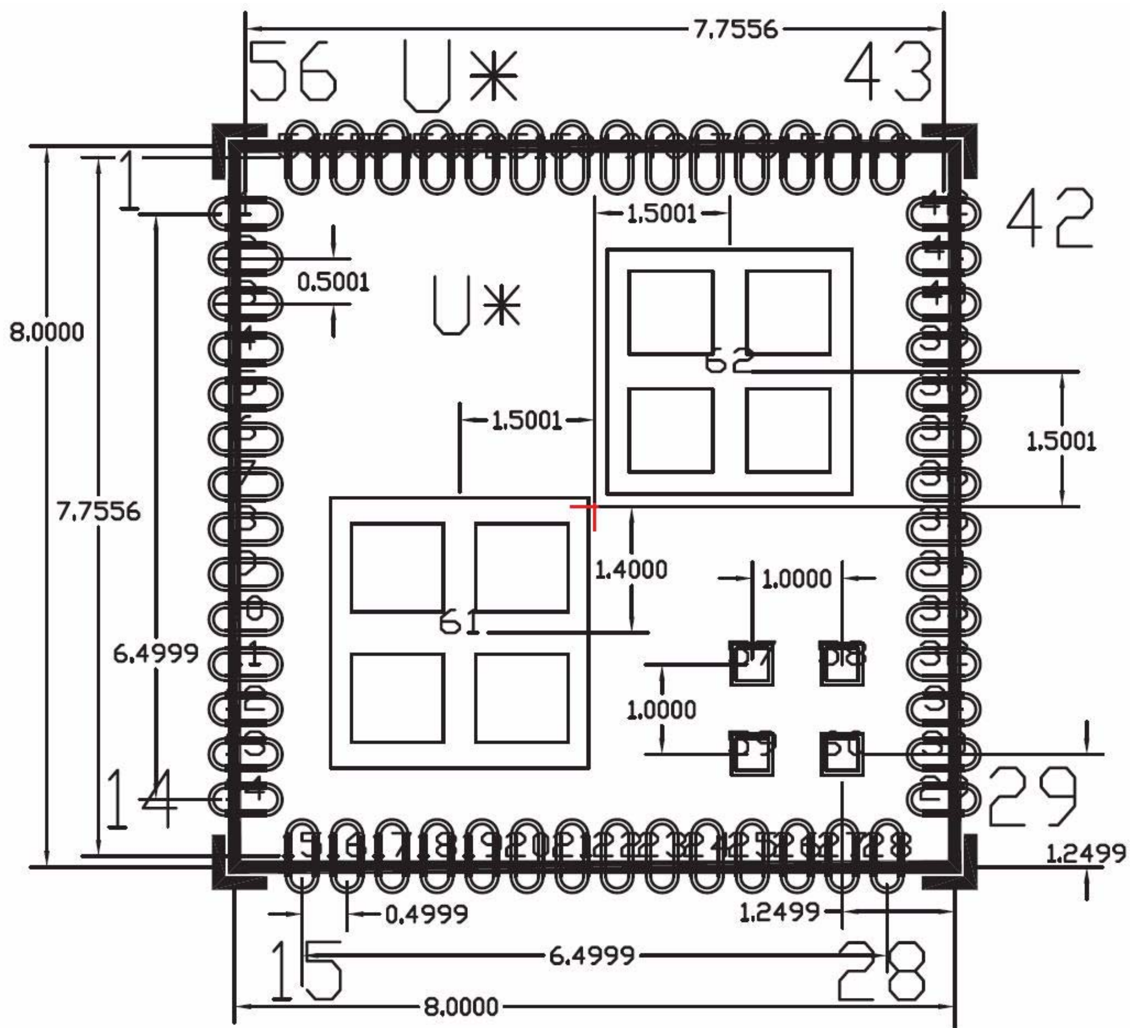

Figure 4. 60-Pin LGA Package Dimensions

3.1 60-Pin LGA Device Marking Details

The MC12311 and MKW01x devices are in the 60-pin LGA (8x8 mm), Case 1664-01. The following figure show device marking examples for the MC12311 device.

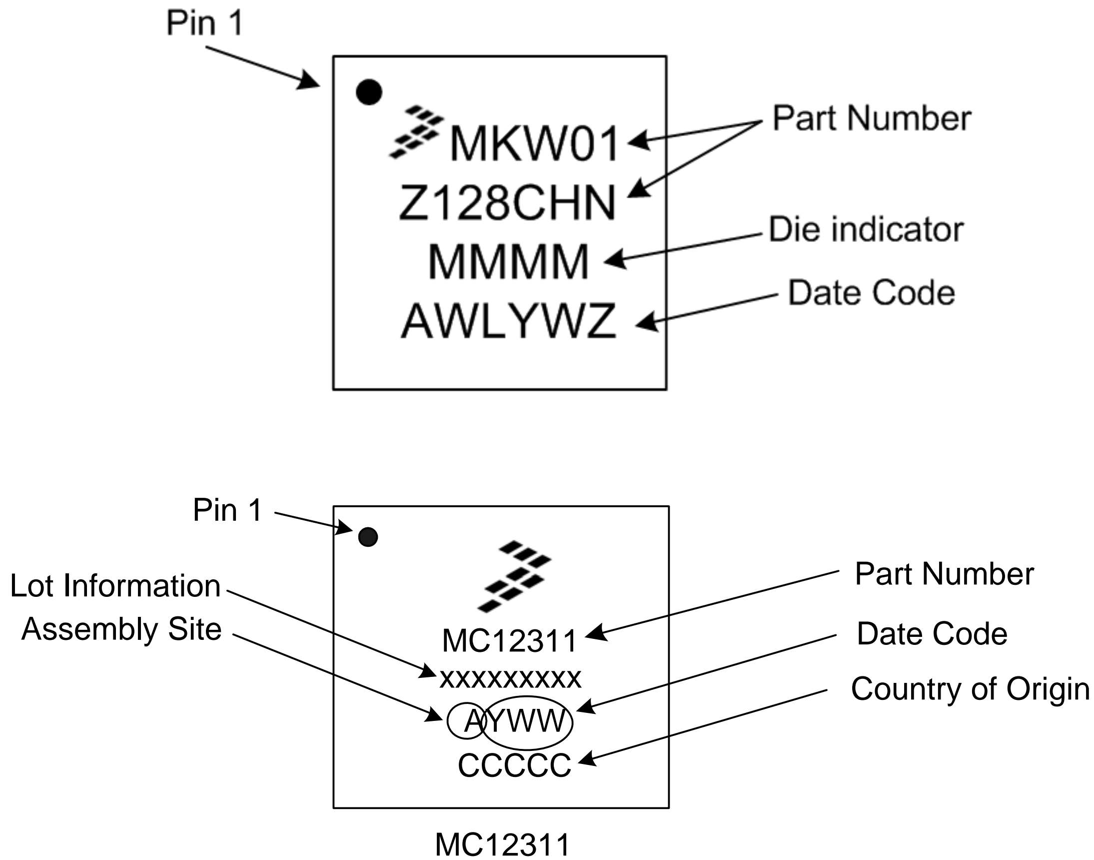

Figure 5. MKW01 and MC12311 Device Marking

3.2 60-Pin LGA Tape and Reel

Tape and Reel packaging is available for the LGA-60 package. Reels are available to support the requirements of both first and second generation pick-and-place equipment. The packaging fully conforms to the latest EIA-481A specification. The antistatic embossed tape provides a secure cavity, sealed with a peel-back cover tape.

Embossed Tape and Reel facilitates automatic pick-and-place equipment feed requirements. The tape is the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the peel.back cover tape.

- Two Reel Sizes Available (7 inch and 13 inch)
- Used for Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA 481, -1, -2

- Tape
  - — Freescale part number L10001A055
  - — Supplier Part number ML0707-AC
- Reel
  - — Freescale part number 57ARL10510D004
  - — Supplier Part number TX16-07-W1
  - — Reel Critical Dimensions:
    - – A 13" diameter
    - – B 7" hub
    - – W1 to suit 16 mm width

Figure 6 shows an example tape and reel mechanical drawing.

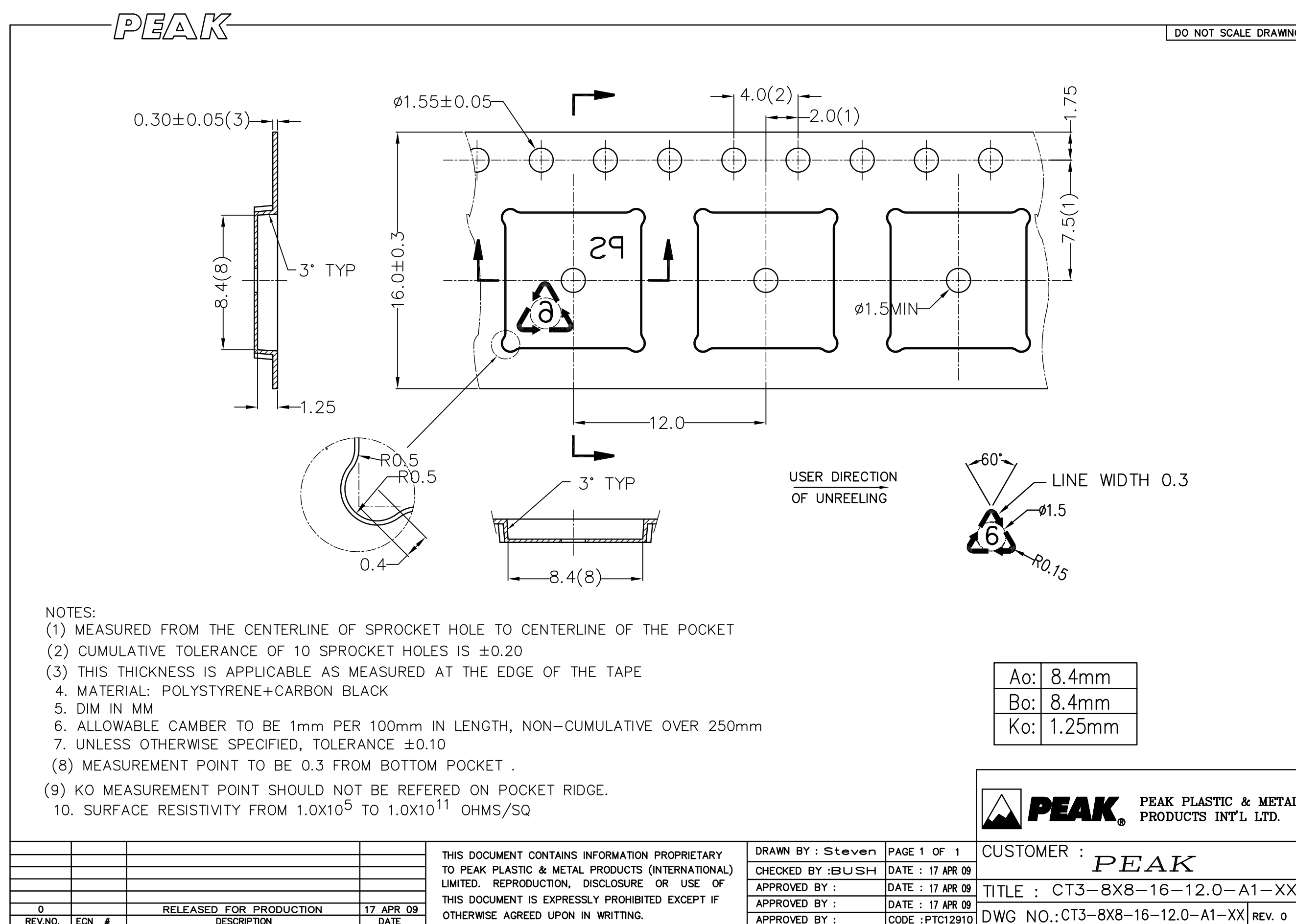

Figure 6. Example 60-Pin LGA Tape and Reel Detailed Mechanical

4 60-Pin LGA Soldering Profile

Figure 7 shows the soldering profile Freescale uses and recommended for the MC12311 and MKW01x 60-pin LGA package, in a board size approximately 2”x2”.

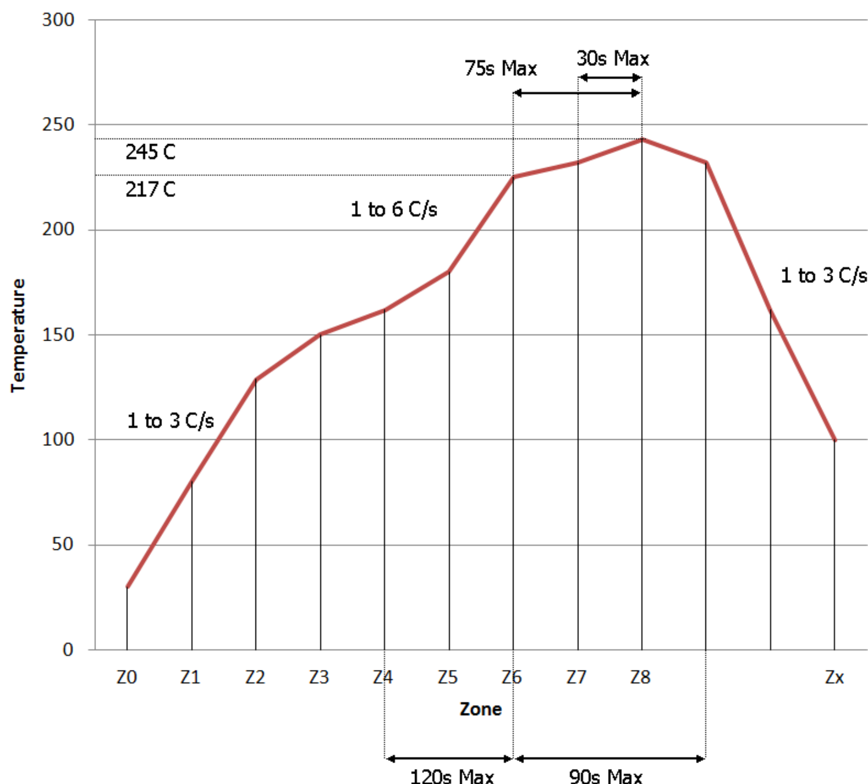

Figure 7. Soldering Profile 60-Pin LGA

5 Design and Board Layout Consideration

To have successful wireless hardware development, the proper device footprint, RF layout, circuit matching, antenna design and RF measurement capability are essential. RF circuit design, layout and antenna design are specialties requiring investment in tools and experience. With Freescale’s available hardware reference designs, RF design considerations and guidelines herein, hardware engineers can successfully design sub-GHz radio boards with good performance.

The device footprint and layout are critical and affect the RF performance by the design implementation. For these reasons, use of the Freescale recommended RF hardware reference designs are important for first time successful board performance. Additionally, the reference platforms have been optimized for radio performance. If the recommended footprint and design are followed exactly in the RF region of the board; sensitivity, output power, harmonic and spurious radiation, and range will have a high likelihood first time success.

The following subsections describe important considerations when implementing a wireless hardware design starting with the device footprint, RF circuit implementation, and antenna selection. Figure 1,

below, shows an example of a typical layout exhibiting the critical RF sections which should be copied exactly for best radio performance. The less critical layout area, mostly the digital circuitry of the board, can be modified without degrading radio performance.

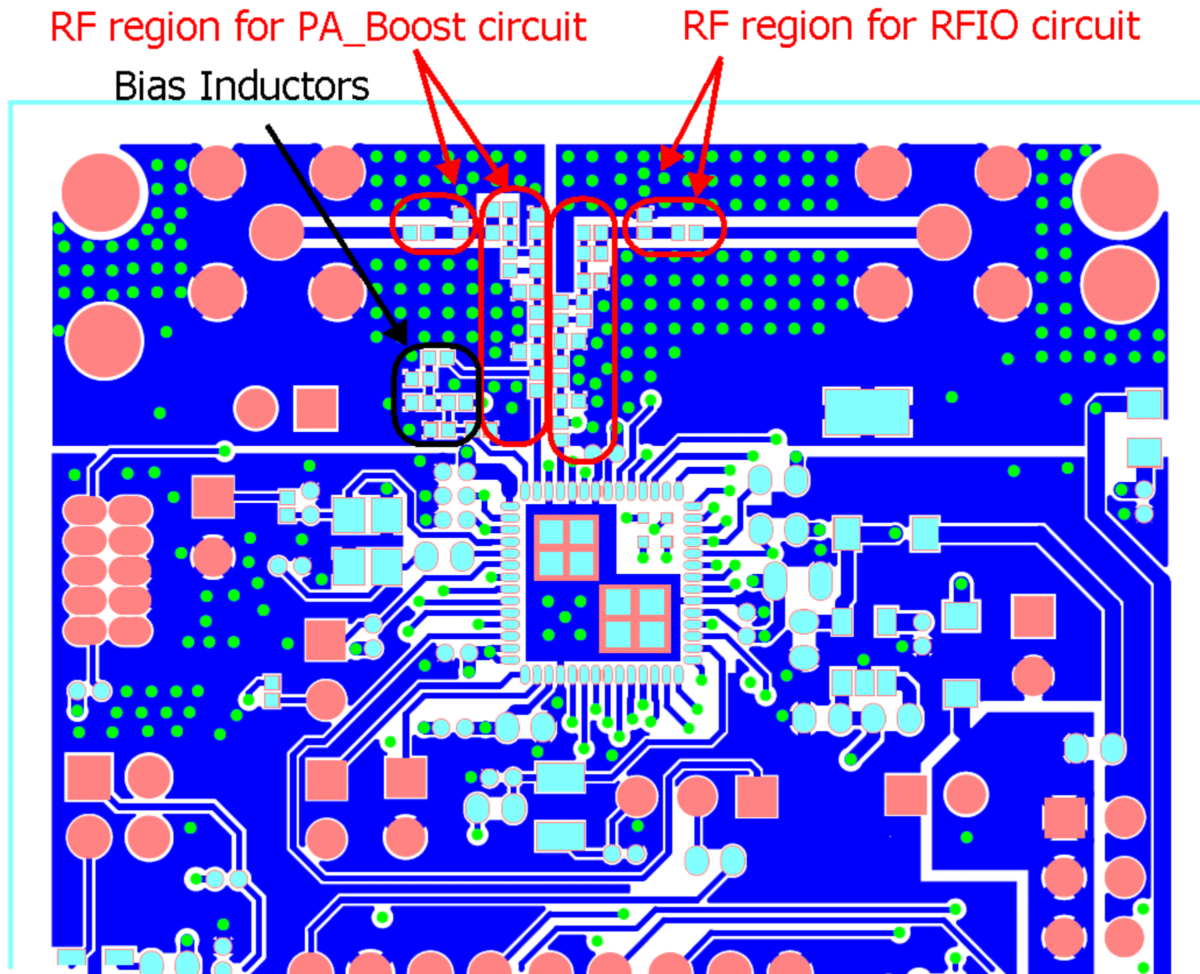

Figure 8. MKW01 MRB Layout, RF Section

The MKW01 (the reference board shown above is MRB-KW01) and the MC12311 sub-GHz transceiver parts have two RF connections. The RFIO path is for transmit and receive; the PA_Boost is for transmit only.

Those components are the RF path components shown in this region of the schematic:

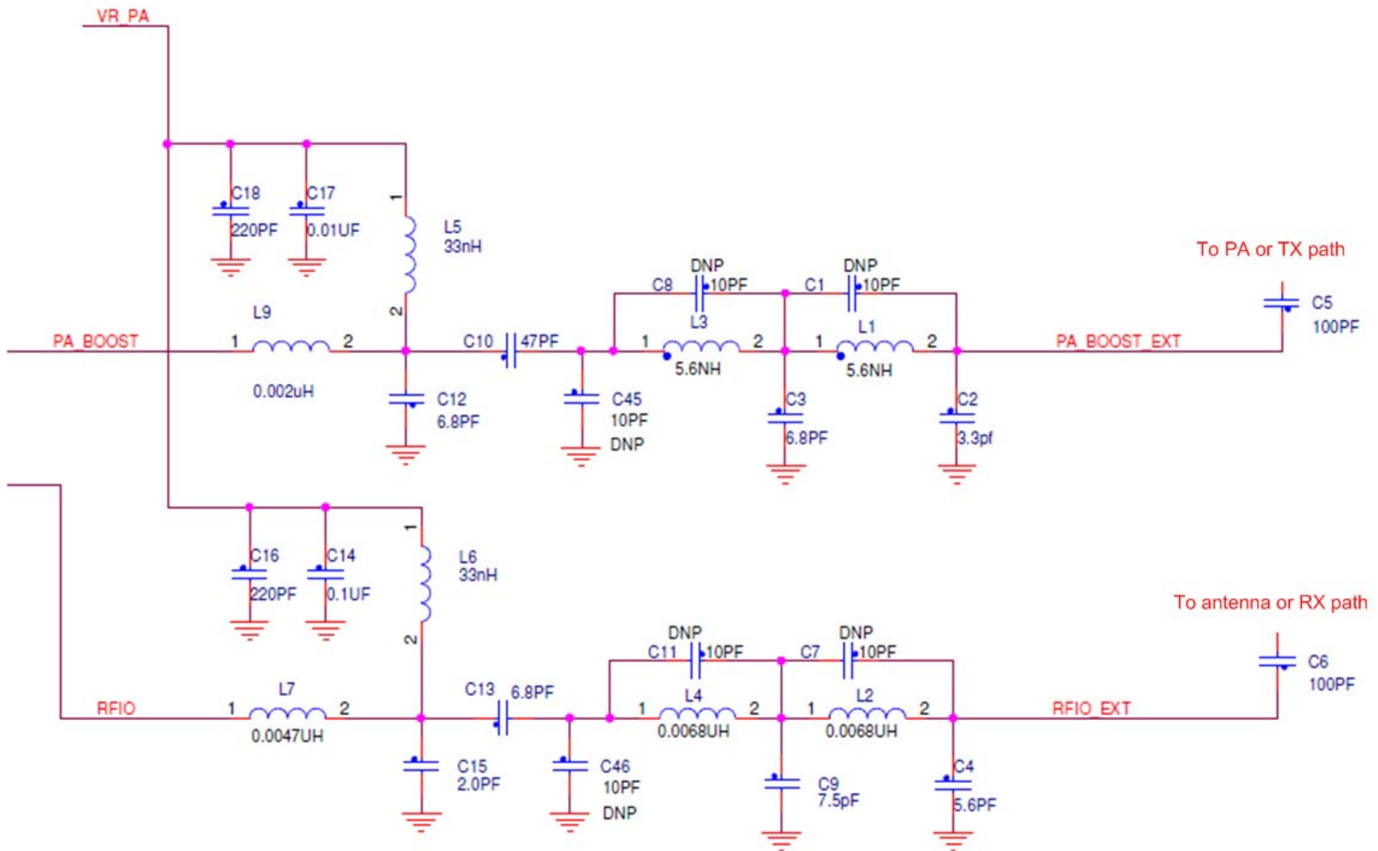

Figure 9. MKW01 MRB Schematic, RF Section

The left side circuitry boxed in red of Figure 8 above corresponds to the upper component path in Figure 9, the PA_Boost path. The right side circuitry boxed in red of Figure 8 above corresponds to the lower component path in Figure 9, the RFIO path.

The circuitry in each path consists of a few components to match the impedance to the filter and a low pass filter to reject harmonics on the transmit signal.

Copying the schematic and layout exactly, including the board material and dielectric thickness and the ground circuitry underneath will enhance the likelihood of RF performance matching the MRB and success with the first board layout.

5.1 Board Layers

The recommended board stackup for either a two-layer or four-layer board design is as follows:

- Two-layer stackup
  - Top - RF routing of transmission lines, signals, and some ground
  - Bottom - RF reference ground, signal routing, and general ground
- four-layer stackup
  - L1 (Top) - RF routing of transmission lines, some ground fill
  - L2 - RF reference ground
  - L3 - DC power
  - L4 (Bottom) - Signal routing

5.2 MKW01 Device Footprint

The performance of RF circuitry can be influenced by the devices footprint. As a result, a great deal of care has been put into creating a footprint that provides appropriate grounding and signal connections to ensure receiver sensitivity and output power are optimized. Freescale highly recommends copying the IC region of the PC board component layer exactly as it is shown in Figure 1 and Figure 10; this includes via locations as well. Changes in this region of the layout can cause performance changes from the Freescale reference design.

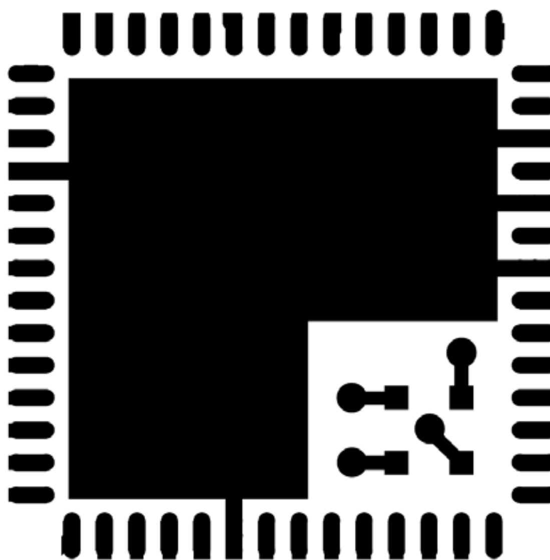

Figure 10. Close-In View of MKW01 Footprint on Freescale Reference Design MRB (Pin 1 Is Upper Left)

Note that several pins are ground and are connected with a trace directly to the ground flag under the part. In most of these cases the other side of each of the pins has a short trace leading to a via hole to the internal ground plane on layer 2. This ensures a low-inductance path to ground where needed.

The four bottom-side connections are not RF critical and are shown with a short trace to a via hole connecting to some internal trace to an optional test point. Normally there will not be any external connection to those four bottom-side contacts (they are internal SPI connections between the MCU and Transceiver on the MKW01 or MC12311) other than an optional test point. If traces are routed to test points care should be taken to avoid coupling RF or noise.

A board layout technique used by some designers or in some applications is to separate the grounding of the RF or analog circuitry from that of the digital circuitry.

As can be seen in Figure 4, the package dimensions, There are two ground flags on the bottom of the part. Figure 11, shows a suggested footprint with those two ground pads separated and identified as to which is RF ground and which is Digital ground.

Likewise, the layer 2 ground plane should be split to separate the RF ground from the Digital ground. The RF ground is the layer 2 reference ground under the RF components and all microstrip lines, extending underneath the RF ground flag footprint of the device. The digital ground will fill layer 2 for most of the rest of the board. The two grounds are typically joined at 1 part, typically a power entry point and sometimes with an inductor to pass DC but not RF. (Pin 4 in Figure 11 is connected to the inner layer digital ground.)

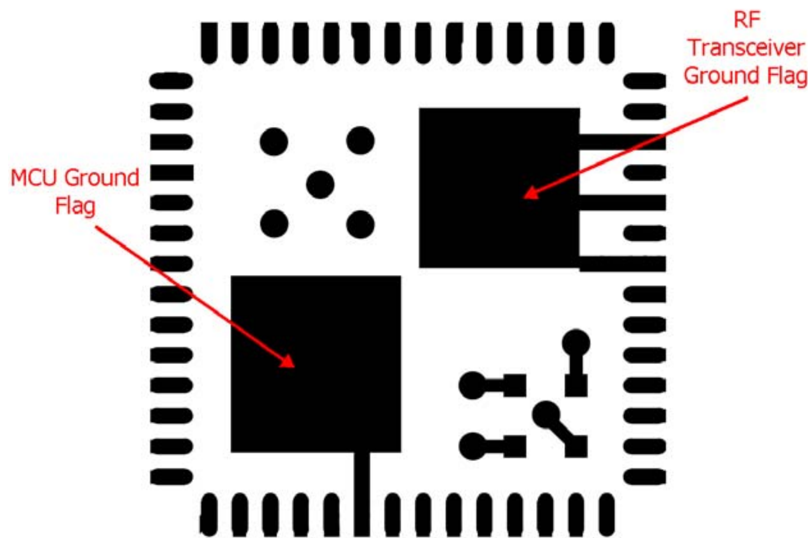

Figure 11. Close-In View of Suggested MKW01 Footprint Concept with Separate RF and Digital Grounds (Pin 1 Is Upper Left)

If such a separated ground concept is being implemented, a group of via holes should be implemented connecting each ground pad to the appropriate layer 2 ground plane just below it.

5.3 Signal Trace and Ground Considerations

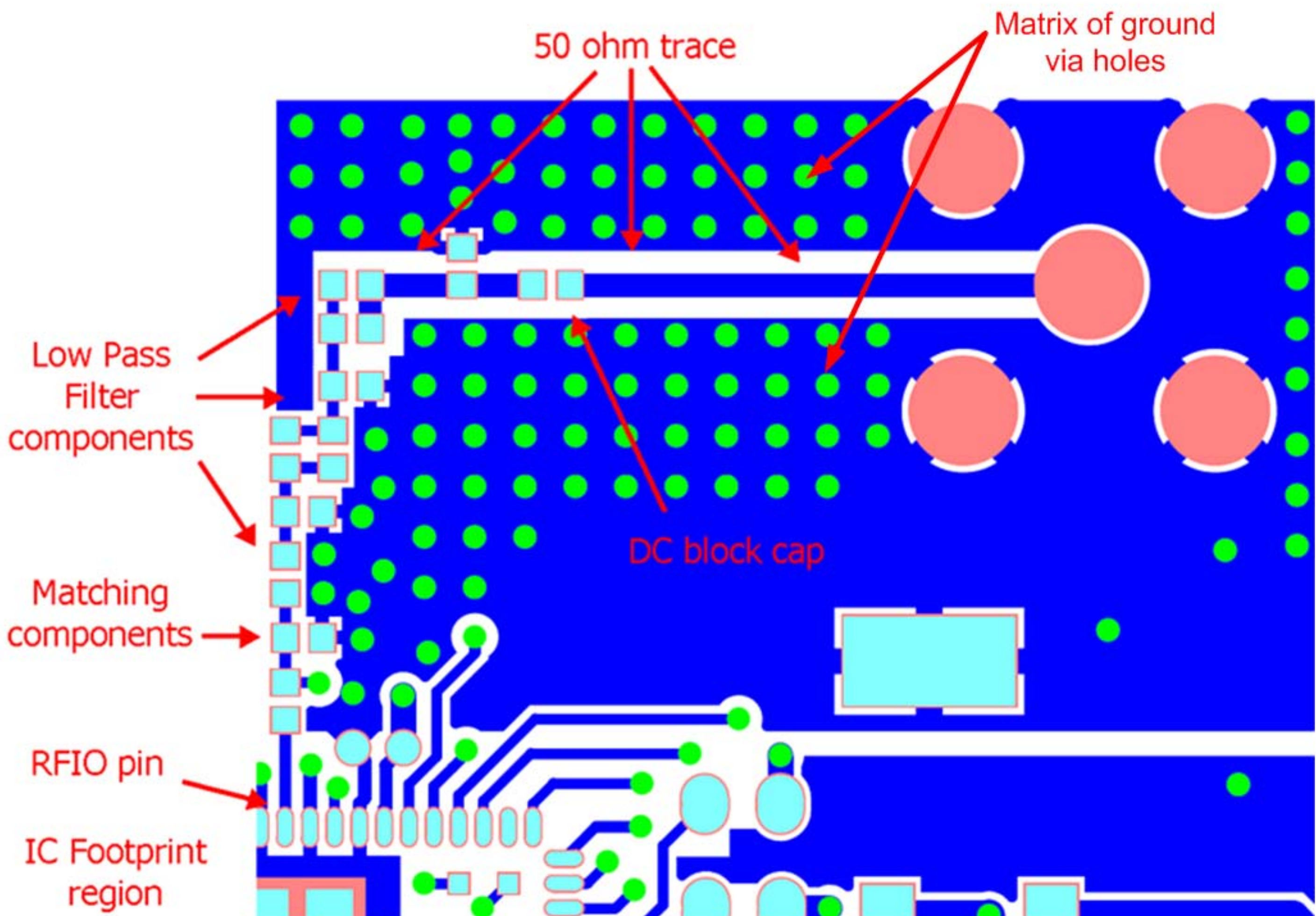

Figure 12. Close-In View of the RFIO Output Path Matching and Filter Component Footprints and 50 ohm RF Signal Trace Shown

Figure 12 shows the RFIO path on the MRB-KW01 (this board is same for all frequency band variants). To accommodate the physical placement of the transceiver with the nearby RF matching large RF connector, a long length of 50 Ohm trace is required. (It appears long in the figure but it is actually only about 1 cm.)

For the MRB-KW01 reference design the board is designed as a 4 layer board with the top layer (layer 1) as signal and layer 2 as ground (see Section 5.1, “Board Layers”). Between layer 1 and layer 2, the thickness and dielectric constant were chosen such that a 50 ohm line is 18 mils wide. These board parameters must be controlled and the fabrication drawing mandates the line width for 50 ohms. This allows the board fabricator flexibility in layer thickness and dielectric constant so long as the 50 ohm trace is maintained.

If line length is used as a series matching element or if line widths are used to create matching elements using lengths of line in impedances other than 50 ohms then the thickness and dielectric constant should be specified independently because the electrical length of a signal trace is proportional to (the square root of) dielectric constant and the relationship between trace width, impedance and dielectric constant is not linear. The formulas for microstrip impedance and electrical length are publicized and there are numerous online calculators that can be used in design.

Within a 50 ohm system such as between the antenna and the 50 ohm, a length of 50 ohm trace will have no effect on the impedance presented to the device. (There may be insertion loss however, so it is best to keep trace lengths short.) However any length of trace in the midst of a non-50 ohm system (such as inside the matching network or filter) will behave like a series inductor and will perturb the impedances inside the structure. Likewise component solder pads wider than, or extending beyond the 50 ohm trace, will act as a small capacitor to ground affecting the impedance. These effects are typically negligible for a physically small circuit at 450 or 900 MHz. If the circuit is copied exactly, or nearly exactly, from the reference design, similar performance can be expected. To meet mechanical design considerations, board layout changes to the matching and harmonic filter circuitry may be desired, so empirical optimization of component values may improve performance.

It is common practice to extend ground plane into unused regions of layer 1. Layer 1 ground should be connected to layer 2 ground with a large number of via holes, also identified in Figure 12 above. Top layer ground should be kept far enough away from RF signal traces to avoid perturbing the line impedance, typically a line width or further.

The MRB-KW01 reference design uses standard FR-4 fiberglass-epoxy PC board material. For circuits in the frequency ranges and power levels of this family of parts, this material offers very good electrical and mechanical performance at competitive cost. Lower RF insertion loss can be achieved by using high-performance and high-cost PC board materials but this is typically not required. Low loss PC board material typically has a different dielectric constant and available thicknesses so line lengths and widths in artwork designed for fiberglass epoxy boards may not result in the proper impedances in any other material.

Avoid any non-ground trace routing on the ground layer that will result in disrupting the ground under the RF traces. See Section 5.1, “Board Layers,” for recommended layer and ground assignment.

Avoid routing of digital, analog, power, or baseband traces near or parallel to RF transmission lines or RF bias lines. RF signals will couple to these traces causing crosstalk, noise or signal distortion. Avoid routing traces with RF or switching signals in a manner that is not inherently shielding. The microstrip used for RF traces tends to be somewhat shielding due to the proximity of the ground plane and the line impedance. A trace routed without a ground plane or a trace routed through a header with vertical pins (the type used for jumpers) could act as an antenna, resulting in unintentional radiation of the signal or noise. The CLKOUT signal of the MKW01 is routed to the MCU EXTAL input via jumper J8. This structure provided an easy to change option for testing clocking on the evaluation board but resulted in some unintentional radiation of the CLKOUT signal and is not recommended for production.

Freescale’s current family of sub-GHz transceiver parts use only single-ended inputs and outputs for RF interface. Therefore baluns and differential line structures are not required and are not discussed in this document.

5.4 Thermal Relief for Components at the Ground Plane

Many components, connectors, and header pins must be soldered to ground. The ground plane can be nearly as large as the board itself and may extend over 2 or more layers. This thermally conductive plane of copper can draw heat away from the solder joint during assembly, potentially causing uncontrolled solidification and reliability issues. It will also draw away heat from the soldering operation during board rework, complicating that process.

The component pads attached to ground can be thermally isolated while electrically connected using thermal relief structures as shown in Figure 13.

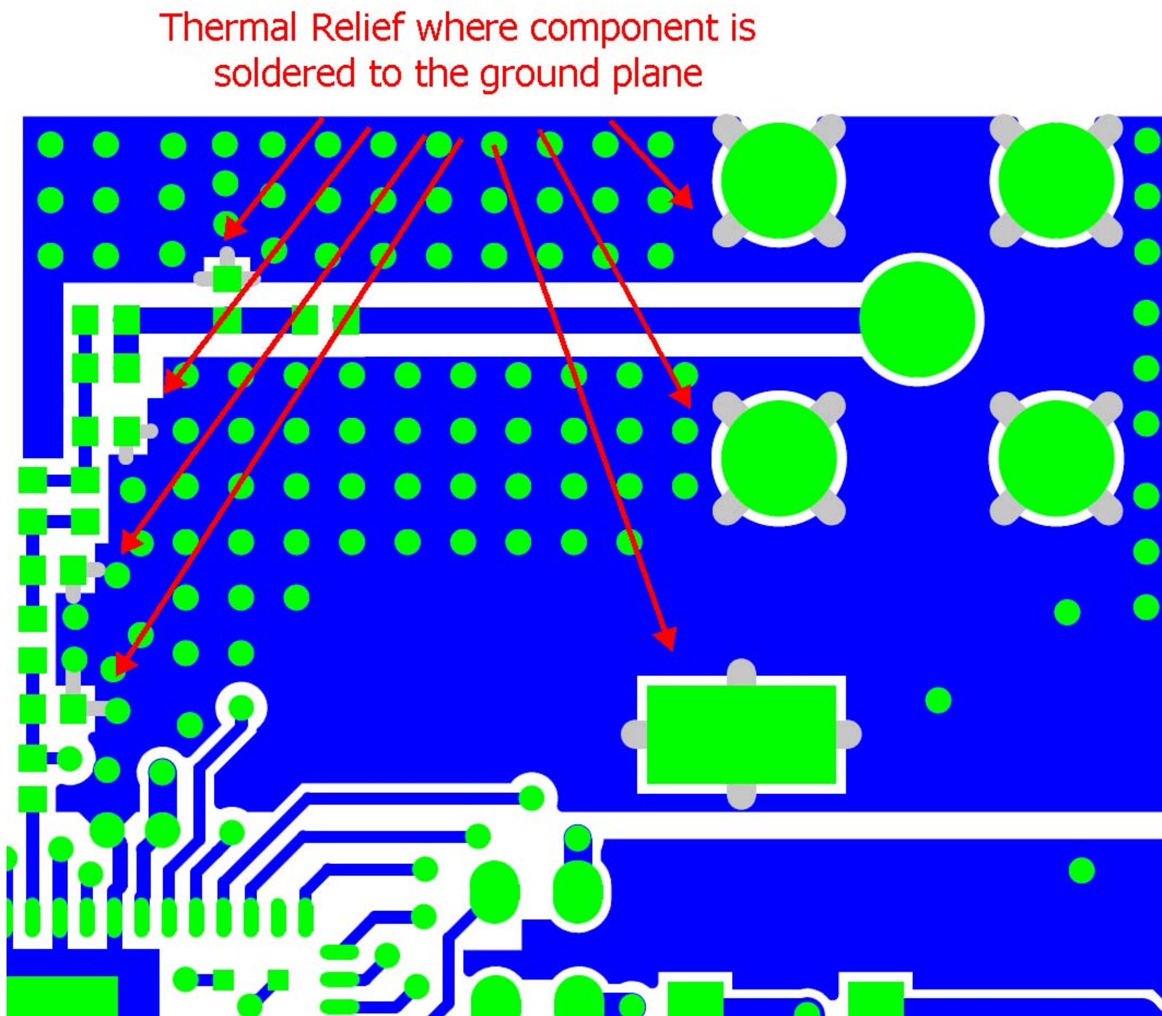

Figure 13. Same Region as Shown in Figure 12 with Thermal Reliefs Connections Identified and Highlighted in Grey

For sub-GHz circuits, the thermal relief should be kept electrically short and there should be multiple via holes to appropriate ground layers as close to the structure as practical.

Do not copy any of the artwork images in this document. Rather, build footprints using the dimensions in Figure 1, Figure 2, and Figure 3 of this document and Figures 8 and 9 of the MKW01Z128 Data Sheet. Or copy them from the MRB-KW0x Design Files package, KW01-MRB_PCBRD.zip, which is available on the Freescale.com website under Hardware Development Tools, on the Downloads tab of the MRB-KW0x section. The design files include the board layout for the MRB-KW01, which can be used as a starting point in a new product development.

5.5 Antenna selection

Freescale often recommends printed antennas for our 2.4 GHz connectivity products. Such antennas can use a large amount of PC board area when implemented on 900 MHz products and will be twice as large yet for 450 MHz products.Therefore we have not implemented a printed antenna on our reference design for sub-GHz, but include a connector mounted antenna with MRB-KW01. Any 50-ohm antenna for the desired frequency range may be substituted.

A naturally-large product may have room for a full-sized printed antenna on the PC board. Alternately, there are commercial chip antennas for various bands available that are often quite small, which can allow a very small form-factor product to use sub-GHz frequency bands. Compared to the large connector-mounted antennas supplied with the MRB, performance degradation can be expected with reduced-size antennas and various antenna configurations should be analyzed and experimented with in developing a sub-GHz product.

Conversely, performance enhancement can be realized with larger directional antennas. Directional antennas might be considered for a non-moving, point-to-point installation where the link distance is long and path loss is high.

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