Freescale Semiconductor
Application Note

Document Number: AN3835
Rev. 0, 6/2009

MC9S08SG32 Series High-Temperature Devices Design Considerations

by: Han Lin
Applications Engineer, Austin, Texas

1 Introduction

Comprehensive real-time monitoring and intelligent management of in-car electronics are becoming more important as users want safer, more fuel saving, and reliable driving experience. To meet these needs, microcontrollers need to be placed near electronics such as sensors and actuators to provide responsive decision making. Placing MCUs near these devices can reduce latency, minimize loss of data, and cut costs that may otherwise be present with lengthy and complex wire routing.

Automotive electronic devices often operate in areas beyond standard temperatures. MCUs nearby are also required to withstand high temperature stress. Freescale's 8-bit MC9S08SG32 series of high temperature microcontrollers are designed to qualify for the automotive AECQ100 Grade 0 standard and are capable of high temperature operations, up to 150 °C ambient temperature.

This document provides design considerations and guidelines for automotive designers when using the AECQ100 Grade 0 MC9S08SG32 in a high temperature environment.

Contents

1 Introduction 1
2 AECQ100 Standards 2
3 Package Reliability at High Temperatures 3
4 Thermal Design Considerations 3
4.1 Maximum Junction Temperature (T_J) 3
4.2 Power Dissipation (PD) Capability 4
4.3 Power Dissipation (PD) 4
4.4 Optimizing T_J 5
5 Chip Internal Reference Clock 6
5.1 ICS Version 2 Introduction 6
5.2 Clock Accuracy Over Temperature Range 7
5.3 Application Example Using SCI 8
6 Conclusion 10

© Freescale Semiconductor, Inc., 2009. All rights reserved.

freescale™ semiconductor

2 AECQ100 Standards

AEC-Q100 outlines test standards and conditions required before passing the automotive qualification. AEC-Q100 is governed by the Automotive Electronic Committee (AEC), one of the most recognized quality standards in the global automotive industry.

Different grades under the AEC-Q100 depend on operational temperature conditions. Freescale's MC9S08SG32 series is qualified under the AEC standard and offers both Grade 0 and Grade 1 devices.

Where:

- AEC Grade 0 devices are qualified for –40 °C to 150 °C ambient temperature.
- AEC Grade 1 devices are qualified for –40 °C to 125 °C ambient temperature.

Table 1 highlights critical accelerated environmental and lifetime stress tests from the AEC-Q100. Compared to the MC9S08SG32 ACE Grade 1, AEC Grade 0 devices undergo more hours, cycles, and a larger safeguard temperature range. This ensures the AEC Grade 0 device can endure up to a 150 °C high ambient temperature. For more details, see: http://www.aecouncil.com/AECDocuments.html.

Table 1. Highline of AEC-Q100 Grade 1 and Grade 0

Test name	Test symbol	Condition	Test method	Unit	AEC Grade 0 (ambient operating temperature – 40 to 150 °C)	AEC Grade 1 (ambient operating temperature – 40 to + 125 °C)
Temperature cycling	TC	–65°C to 175°C	JEDEC JESD22-A104	cycles	500	—
		–50°C to 175°C			1000	—
		–50°C to 150°C			2000	—
		–65°C to 150°C			—	500
		–50°C to 150°C			—	1000
Highly accelerated stress test	HAST	130°C/85%RH	JESD22-A101 or A110	hours	96	96
High temperature operating life	HTOL	175°C Ta	JESD22-A108	hours	408	—
		150°C Ta			1000	408
		125°C Ta			—	1000
Early life failure rate	ELFR	175°C Ta	AEC Q100-008	hours	24	—
		150°C Ta			48	24
		125°C Ta			—	48
NVM endurance and operational life	EDR	175°C Ta	AEC Q100-005	hours	1000	500
		150°C Ta			2000	1000

3 Package Reliability at High Temperatures

The reliability of electronic components can be affected when operating at elevated temperatures. Extensive and extended testing such as moisture sensitivity level 3 (MSL3), wire pull tests, ball shear tests, and temperature cycling were conducted to ensure that the SG32 AEC Grade-0 devices are capable of enduring a high temperature environment.

4 Thermal Design Considerations

It is critical to ensure that the MCU does not operate outside of its maximum allowable thermal specifications. Operating outside of the specification can lead to MCU internal damage or malfunction.

The most important thermal parameter that designers need to abide by is the maximum junction temperature (T_{Jmax}). T_{Jmax} is a function of parameters such as power dissipation and thermal resistance of the chosen package. Thermal resistance (θ_{JA}) is the ability of the device package to allow the dissipation of internal heat. This section first takes a top-down approach to help you understand how these factors affect the junction temperature and then discusses ways to minimize junction temperature on SG32 devices.

4.1 Maximum Junction Temperature (T_J)

Junction temperature is not ambient temperature. Ambient temperature is the temperature outside of the silicon package. The junction temperature is the temperature of the silicon inside of the package. The junction temperature is also referred to as the die temperature.

When modeling the thermal design it is necessary to ensure the sum of all parameters that contribute to the increase of the junction temperature to not exceed the maximum T_J value specified in the data sheet.

The following Equation 1 for chip-junction temperature (T_J) in °C can be used to govern thermal dissipation on MC9S08SG32 parts. It provides a good reference to help designers estimate important parameter values for thermal considerations.

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textbf{Eqn. 1}$$

Equation 1 is a reference from the *MC9S08SG32 Data Sheet*.

Where:

T_A = Ambient temperature, °C.

θ_{JA} = Package thermal resistance, junction-to-ambient, °C and W

$P_D = P_{int} + P_{I/O}$, PD can be understood as source of heat flux (Watts)

$P_{int} = I_{DD} \cdot V_{DD}$, Watts — MCUs internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

Table 2 specifies that the maximum junction temperature is 135 °C for the MC9S08SG32 AEC Grade 1 standard packages (◆) and 155°C for AEC Grade 0 packages (◆). Table 2 shows that the package with more pin counts has less thermal resistance, therefore better heat dissipation. Use a four-layer PCB board over a single-layer board for better heat dissipation.

Table 2. Referenced from MC9S08SG32 Data Sheet-Thermal Characteristics

Rating	Symbol	Value		Unit	Temp Rated	
					Standard	AEC Grade 0
Thermal resistance Single-layer board		Airflow at 200 ft/min	Natural Convection			
28-pin TSSOP	θ_{JA}	71	91	°C/W	◆	◆
20-pin TSSOP		94	114		◆	—
16-pin TSSOP		108	133		◆	◆
Thermal resistance Four-layer board						
28-pin TSSOP	θ_{JA}	51	58	°C/W	◆	◆
20-pin TSSOP		68	75		◆	—
16-pin TSSOP		78	92		◆	◆
Maximum junction temperature	T_J	135		°C	◆	—
		155			—	◆

4.2 Power Dissipation (PD) Capability

Power dissipation capability ($PD_{capability}$) can be understood as the maximum power generation allowed on the MCU to keep T_J below the maximum T_J.

$PD_{capability}$ can be obtained by reworking Equation 1 to the following Equation 2:

$$PD_{capability} = (T_{Jmax} - T_A)/(\theta_{JA}) \quad \textbf{Eqn. 2}$$

For example, if a 28-pin TSSOP is selected for a four-layer board design and the target product maximum ambient temperature is at 140°C, then:

PDcapability = (TJmax – TA)/ (qJA)

= (155°C – 140°C) / (58°C /W)

= 0.258W

4.3 Power Dissipation (PD)

The power dissipation on the MCU can be estimated with Equation 3. When calculating the PD, designers need to keep in mind that PD must be less than the calculated $PD_{capability}$ so that T_J does not exceed T_{Jmax}.

$$PD = P_{int} + \Sigma P_{I/O} \quad \textbf{Eqn. 3}$$

Where:

$P_{int} = I_{DD} \cdot V_{DD}$, Watts — MCU internal power
$\sum P_{I/O}$ = Sum of Power dissipation on input and output pins

NOTE

Power dissipation of each pin can be understood as the current flow in or out of a pin multilpied by the voltage supplied to the MCU (V_{DD}). Regardless of the direction of the current flow, this current will pass through the internal die. The *MC9S08SG32 Data Shee*t specifies that the total current of all the pins used must not exceed 50 mA (|50mA| = | –50mA|) for AEC Grade 0 devices and 100 mA (|100mA| = | –100mA|) for Grade 1 devices. When calculating $\sum P_{I/O}$, ensure the total I_{OH} and I_{OL} current do not exceed these specifications.

Table 3. Referenced from the MC9S08SG32 Data Sheet — DC Characteristics

Num	C	Characteristic		Symbol	Condition	Min	Typ	Max	Unit	Standard	AEC Grade 0
3	D	Output high current	Max total I_{OH} for all ports	I_{OHT}	V_{OUT} < V_{DD}	0	—	–100	mA	◆	—
						0	—	–50	mA	—	◆
5	D	Output low current	Max total I_{OL} for all ports	I_{OLT}	V_{OUT} > V_{SS}	0	—	100	mA	◆	—
						0	—	50	mA	—	◆

4.4 Optimizing T_J

Expanding from Equation 1, gives the following Equation 4.

$$T_J = T_A + PD \times \theta_{JA}$$
$$T_J = T_A + (P_{int} + P_{I/O}) \times \theta_{JA}$$
$$T_J = T_A + [(I_{DD} \times V_{DD}) + P_{I/O}] \times \theta_{JA}$$

Eqn. 4

Equation 4 displays the mathematical relationship between the T_J and its parameters. Reducing the parameters' values keeps the junction temperature lower so that it maintains below T_{Jmax}. The following are tips to reduce the T_J while allowing other parameters to have a higher value.

- Reducing P_{int} ($I_{DD} \times V_{DD}$) — Decrease the MCU current consumption (I_{DD}) by configuring the MCU to run at the lowest bus speed allowed by the application, or keeping the V_{DD} to the minimal operational voltage if possible.
- Reducing θ_{JA} — Select a PCB that has good heat sink (for example a 4 layer board rather than a 1 layer board).
- Reducing $P_{I/O}$ — Limit current flowing on the I/O pins.
- Reducing T_A — Increase air flow circulation around the MCU.

5 Chip Internal Reference Clock

The MC9S08SG32 can run from either an external clock or from a built-in internal reference clock. Many designers prefer the internal clock for cost effectiveness and space saving. The built-in reference clock has a deviation due to the temperature range. Discussed here is the basic concept for the internal reference clock and how to use it to emulate its deviation due to a large temperature range.

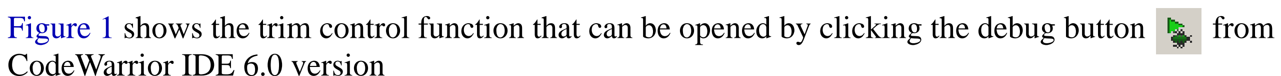
5.1 ICS Version 2 Introduction

The MC9S08SG32 uses an ICS V2 peripheral for configuring different clock sources that can be used by the MCU. The ICS V2 contains an internal clock that is normally called the 32 kHz internal reference clock. This clock can be multiplied by a factor of 1024 to produce a higher core speed, up to 40 MHz on AEC Grade 1 devices, and up to 36 MHz on AEC Grade 0 devices. The internal reference clock speed can be adjusted by either increasing the ICSTRM register value (decreases speed) or decreasing ICSTRM register value (increases speed). This is called the trimming process. After an ICSTRM register value is identified at the desired speed, the user must store this value in a flash location for future use. Freescale provides an ICSTRM value in flash location 0xFFAF, named NVTRIM. Provided that the NVTRIM keeps the same internal reference clock trimming value when leaving the Freescale production factory and the device has never been reprogrammed by a third party; copying this value to the ICSTRM register in your application allows the internal reference clock to operate typically at around 31.25 kHz. Refer to the internal clock source (ICS) characteristics in the *MC9S08SG32 Data Sheet* for details on the typical condition.

For the AEC Grade 1 MC9S08SG32 devices, the internal reference clock must be trimmed within the range of 31.25 kHz – 39.0625 kHz. For AEC grade 0 devices, the internal reference clock must be trimmed within the range of 31.25 kHz – 35.156 kHz. This ensures devices to operate below the maximum core speed when using with the 1024 multiplier (35.156 kHz × 1024 = 36 MHz). 36 MHz is the maximum core speed allowed for AEC grade 0 devices. Although you can assign ICSTRM from 0x00 to 0xFF, do not assign a random value to the ICSTRM register. A random ICSTRM value may trim the internal reference clock to run out of range. For example, on an AEC Grade 0 device, if the MCU is configured as FLL engaged internal clock mode (FEI mode), the internal reference clock is multiplied by a factor 1024 to produce a higher core clock speed. If your internal reference is randomly trimmed at 38 kHz, then the core speed is 38 kHz × 1024 = 38.912 MHz. This exceeds the maximum core speed for AEC 0 devices at 36 MHz. For more details on how to use ICS V2, please refer to the *MC9S08SG32 Series Data Sheet*.

NOTE

The NVTRIM value differs from part to part. If the value is erased, you must re-trim the value again for each part that was erased. As shown in Figure 1, the PEMICRO connection manager => Trim Control function can re-trim the parts, but it can be tedious over large quantities. Use the Freescale factory programming service to trim desired frequency for production volume and quality. Details can be found by searching factory programming at www.freescale.com.

Figure 1 shows the trim control function that can be opened by clicking the debug button  from CodeWarrior IDE 6.0 version

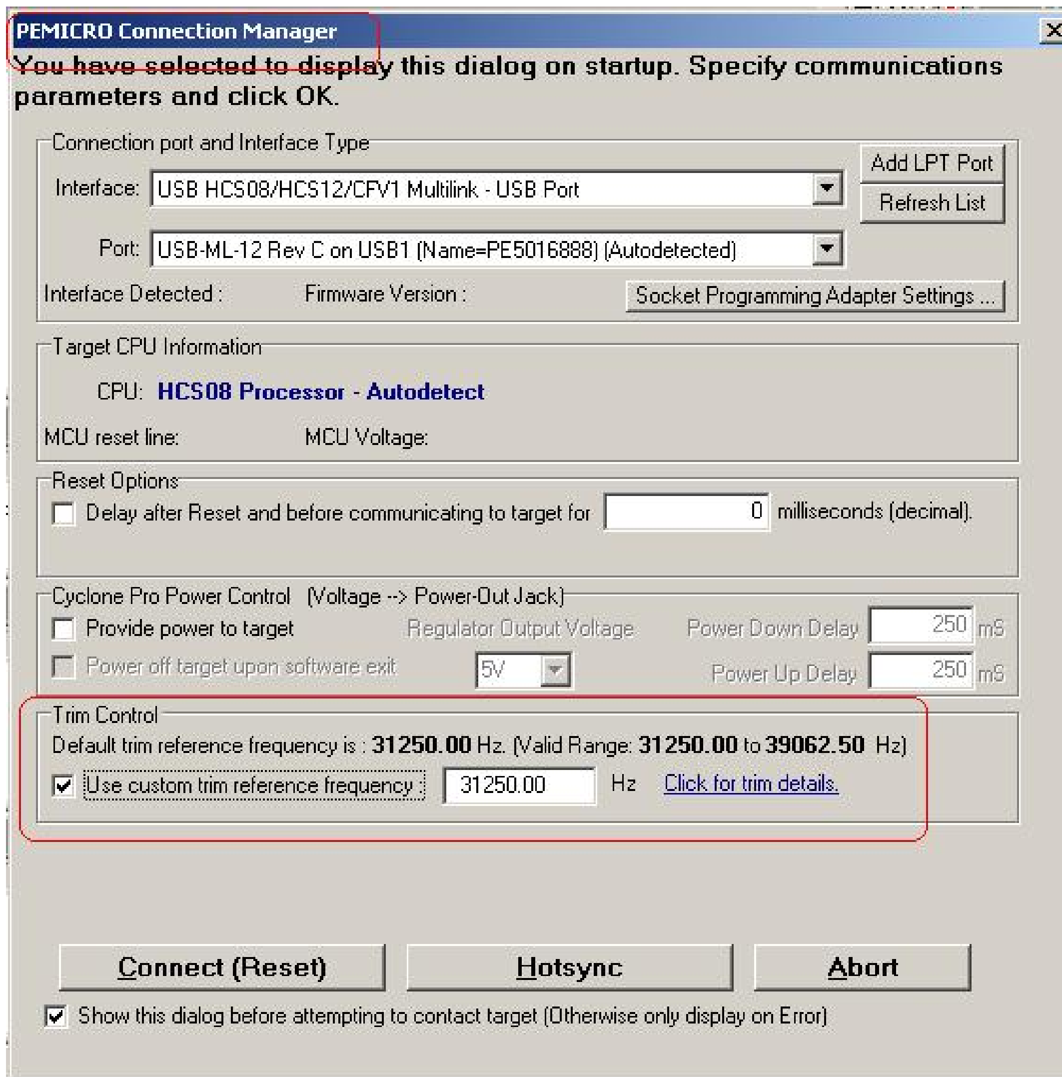


Figure 1. PEMICRO Connection Manager

5.2 Clock Accuracy Over Temperature Range

The internal reference clock is subject to deviation due to temperature. According to the data sheet (or see Table 4), the internal reference clock has a worst case scenario of ±3% deviation over operational temperature on the AEC Grade 0 parts, and ±1.5% deviation on the AEC Grade 1 parts. When the internal reference clock is used as a clock source for the bus clock, or MCU peripherals designers need to consider that all MCU peripheral time bases are also subject to the same deviation (for example, RTC, PWM, and so on.). The following is an example of using on-chip SCI peripheral with the internal reference clock.

Table 4. Referenced from the MC9S08SG32 Data Sheet — Internal Clock Source Characteristics

Num	C	Rating	Symbol	Min	Typical	Max	Unit	Standard	AEC Grade 0
9	D	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	0.5 –1.0	± 1.5	$\%f_{dco}$	◆	—
				—	0.5 –1.0	± 3		—	◆

5.3 Application Example Using SCI

On the HCS08SG32 AEC Grade 0 devices, 3% deviation is the worst case scenario for the internal clock source due to temperature. When the application uses this clock as a bus clock, the SCI baud rate is also subject to this deviation. The desired SCI baud rate can also be subject to a fixed deviation due to the baud rate register configuration. The following sections show the SCI baud rate is impacted, what can be done to reduce baud rate deviation, and the test that can be performed to ensure the SG32 SCI baud rate is compatible with the peer devices.

5.3.1 Baud Rate Deviation due to Baud Rate Register Configuration

The serial communications interface module in the MC9S08SG32 uses the following formula to determine its baud rate.

$$SCIbaudrate = (BUSCLK)/(16 \times BR) \qquad \textbf{Eqn. 5}$$

Where:

BR = The bits available in the SCI baud rate registers (SCIBDH, SCIBDL) selecting a value from 1 to 8191.

BUSCLK = bus clock. In this section, it is assumed that the bus clock derives the internal reference clock source.

In this example, the bus clock (BUSCLK) is 16 MHz and the target baud rate is 115200 bps. The BR is calculated using the following formula derived from Equation 5.

BR = BUSCLK/(16×SCI baud rate)

BR = 16 MHz / (16x115200) = 8.68

The BR is calculated to be 8.68. However, the BR value does not represent decimal points. It is tempting to round up this value to 9. However, this immediately introduces a deviation from our desired baud rate. Where the baud rate becomes:

SCI baud rate = 16 MHz/(16×9) = 111111.1 bps

Then the deviation of the baud rate is as following:

SCI baud rate deviation = [(115200 –111111.1) / 115200] × 100 = –3.55%

At –3.55% SCI baud rate deviation, SCI communication may remain tolerable by some peer devices. However, after adding the deviation due to temperture (–3%), a larger deviation is – 6.55%. This larger deviation is more likely to fail SCI communication.

5.3.2 Reducing Baud Rate Deviation via Clock Trimming

Although the internal clock deviation (±3% worse case) is not avoidable over a high temperature range, it is possible to reduce the deviation caused by the baud rate register configuration. This is done by trimming the internal reference clock speed. See example below:

BUSCLK = BR × (16 × SCI baud rate)

= 9 × (16 × 115200)

= 16,588,800 Hz

Internal Reference Clock = Core clock /1024

= (BUSCLK × 2) /1024

= (16,588,800 × 2) /1024

= 32400 Hz

From the example above, by trimming the MCU to the calculated internal reference clock speed, the baud rate deviation introduced by BR configuration error can be reduced, leaving only the ±3% deviation due to temperature.

5.3.3 Testing SCI Baud Rate Deviation with Peer SCI Devices

There is no fixed standard baud rate tolerance for SCI communication. Some devices may tolerate larger deviated baud rate transmissions while others may not. Also, it is difficult to predict whether a specific MC9S08SG32 part will result in the worst case 3% deviation over temperature.

One of the ways to emulate the SCI baud rate deviation over temperature is to trim the internal reference clock speed at –3% and at +3% of the desired baud speed.

Then, test both the –3% and +3% boundary cases to verify that the peer devices continue to communicate correctly with the MC9S08SG32 AEC grade 0 part.

Make sure to also account for the deviation that can potentially be caused by peer devices.

Example:

> Consider the worst case scenario where an MC9S08SG32 part can be a –3% deviation and the other part 1%, this is a total of |1%| + |–3%| = 4% deviation. Trim the MC9S08SG32 part to ±4% away from its desired frequency and test to verify that all the expected SCI characters are properly communicated between the devices.

6 Conclusion

The MC9S08SG32 high temperature devices are qualified to meet AEC Grade 0 requirements to operate up to 150 °C ambient temperature not exceeding T_{Jmax}. MCU characteristics that are susceptible to high temperatures must be taken into account during design and test.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: AN3835
Rev. 0
6/2009

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals”, must be validated for each customer application by customer’s technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics as their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see http://www.freescale.com or contact your Freescale sales representative.

For information on Freescale’s Environmental Products program, go to http://www.freescale.com/epp.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2009. All rights reserved.

freescale™ semiconductor