AN3274
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eXtreme Switch Protection Guidelines

1 Purpose

This document provides protection guidelines for the discrete components required to fulfill the eXtreme Switch devices' intended function.

2 Scope

This document is written generically for several different eXtreme Switch devices such as:

- single output switch, MC33982B,
- dual output switch, MC33984B,
- quad output switch, MC33580BA, and MC33874B.

The goal is to propose safe configurations of the eXtreme Switch devices in case of application faults and protect all circuitry with minimum external components. It serves only as a guideline to assist in the development of user specific solutions.

Development effort will be required by the end users to optimize the board design and Printed Circuit Board (PCB) layout.

Contents

3 Product environment

3.1 Overview about eXtreme Switch devices

The eXtreme Switch devices are self-protected, configurable silicon switches that can replace electromechanical relays, fuses and discrete circuits in power management applications. These are "Smart-Power" range products, designed for automotive and industrial applications. Each output can control separately resistive, as well as inductive and capacitive loads.

The eXtreme Switch products are high-side switches (N-channel MOSFET) with ultra low on-resistance (i.e. 2m Ohms), packaged in a Power QFN (PQFN) surface mount power package.

The switches integrate:

- overload protection,
- over-current detection,
- short-circuit protection,
- over-temperature protection,
- high voltage survivability,
- under-voltage and over-voltage shutdown with hysteresis.

Also, the devices provide:

- configuration and diagnostic feedback via a serial protocol interface (SPI),
- proportional load current sense,
- configurable slew rate,
- electrostatic discharge protection (ESD),
- active negative voltage clamp for fast de-energizing of inductive loads,
- loss of ground protection,
- open load diagnostic,
- reverse battery protection.

These devices also have a very low quiescent current in sleep mode.

3.2 Typical safe application schematic

This cost effective solution allows control and a fault diagnostic, which are not available with relays. No fuse is required; minimal PCB space is needed.

Figure 1, page 3 shows a typical safe application diagram for the MC33982B device. For MC33984B, the dual silicon switch device, the only circuit modification required in an additional dedicated additional input (IN1) corresponding to the second output (HS1).

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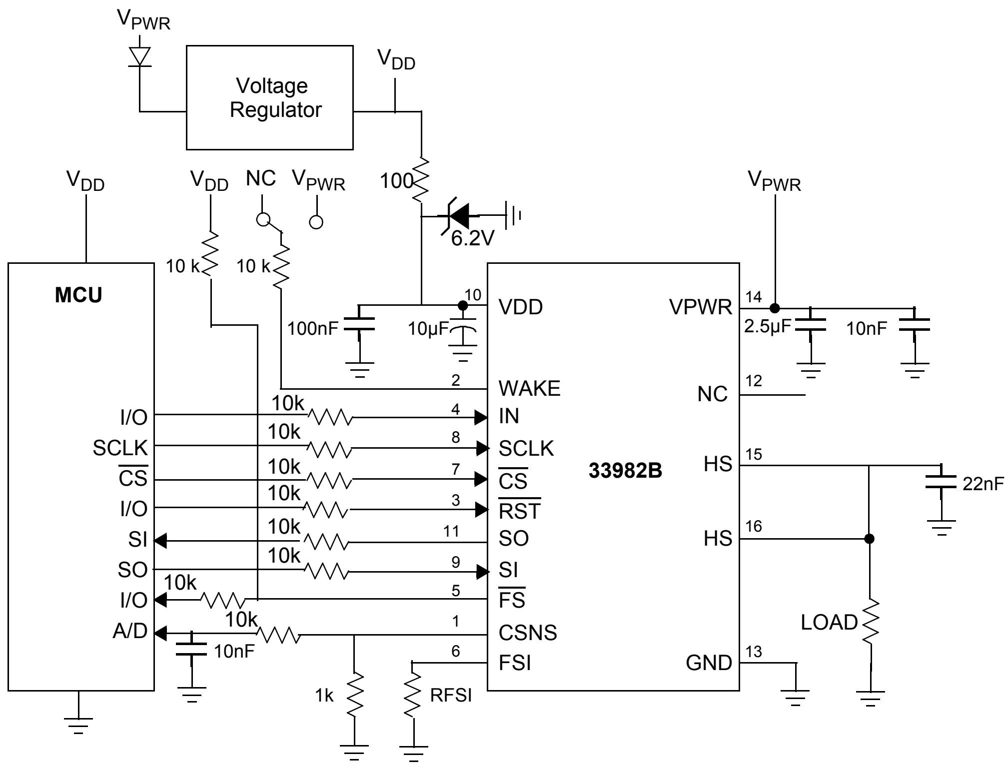


Figure 1. Typical safe application diagram

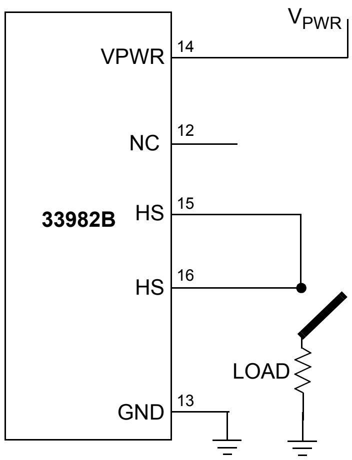
This application note describes solutions to protect not only the eXtreme Switch device, but also its supply and the load during applicative issues such as supply disconnections.

4 Fault conditions on the Ouput(s)

The eXtreme Switch devices are fully protected in case of fault conditions on the output(s), such as following:

- load disconnected,
- output shorted to ground,
- output shorted to the battery.

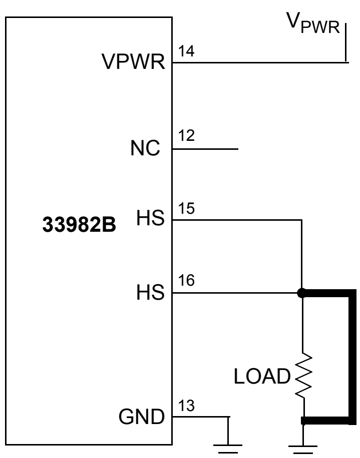
4.1 Load disconnect



The eXtreme Switch devices integrate open load detection circuitry on the output(s). If the load is disconnected, the output open load fault is detected and reported as a fault condition when the output is disabled (OFF). The fault is reported to $\overline{FS}$ output pin and latched into the SPI status register. The OL fault bit will be set in the status register. If the open load fault is removed, the status register will be cleared after an SPI read of the status register.

It is recommended that the open load detection circuitry be disabled (OL_dis bit sets to logic [1]) in case of permanent open load condition.

4.2 Output shorted to the ground

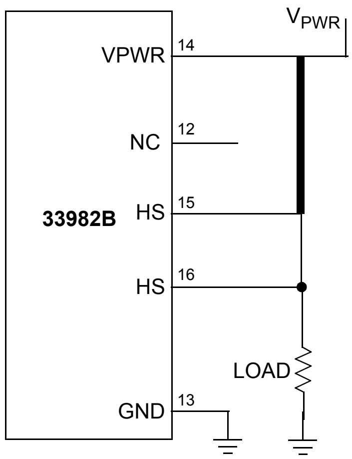


Latched over-current circuitry protects the system (wire harness, board layout traces ...) in case of resistive or hard short-circuit conditions with OCLO or OCHI current detections respectively. The corresponding over-current fault (OCLO or OCHI) is detected in the ON state, reported to $\overline{FS}$ output pin and latched into the SPI status register. The OCHI or OCLO fault bit will be set in the status register. If the over-current fault is removed, the status register will be cleared after an SPI read of the status register.

For the high ambient temperature, the over-temperature shutdown circuitry dedicated for each output can protect the device in case of an overload condition. This protection incorporates a thermal hysteresis. If an over-temperature is detected, an OT fault will be reported in real time to the $\overline{FS}$ output pin and latched into the SPI status register until a read operation. The over-temperature detection is also available in the OFF output state.

The microcontroller (MCU) manages faults during cases of permanent overload or short-circuit conditions by limiting the duration and number of activation cycles. Freescale recommends using the FS output signal as an MCU interruption to immediately catch the fault occurrence. This strategy avoids periodic SPI fault register polling (depending on the SPI traffic). In those situations the MCU needs to drive the device, avoiding a permanent fault report under nominal operation. For example, if one output is consistently open in the application, the openload detection circuitry must be disabled.

4.3 Output shorted to the battery



As mentioned previously, open load detection circuitry reports a fault in case the output(s) voltage is above a defined voltage threshold (3.0V typ.). This circuitry can help to detect a short-circuit from the output(s) to the battery in the OFF state.

Moreover, the current recopy feature should report a current lower than nominal current value in case the short-circuit impedance is similar to the $R_{DS(ON)}$ value of the high-side silicon switch.

It is recommended that the device be switched in sleep mode (WAKE and $\overline{RST}$ set to logic [0]) in case a of permanent output shorted to the battery condition.

5 Loss of supply voltages and ground

5.1 Reverse battery

A reverse battery condition consists of inverting the ground and the battery supply voltage. The eXtreme Switch devices survive the application of reverse voltage as low as -15V for 2 minutes. The output is turned ON in reverse battery conditions to limit power dissipation within the device.

Note: the electrical design that incorporates the eXtreme Switch device must ensure that VDD current path is opened during a reverse battery condition. For that, a diode should be included in series with the V_{DD} voltage regulator.

5.2 Loss of V_{PWR}

If the V_{PWR} supply is disconnected, the SPI operations (register configurations, register reading, daisy chain) are maintained until $\overline{RST}$ is set to logic [1]. During a loss of VPWR, the SPI pull-up and pull-down current sources are not operational. No current is conducted from V_{DD} to V_{PWR}.

No issue exists for resistive or capacitive loads, but additional protection circuitry is required for the device to support a battery disconnect for an inductive load connected to HS terminal(s). In fact, the current path from the inductor flows between HS and GND pins. The demagnetization is fast, but the internal HS/GND ESD circuitry can not withstand high current nor dissipate much energy. Thus, it is essential to add external components to create a path for the de-energizing current during this condition. The inductive effect can be provided by the vehicle wiring length, which could be several meters. Assuming a 10 meters loop and about 1µH/meter, the inductance is about 10µH. At high current (assume 10A), the energy is $\frac{1}{2} L I^2 = 0.5mJ$.

Figure 2 shows three possible battery disconnect protections.

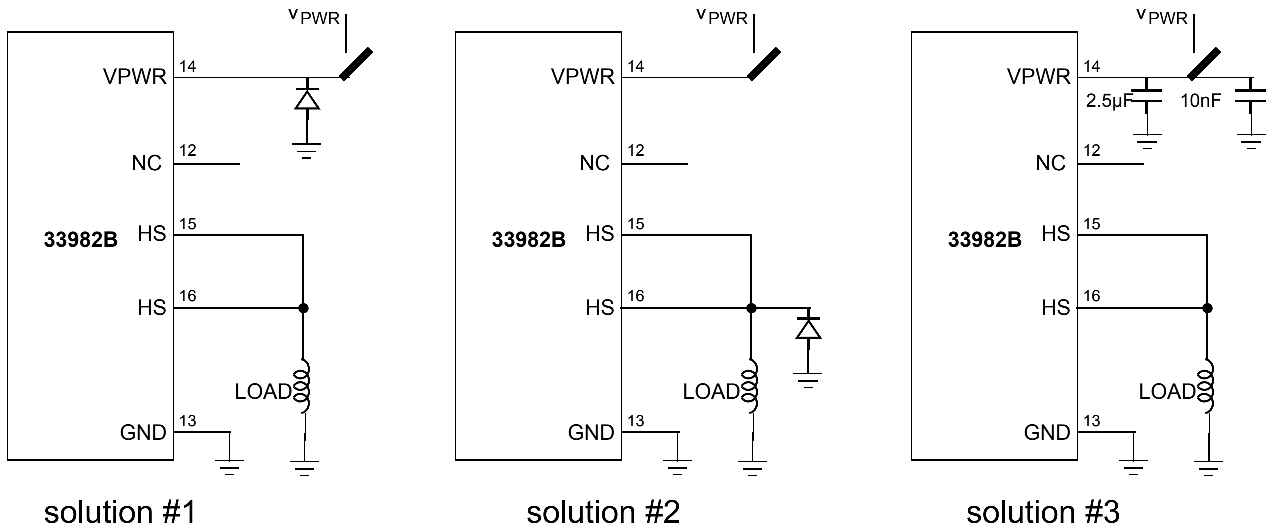


Figure 2. Battery disconnect protections

In the first solution, a diode can be added between the VPWR and GND pins. The inductive demagnetization will be done through the high-side silicon switch, with the output voltage clamped to -16V typ. Note that there is no reverse battery protection without an additional zener diode placed in series with the clamping diode.

In the second solution, a diode is added in parallel with the load. This implementation does not tolerate a reverse battery condition. In fact, the diode will be polarized in direct if the reverse battery condition occurs.

In the third solution, a non-polarized capacitor can be added between the VPWR and GND terminals. If the capacitance value is large enough, the inductive energy is quickly drained through the power MOSFET. If we allow a V_{PWR} (Vbattery) capacitor to deplete to zero and then recharge to an opposite polarity (starting from 13V and ending in -15V), the energy supplied and then stored is ½ C ($V1^2 + V2^2$). This leads to a Ceramic capacitance of 2.5uF to provide the energy of 0.5mJ.

This protection circuitry is recommended for all applications sustaining the reverse battery condition.

Moreover, it is recommended to turn-off the output(s) before a normal to sleep mode transition.

5.3 Loss of V_{DD}

If the V_{DD} supply is disconnected, the SPI register content is reset and the device is configured in the default mode corresponding to a low logic state on each SPI bit, as shown **Table 1**. No current is conducted from V_{PWR} to V_{DD}.

Table 1. Default SPI-configurable parameters

Configurable parameter	Default value
over-current protections	enable
severe over-current level	OCHI0
resistive over-current level	OCLO0
over-current blanking time	t_{OCLO0}
over-temperature protection	enable
over-voltage detection	enable
under-voltage detection	enable
open-load detection	enable
load current sense	enable with CSR0 ratio for MC33982 disable for MC33984
slew-rate	slow slope
watchdog time-out	t_{WDTO0}

During a loss of VDD, the WD bit can not be toggled properly due to a SPI communication failure from the microcontroller. The eXtreme Switch device will revert to Fail-safe mode, as long as the device is awake. In this mode, the ouput(s) state depends on the FSI input configuration as it relates to the external FSI resistor, called RFSI.

If the FSI terminal is shorted to ground, the output is controllable with the corresponding IN terminal. Otherwise, the state of the output is predefined (OFF or ON) after the watchdog time-out.

5.4 Loss of ground

Two ground disconnect configurations can be examined, as described in **Figure 3**.

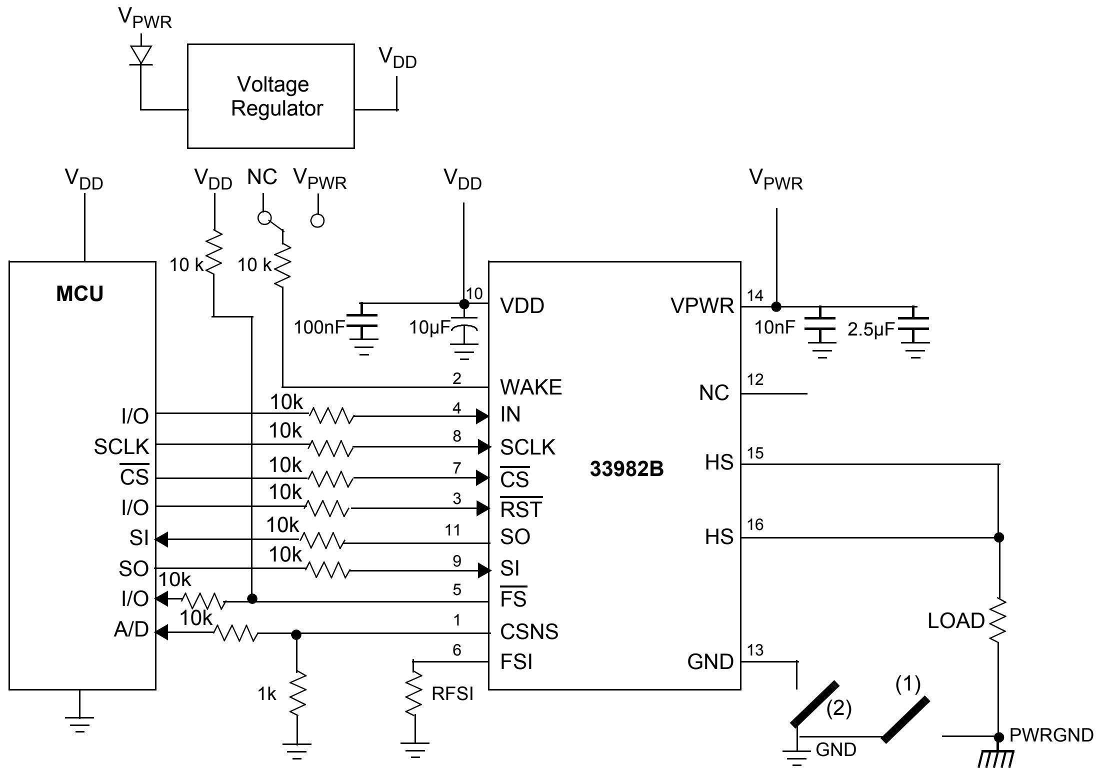


Figure 3. Module (1) or eXtreme Switch (2) ground disconnect conditions

In the event that the ground of the module (GND) is disconnected from load ground (PWRGND), the device protects itself and safely turns off the output. The ground disconnect protection is active regardless of the state of the output at the time of disconnection. Ground disconnection overrides the Fail-safe operation. In case of inductive load, the freewheeling diode in parallel with the load must discharge any energy stored in the load or wiring inductance because the output negative clamp circuitry behavior can not be guaranteed during loss of module ground.

For the eXtreme Switch ground disconnect, the current flowing through the digital I/Os (WAKE, IN, SCLK, $\overline{\text{CS}}$, $\overline{\text{RST}}$, SO, SI, $\overline{\text{FS}}$ and CSNS) should be limited by a 10k resistor (+/-5% tolerance) in series, as shown in **Figure 4**. In this case, the ground terminal (#13) voltage increases and the device protects itself and safely turns off the output.

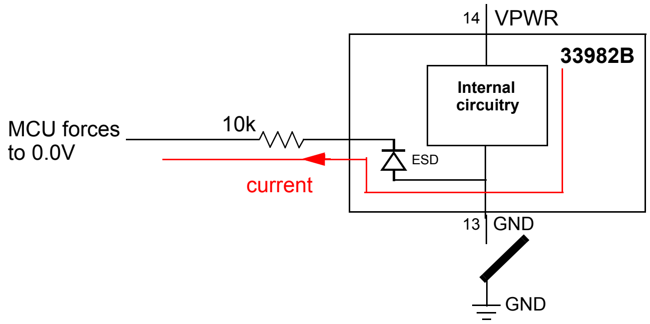


Figure 4. Current flows in negative I/O clamping mode

5.5 Ground shift within the module

The FSI resistor should be placed closely to the eXtreme Switch device, and its ground connection should be connected directly to the IC's ground, to avoid a voltage differential between ground points.

The CSNS resistor should be placed closely to the MCU, and its ground connection should be connected directly to the MCU's ground.

6 Filtering

6.1 V_{PWR} bypass capacitor

The purpose of the V_{PWR} bypassing capacitor on the eXtreme Switch is fourfold.

First, it helps to suppress voltage transients that the vehicle impresses on the battery line. The transients on the battery line may contain a large amount of energy, so this capacitor is capable of attenuating only brief transients. Other methods are needed to protect the module from higher energy transients, such as load dump.

Second, it provides a voltage source for the highest frequency components of the inrush current or short circuit current. This is necessary to maintain the V_{PWR} voltage during these conditions.

Third, it suppresses HF noise at the V_{PWR} pin that is generated by the eXtreme Switch itself. The noise can originate in the charge pump circuitry or it may occur when an output is switched ON or OFF.

Fourth, during a loss of Vpwr condition, the V_{PWR} capacitor supplies load current to de-energize load inductance, as explained in the “loss of V_{PWR}” section.

It is recommended that a 2.5µF and a 10nF (50V) ceramic are placed on the V_{PWR} terminal.

6.2 V_{DD} bypass capacitor

Bypassing capacitors are selected based on the desired high frequency response and the holdup time during brown outs and transients. They also attenuate noise generated by the eXtreme Switch device from SPI transmissions, for example. Consequently, the V_{DD} capacitor need only have a good high frequency response. 10µF and 100nF (50V) components should be placed as decoupling capacitors.

6.3 Output bypass capacitor

It is recommended that a 22nF capacitor to be placed on each output (HS) to dissipate energy in any high frequency, high voltage transients, especially ESD transient pulses. A 50V ceramic capacitor has sufficient voltage capability.

A 470nF (50V) ceramic capacitor should be placed on each output terminal for suppression of ground noise coming from the vehicle.

6.4 Current recopy low-pass filter

A1k resistor should be used on the CSNS output pin with +/-1% tolerance to monitor the RMS load current for potential steady state overload faults. This resistor should be placed close to the MCU and its ground connection should be connected directly to the MCU’s ground. The voltage on CSNS output pin should not exceed the V_{DD} voltage of the A/D.

A low pass-filter, as an RC filter, can be placed across the CSNS resistor to suppress HF noise. The time constant of this filter (tau = RC) of the filter should be about 100µs. C_{FILTER} should be placed close to the MCU's A/D input. Placing the filter capacitor C_{FILTER} close to the MCU rather than close to the eXtreme Switch’s CSNS pin is the preferred practice. Also, the ground connection for C_{FILTER} should be at the same potential as the ground of the A/D reference. The filter resistor R_{FILTER} is also used to limit the A/D's input pin current.

It is recommended to use 10k resistors with +/-5% tolerance and 10nF (20V) ceramic capacitors as low-pass filter components.

7 Beyond maximum ratings

7.1 -40V on V_{PWR}

The V_{PWR} minimum rating is -18V and the part will begin to break down at roughly -20V.

The eXtreme Switch device is protected in cases of positive or negative transients on the V_{PWR} line, as defined per the ISO/DIS 7637-2 international standard. The device is fully compliant with the Table A.3a of the specification, except for the Pulse 1 where the test level must be limited to -35V. Additional components should be used to survive any more negative transient disturbance, as described in **Figure 5**.

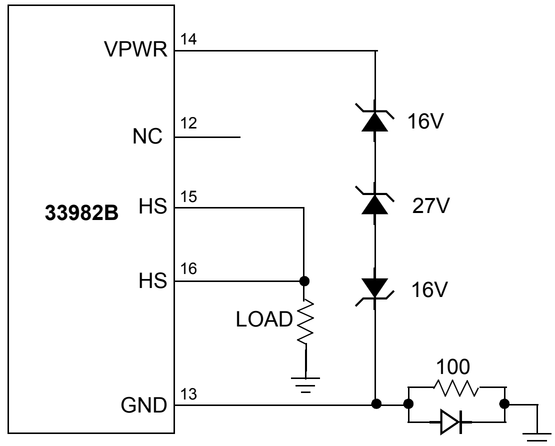


Figure 5. Battery external clamp circuitry

7.2 V_{DD} shorted to the battery

The V_{DD} maximum rating is 7.0V, and the device will begin to break down at roughly 8.5V. A 6.2V zener diode coupled to a 100 resistor with +/-5% tolerance can prevent the device damage in case V_{DD} is shorted to V_{PWR}, as illustrated in **Figure 6**.

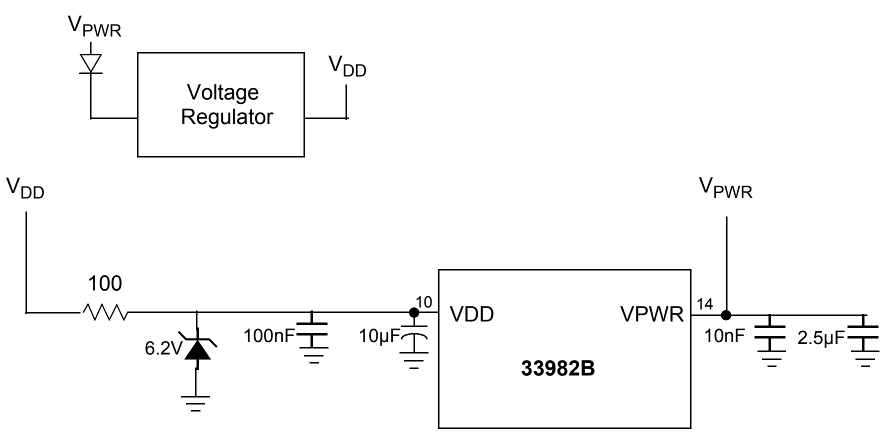


Figure 6. VDD clamp circuitry

7.3 Digital I/Os shorted to the battery

A 10k resistor with +/-5% tolerance needs to be added in series on all digital terminals in order to limit the current in clamping mode during a short to battery fault. The same method is used to limit Battery current in to the WAKE input terminal.

The tau result of the SPI signals (SCLK, $\overline{CS}$, SO and SI) is 40 to 100ns with a 4 to 10pF input capacitance. It can not be acceptable for high SPI frequency transmissions. Placing a 1nF capacitor (20V) in parallel with the 10k resistor provides cleaner rising and falling edges.

The $\overline{FS}$ pin is an open drain configured output and is active LOW. This terminal requires a pull-up resistor to the V_{DD} supply. The typical application schematic recommends a 10k resistor with a +/-5% tolerance.

8 Design Review

Please contact the local Field Application Engineer (email: support@freescale.com) in order to book a design review session before new eXtreme Switch design introduction.

9 References

Freescale Semiconductor Application Note, AN2467, Power Quad Flat No-lead (PQFN) Package.

ISO International Standard, ISO/DIS 7637-2, Road vehicles - electrical disturbance by conduction and coupling.

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