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Application Note

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S12XD and S12XE Family Compatibility

by: Martyn Gallop, MCD Applications, East Kilbride
Steve McAslan, MCD Applications, East Kilbride

1 Introduction

The high performance MC9S12X MCU architecture, which includes the MC9S12XD family, now adds the MC9S12XE family supporting additional system integrity features and enhanced peripheral modules. This application note describes the differences between the MC9S12XD (S12XD) and MC9S12XE (S12XE) families and steps that can help to maximize reuse of software and hardware between the two.

The following list summarizes the differences between the S12XE family and the S12XD family.

- 50 MHz operation
- Memory protection unit
- Emulated EEPROM
- Flash with error correction coding
- Enhanced memory management controller
- Faster conversions and 12-bit mode for analog to digital converters

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- Internal PLL featuring frequency modulation option
- Enhanced XGATE peripheral co-processor
- Enhanced CPU
- Extended voltage regulator with extended autonomous periodic interrupt counter
- Enhanced debug module capabilities
- SPI now features 16-bit mode
- Standard timer module available and enhanced ECT output compare configuration

2 System Integrity Improvements through Memory Management

Increasingly, embedded systems contain software provided by several suppliers. For example, an application developer may select a driver for a particular peripheral from one supplier while a different vendor provides the real-time kernel. The developer then integrates these together with the specific application code. The correct interaction of peripheral drivers, RTOS kernels, and applications is an important and complex challenge for the system integrator. It is important that the various software modules do not incorrectly access or modify another's memory space or hardware.

The S12XD family provides a limited memory protection scheme that applies only to the on-chip RAM and is primarily intended to manage the interaction of the CPU and XGATE.

The S12XE family includes significant new capabilities to help manage the on-chip and external memory through changes to the CPU and the provision of a new memory protection unit (MPU) module. These new features provide an advanced scheme that allows incorrect software behavior to be detected and averted.

2.1 The CPU, System States, and the MPU

The S12XE protection uses a bus master approach where eight memory access descriptors are available for controlling the access permission for any defined bus master. These descriptors are located in a new MPU and define the range of memory addresses and the type of access allowed. If a software task accesses resources outside those permitted, the system generates a non-maskable interrupt.

The MPU supports up to four bus masters. There are two bus masters allocated for the CPU, one for the XGATE and one for another module such as the FlexRay controller.

The CPU can operate as two different bus masters depending on if the active system state is supervisor state (CPU_SS) or user state (CPU_US). In user state, the CPU is unable to execute certain instructions. This prevents a user state task from changing the system state to supervisor state. The supervisor state allows the MPU to restrict access for code executed by kernels or drivers that require access to system resources.

To support CPU system states, the S12XE CPU includes a new bit, the U-bit, in the condition code register (CCR bit 15) and a new non-maskable software system call (SYS) interrupt instruction and associated vector. The SYS instruction is similar to the existing SWI instruction. In fact, it was added to prevent system calls from having to use the SWI, which is often used by debug tools.

The BDM (debug) interface on the S12XE operates independently of the system states and the MPU. This allows a debugger to access any location within the memory map without causing an error or non-maskable interrupt.

2.2 User State

User state is entered from supervisor state by application code setting the U-bit. User state prevents the CPU from performing several operations so that software cannot:

- Set or clear system interrupt enables (X, I)
- Set or clear stop enable (S)
- Clear the User State bit (U)
- Change interrupt priority (IPL[0:2])

These limitations affect the instructions that direct modify bits in the CCR (CLI, SEI, ANDCC and ORCC) and instructions that modify the entire register (RTI, PULC, EXG, TFR). If the CPU executes one of the above instructions, it modifies the unprotected bits in the CCR and leaves the protected bits unchanged.

The CPU is also unable to execute the WAI and STOP instructions. Instead, it performs the equivalent of a NOP instruction.

2.3 Supervisor State

The MPU restricts memory accesses of the CPU in supervisor state only when the supervisor state enable (SVSEN) bit in the MPUSEL register of the MPU is set.

The CPU returns to supervisor state from user state on entry to an interrupt service routine (ISR): the CCR with the U-bit set is stacked and the U-bit is then cleared. The only way for the MCU to remain in supervisor mode at the end of an ISR is for the service routine code to clear the U-bit in the stacked CCR word.

2.4 MPU Descriptors

The MPU features eight identical descriptors that configure protection for the system.

These descriptors describe the memory access permitted by each master. A bus master cannot access memory for which it does not have a descriptor.

The descriptors contain a start and end address for the memory range. The addresses are 20-bits wide and allow access to any address in global memory with an 8-byte resolution. Each descriptor is active if it is assigned to at least one master. Descriptors can be assigned to more than one master.

The descriptors also define the memory access allowed for the given range. They can independently prevent writes to the memory and code execution from the memory. This allows you to define four different behaviors for memory as shown in Table 1.

Table 1. MPU Access Combinations

Write	Execute	Behavior
No	No	Read-only data memory
No	Yes	Read-only code memory
Yes	No	Variable RAM
Yes	Yes	Code execution from RAM

2.5 Memory Protection Compatibility

Following reset, MPU descriptor 0 is configured, by default, for full access rights for all bus masters for the full global memory range. This effectively enables access to all of the memory map for all bus masters. This is compatible with the default condition on the S12 family and on the S12XD family, if protection is not enabled.

If transferring an existing S12XD design that uses the RAM protection scheme, the software must initialize two descriptors to provide the XGATE only and CPU only protection. The existing code that initializes the S12XD MMC protection registers must be removed because these registers no longer exist and their memory locations are reused by the MPU.

NOTE

The NVM blocks also include protection schemes to prevent accidental modification.

3 NVM – Flash and EEPROM

The S12XE family features an improved flash memory module with error correction coding (ECC) and hardware emulated EEPROM. On the S12XD family, the flash and EEPROM modules are separate. On the S12XE, these are combined into a single module known as the FTM.

The FTM contains P-flash blocks intended for program storage and D-flash blocks intended primarily for NVM data storage and for emulated EEPROM storage. The FTM has a completely new memory controller (state machine) to perform flash and EEPROM operations on the P-flash and D-flash blocks.

P-flash and D-flash are implemented with ECC that can resolve single bit errors and detect double bit errors. The ECC implementation on the P-flash requires that programming be done on an 8-byte basis (a P-flash phrase) on aligned by eight address boundaries. The ECC implementation on the D-flash allows programming of individual words.

FTM commands are performed by writing command information, data and global addresses to a Common Command Object (CCOB, a set of six banked word registers) and then clearing the CCIF flag in the FSTAT command register. Error and status flags are also available in the FSTAT register similar to the S12XD family. The flash programming algorithm no longer writes the data value into the flash array.

There is no command queue as on the S12XD, and a flash command must complete before the CCOB can be written with the next command.

All flash commands requiring an address use the global address format. For example, the FTM's view of the P-flash on a 1-Mbyte flash device (9S12EXP100) is a linear address map from 0x70_0000 to 0x7F_FFFF. Linear format S-records starting on an 8-byte boundary and with a line length that is a multiple of eight are expected to be the most efficient match. The 8-byte phrase length maps effectively to the 8-byte data length used by CAN bootloaders.

3.1 Emulated EEPROM (EEEPROM)

The S12XE family features a hardware scheme that implements EEPROM with improved performance and convenience for the user. The emulated EEPROM consists of a buffer RAM corresponding to the maximum size of the EEPROM, a data flash (D-flash), and a state machine to manage the EEPROM contents.

For an emulated EEPROM of 4 Kbytes, there is a RAM of 4 Kbytes. Software can write into the RAM and the value changes immediately. The software can read the RAM at any time and the value returned is the last value written into the memory location. Each time the software writes into the RAM, the memory controller begins a process of copying from the RAM into the D-flash. This process occurs in parallel with the normal CPU operation and requires no further intervention from user software.

The memory controller manages the contents of the D-flash so there is always erased D-flash available to program for new values in the buffer RAM. At reset, the memory controller copies the contents of D-flash into the buffer RAM.

At any time user software can determine, by examining the MGBUSY bit and the ETAG register, if the memory controller has completed its programming operations.

3.2 Emulated EEPROM Format Options

The memory controller allows you to format the size of the emulated EEPROM. If the application requires less than the maximum emulated EEPROM, it is possible to allocate less buffer RAM to this function. The portion of the buffer RAM not used for emulated EEPROM is available as normal RAM. The spare D-flash is then available for direct NVM operation or to extend the number of write-erase cycles on the emulated EEPROM.

You must format the emulated EEPROM once for the lifetime of the application. This operation would typically be performed during initial programming of the MCU.

3.3 NVM Compatibility

Reads of flash and emulated EEPROM behave in exactly the same way as the S12XD (and S12) family. Reading data directly from flash may generate ECC error warnings but these are disabled by default.

The algorithm for programming flash and EEPROM is completely different to the approach for the S12XD and S12 families. For flash programming, the algorithm is different in approach and P-flash also requires aligned 8-byte source data. The most significant change is in the size of data required for each programming operation because the algorithm, although different, uses the same flow and source information as the S12 and S12XD families.

User software on the S12XE now programs flash only through the FTM registers and not by writing into the flash array. This change allows XGATE threads to program P-flash and D-flash, which is not possible on the S12XD family. Although the XGATE cannot read the contents of most of the flash, this enhancement offers new possibilities for in-circuit programming. For example, XGATE could write status information to flash while the CPU is busy with other tasks. This could prove useful if XGATE is performing a system integrity check that discovers a defect in the CPU behavior. The defect information could be written by XGATE to flash for later diagnostic analysis. Take care when using this approach because the NVM is unavailable while the programming operation is under way. The CPU is unable to read from or execute from the NVM that the XGATE is modifying.

For emulated EEPROM programming, there is no programming algorithm needed. If the user software requires to monitor the status of the programming operation, then the code must be updated to account for the new module. However, you must format the emulated EEPROM before the function is available.

The S12XE does not have the flash data compress command present on the S12XD. This functionality is largely replaced by the ECC feature on the S12XE.

4 Memory Management Control (MMC)

The memory management control module on the S12XE retains most of the functionality seen on the S12XD family, adds some additional features, and consolidates the module into a more compact memory range.

The module on the S12XE now features additional chip select controls for use in external bus modes. The PPAGE register is relocated to a new address to allow a more compact use of memory. This greatly simplifies the configuration of descriptors in the MPU. Also, the S12XE MMC no longer contains a RAM protection scheme, as this functionality is now contained in the MPU. There are new options for configuring the memory visible at certain locations in the memory map.

On the S12XD:

- The non-volatile EEPROM protection byte is located in the EEPROM array at 0x130FFD (global).
- The non-volatile flash protection byte is located in the flash array at 0x7FFF0D(global).

On the S12XE:

- The non-volatile EEE(PROM) protection byte is located in the P-flash array at 0x7F0FFD (global).
- The non-volatile P-flash protection byte is located in the P-flash array at 0x7FFF0C (global).

4.1 Chip Select Support

On the S12XE, there are four new chip select control bits in MMCCTL0. See Section 12.8, “External Bus Interface (EBI)” for more information. The new control bits provide the ability to configure different wait states for the different chip selects.

The active range for the chip selects is the same as for the S12XD family, with the exception of CS2:

- On S12XD the active range of chip select CS2 is 0x10_0000-0x1F_0000 (global).
- On S12XE the active range of chip select CS2 is 0x14_0000-0x1F_0000 (global).

Also, chip selects on S12XD are enabled in special test mode, while chip selects on S12XE are disabled in special test mode.

4.2 PPAGE Register

On S12XD, the PPAGE register is located at 0x0030. Address 0x0015 is reserved.

On S12XE, the PPAGE register is located at 0x0015, to simplify access to all of the memory paging registers when the register block is protected by an MPU descriptor. Address 0x0030 is reserved. Other than the change in location, the PPAGE register functions in exactly the same way as on S12XD. Most existing software tools support selection of a different register address for PPAGE.

4.3 RAM Protection

The RAM protection configuration registers in the S12XD MMC (RAMWPC, RAMXGU, RAMSHL and RAMSHU) do not exist on the S12XE. The functionality of these S12XD registers is now part of the MPU functionality. See Section 11.2, “MPU Access Violation Vector”.

4.4 Alternative RAM Mapping Configuration

On the S12XE, there is a new option for alternative mapping of the on-chip RAM into the 4000-7FFF fixed memory space as an alternative to page 0xFD of the program flash. This is a write-once configuration that allows the RAM to be configured as a 24-Kbytes flat memory map + 4-Kbytes paged (28 Kbytes flat if the application does not page the RAM).

This is enabled by a new RAMHM bit (MMCCTL1, bit 3) and the existing ROMHM bit (MMCCTL1, bit 1)

When both of these bits are set,

- Accesses to 0x4000–0x7FFF are mapped to 0x0F_C000-0x0F_FFFF in the global memory space
- Accesses to 0x2000-3FFF are mapped to 0x0F_A000-0x0F_BFFF in the global memory space.

The default value of the RPAGE register remains 0xFD and should be written to 0xF9 in the application to configure a 28-Kbyte flat memory map.

Page 0xFD of the flash can be accessed via PPAGE and GPAGE instructions. By default, RAMHM is reserved and the RAM mapping on the S12XE is fully compatible with S12XD.

4.5 FTM Module Mapping

The S12XE MMC provides four new bits to control the visibility of some FTM memory regions. Each of these new bits in MMCTL1 defaults to 0. This means the appropriate resource is not visible in the map after reset.

The bits are mostly useful for Freescale but they are accessible to customers. These bits can be left in their their default state during typical application operation.

4.6 MMC Compatibility

Software written for the MMC on the S12XD is highly compatible with S12XE. The memory location of the PPAGE register is changed between the families; user software and development must take account of this difference. The RAM protection registers are no longer part of the module, and this function (if used) must be reassigned to the MPU.

The external bus chip select configuration is different; user software must change this to match the new register layout. The MMCTL1 register contains additional memory visibility control bits; users must take care that their existing software does not make unintended writes to these bits.

5 Analog to Digital Converter (ATD)

The analog part of the ATD conversion module is a completely new design for S12XE that supports higher resolution (12-bit), faster sampling rates, and lower power conversion. It includes additional features, such as an internal RC oscillator for conversion in full-stop mode, analog comparison against a user programmed limit (with support for wakeup from low power modes on a match), and sample and hold capacitor discharge (for improved system reliability).

In general, the configuration and conversion sequencing are unchanged from the existing S12XD ATD. This means that the general software flow is common between the two ATD modules. However, some registers and specific control bits have been modified to take account of the improved feature set and to remove redundant functionality.

This section describes the ATD configuration and functionality changes in detail.

5.1 New Features

The ATD includes an internal oscillator that allows conversions to be carried out even when the MCU is in STOP. Software can enable this new functionality by setting a bit in ATDCTL2.

The ATD also has a comparison feature that can cause an interrupt if a conversion is less than or equal to or is higher than a defined value. The comparison function is available in any mode (it is not restricted to STOP mode) and frees the CPU from constantly having to check ATD results against a particular threshold. The comparison interrupt is independent of the ATD result register, allowing the CPU and XGATE to distinguish between regular conversion completion and a comparison event.

Importantly, these features can be combined and allow an MCU to monitor an external analog voltage and wake from stop if it drops below, matches or exceeds a known value. The comparison is available on all channels and compares the ATD result against the value written into the result register.

5.2 ATD Pin Assignments

The S12XEP100 has two 16-channel ATD modules. The pin assignment (the mapping of analog input pins to ATD module channels) is optimized to support the two 16-channel modules.

The S12XDP512 has an 8-channel (ATD0) and a 16-channel (ATD1). The pin assignment is based on a mix of 8-channel and 16-channel modules.

Although the pin locations of the analog inputs are the same for the S12XEP100 and the S12XDP512, in the 144-pin and 112-pin variants a number of the pins are assigned to different ATD modules/channels on the two devices. This can require changes to any existing S12 and S12XD software driver code depending on the package and the channels being used.

Table 2. ATD Channel to Pin Mapping

Family	144-Pin	112-Pin	80-Pin
S12XE	ATD0[15:0] = AN[15:00] ATD1[7:0] = AN[23:16]	ATD0[15:0] = AN[15:00]	ATD0[7:0] = AN[07:00]
S12XD	ATD0[7:0] = AN[07:00] ATD1[15:0] = AN[23:08]	ATD0[7:0] = AN[07:00] ATD1[7:0] = AN[15:08]	ATD0[7:0] = AN[07:00]

Although the 80-pin variants have the same pin assignments, ATD0 on the S12XE is actually a 16-channel module. For optimal compatibility when using this as an 8-channel ATD, set all the WRAP[2:0] bits in ATDCTL0. This causes the input selector to wrap to channel 0 if it increments past channel seven in a multiple channel conversion. The same recommendation is valid when using ATD1 in the 144-pin package.

5.3 ATD Register Detail

The ATDCTL1 register includes three new control bits:

- Bit 4 is now SMP_DIS. This is the discharge before sampling bit that, when set, causes the internal sample capacitor to be discharged each time before sampling the channel. This can help to detect an open circuit instead of measuring the previous sampled channel.
- Bits [6:5] are two new bits named SRES[1:0]. These select 8-bit, 10-bit, or 12-bit conversion resolution.

The ATDCTL2 register contains three changes:

- Bit 7 (ADPU) has been removed. The ATD module is enabled by default and is static, consuming only leakage current when not converting. There is no longer a requirement for a 20µs setup delay.
- Bit 5 (AWAI) has been removed. If the application requires that the ATD needs to halt in wait mode, any on-going conversions must be halted explicitly by the application software in the wait entry code (considering the faster conversion timing and reduced power consumption this is likely to be a requirement for a continuous conversion sequence only.)
- Bit 5 is replaced by a new internal clock (enabled) in stop mode bit (ICLKSTP) that controls if the ATD converter continues activity in stop modes (including full system stop).
- Bit 0 (ACIF) is removed. This was a copy of the SCF flag. Any software reading the ACIF bit must be modified to read the SCF flag.
- Bit 0 is replaced by a new ATD compare interrupt enable flag (ACMPIE) that allows the STD to cause an interrupt if a compare condition occurs.

The ATDCTL4 register contains a single bit change:

- Bit 7 (SRES8) has been removed. ATD resolution is now configured by the new SRES[1:0] bits in ATDCTL1.
- Bit 7 is replaced by an additional sample length configuration bit SMP2 (adjacent to existing SMP1 and SMP0). Sample time encoding is not compatible and user software must configure the ATD sample times so that it is compatible with the application characteristics. See Section 5.5, “Additional Comments on the ATD”.

The ATDCTL5 register contains two changes:

- Bit 6 (DSGN) has been removed. Applications requiring signed offset data should manipulate the results data in software.
- Bit 6 is replaced by the SC bit from ATDTEST1 bit 0. Conversion of the external channels or internal references are now initiated by the conversion start access to ATDCTL5.
- Bit 7 (DJM) has been moved to ATDCTL3 bit 7. The data justification mode affects the format of the conversion results written by the converter to the results register and the justification of the comparison values data written to the results registers by the CPU or XGATE. On S12XE, this bit is reserved.

The ATDTEST0 and ATDTEST1 registers are replaced by a new 16-bit ATD compare enable register (ATDCMPE). The register defaults to ATD compare disabled. As long as it is not written, it is compatible. The only compatibility issue is that any writes to the SC bit to enable conversion of the internal references should now be part of a modified write to ATDCTL5.

The PORTAD0 and PORTAD1 registers are replaced by a new 16-bit ATD compare higher than register (ATDCMPHT). Application code that accesses the PORTAD registers must be modified to access the alternative PTxADx registers in the Port Integration Module (PIM).

The ATDDRn registers are read-only on the S12 and S12XD. On the S12XE, they are also used as comparison registers, and so the software can write to these registers. Writing to ATDDRn registers causes the last ATD conversion result to be lost.

5.4 Conversion Complete Flag Clearing

The default flag clearing mechanism (with AFFC = 0) for the conversion complete flags (CCFx) in ATDSTAT2 has been updated. On the S12XD, the conversion complete flags are cleared by a single read of the ATDSTAT2 register followed by a read of the appropriate conversion result register(s). On the S12XE, the conversion complete flags must be cleared by writing a one to the set CCFx bit (standard flag clearing method on S12 and S12XD).

The fast flag clear mode (i.e. with AFFC = 1) remains compatible.

5.5 Additional Comments on the ATD

The 12-bit resolution is intended to improve the relative sampling resolution. The absolute error of the converter is expected to be the same as for the current 10-bit ATD.

The S12XE analog design does not include a buffer amplifier (as on the S12XD). Therefore, conversion accuracy is going to be more sensitive to the correct sample time than on S12XD. To assist with setting a suitable sample time, the encoding of the sample timing (SMP bits) is enhanced.

5.6 ATD Compatibility

The significant new functionality on the ATD requires a number of changes to the configuration registers on the module. The general flow of the software is unchanged so software changes are expected to be relatively minor. Although, the changes must be implemented correctly.

6 Internal Phase Locked Loop (IPLL)

In general, the functionality of the clocks and reset generator (CRG) is similar from S12XD to S12XE. The key difference is that the S12XE internal PLL (IPLL) does not require an external filter circuit on the PCB (there is no XFC pin). The S12XE also has a new register configuration and provides support for frequency modulation, which can assist with EMC emissions in some applications.

User software must configure the CRG to generate a VCO frequency within a specified range. There are new controls to configure the IPLL filter and VCO gain for specific input reference frequency ranges and the VCO output frequency ranges respectively. The VCO output clock is then divided down to provide the required IPLL clock output. The IPLL frequency modulation can be enabled and selected for three different modulation amplitudes.

6.1 CRG Register Detail

The SYNR register includes two new control bits:

- Bits [7:6] are two new bits named VCOFRQ[1:0]. These bits control the gain of the VCO and user software must select the correct configuration based on the target frequency.

The REFDV register includes two new control bits:

- Bits [7:6] are two new bits named REFFRQ[1:0]. These bits configure the internal filter and user software must select the correct configuration based on the reference clock frequency.

There is no longer any distinction between acquisition and tracking mode. This leads to changes to two bits in the PLLCTL register:

- Bit 4 ACQ is removed.
- Bit 5 AUTO is removed.
- Bits [5:4] are two new bits named FM[1:0]. These bits enable and select frequency modulation on PLLCLK for reduced noise emission.

This also causes changes in the CRGFLG register:

- Bit 2 TRACK status bit is removed.
- Bit 2 becomes the illegal address reset flag (ILAF) from the CRGINT register, so all CRG flags are now located in the CRGFLG register.
- Bit 6 in the CRGINT register is now reserved.

The CLKSEL register contains a new bit:

- Bit 5 is a new bit named XCLKS. This read-only bit reflects the selected (latched) oscillator configuration.

The CRG also features a new register POSTDIV that divides the VCO output clock (VCOCLK) down to the desired system clock frequency. This replaces the CTFLG register on the S12XD family that was used only for factory test.

7 XGATE

The XGATE on the S12XE features the ability to respond to high priority interrupts. In addition, the XGATE error interrupt is now a non-maskable interrupt to the CPU.

7.1 Interrupt Capability

The XGATE module of the S12XD family does not support pre-emption. An active XGATE thread on the S12XD is not interruptible. The S12XE XGATE module supports a single level of pre-emption. Any active lower priority thread (level 1, 2 or 3) is interrupted by any new higher priority interrupt (level 4, 5, 6, or 7) that is routed to the XGATE.

The interrupt causes XGATE to swap to an alternative set of registers. This new context is the same programmers' model, featuring general purpose registers R0 to R7, the PC, and the CCR.

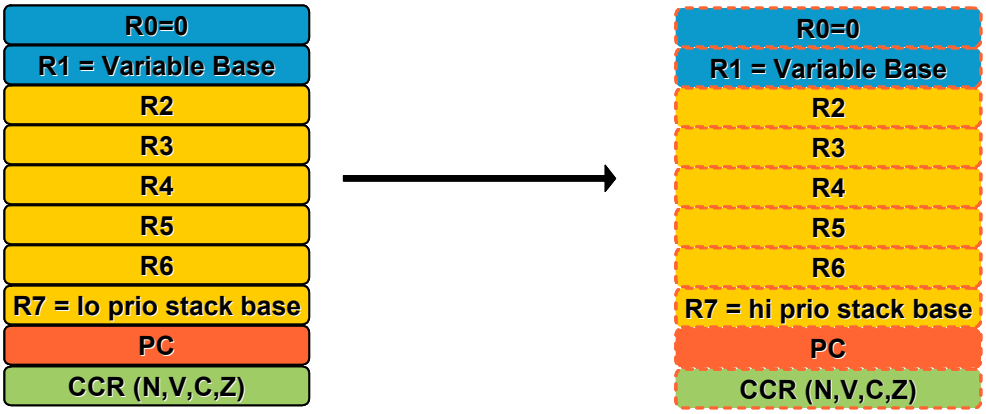

Figure 1. XGATE Context Switch

When programming the XGATE in C, the tool chain creates a software stack that it uses for function calls. The stack base address is configured by each software thread. Because each thread on the S12XD starts with the XGATE in its default state, a single stack location can be used for all threads.

If a high priority thread does interrupt a low priority one, the context for the low priority thread (including any register used as a stack pointer, typically R7 for existing tools) is swapped out. At the end of any high priority exceptions, the low priority context is restored and the thread continued.

To avoid a high priority thread corrupting the low priority thread's stack, the S12XE XGATE supports hardware initialization of register R7 at the beginning of each thread execution. This allows a different stack base address for high and low priority threads. These two stack pointer base addresses must be stored in two new initial stack pointer configuration registers (XGISP31 and XGISP47) during XGATE initialization. Additionally, the XGATE compiler should be configured not to re-initialize the stack pointer at the start of each thread.

To maintain compatibility with the XGATE memory map, the two stack pointer base registers are banked at the same location as the existing XGATE vector base address register (XGVBR @ module base + 0x0006), and the register banking is controlled by a new initial stack pointer select register (XGISPSEL @ module base + 0x0005).

The S12XE XGATE also has a new channel priority level register (XGCHPL @ module base + 0x0003) that indicates the interrupt level of the currently executing thread.

Legacy code and tools are compatible if only low priority or high priority interrupt levels are used or where it is guaranteed that a high priority thread does not interrupt a low priority thread.

7.2 Error interrupt

The XGATE error interrupt on S12XE is a non-maskable interrupt. This is different to the S12XD where the interrupt is a normal I-bit maskable interrupt. The sources of this interrupt are the same as on the S12XD, except that XGATE access violations detected by the MPU also use this vector. See Section 7.1, "Interrupt Capability" for more information.

8 CPU Enhancements

The four fuzzy instructions (MEM, REV, REVW, and WAV/WAVR) are deprecated and may be removed in future versions of the S12X CPU.

The CPU on the S12XE includes two enhancements from the CPU on the S12XD family: the user/supervisor state bit and the SYS opcode. These enhance the usability of the MPU in embedded systems and are discussed in detail in the MPU section.

9 Voltage Regulator

The on-chip voltage regulator (VREG) generates supply voltages for the NVM and oscillator/PLL modules and the core logic.

On the S12XD, the VREGEN pin allows the use of an external voltage regulator for the core power supply. In this case, the core supply pins are connected together on the application PCB.

On the S12XE, the VREGEN pin is not available, and the internal voltage regulator is always enabled. It is recommended that the core supply pins are not connected together on the PCB and that each pair of supply pins has a dedicated decoupling capacitor. S12XD designs using an external voltage regulator to supply the 2.5V core supplies must be modified appropriately.

V_{DD1}, V_{DD2}, and V_{DDPLL} are all nominally 2.5V on S12XD.

Table 3. S12XD V_{DD} Values

		Characteristic	Symbol	Min	Typ	Max	Unit
7	P	Low Voltage Interrupt Assert Level Deassert Level	 V_{LIVA} V_{LVID}	 4.1 4.25	 4.37 4.52	 4.66 4.77	 V V
8	P	Low Voltage Reset Assert Level	 V_{LVRA}	 2.25	 —	 —	 V
9	C	Power-on Reset Assert Level Deassert Level	 V_{PORA} V_{PORD}	 0.97 —	 — —	 — 2.05	 V V

On S12XE V_{DD} (= V_{DD1}) and V_{DDPLL} are nominally 1.8V, V_{DDF} (==V_{DD2}) is nominally 2.8V.

Table 4. S12XE V_{DD} Values

		Characteristic	Symbol	Min	Typ	Max	Unit
5	P	Low Voltage Interrupt Assert Level Deassert Level	 V_{LIVA} V_{LVID}	 4.06 4.19	 4.21 4.34	 4.36 4.49	 V V
6	P	V_{DD} Low Voltage Reset Assert Level	 V_{LVRA}	 1.62	 —	 —	 V
7	P	V_{DDF} Low Voltage Reset Assert Level	 V_{LVRFA}	 2.6	 —	 —	 V
8	P	V_{DDX} Low Voltage Reset Assert Level	 V_{LVRXA}	 3.13	 —	 —	 V

NOTE

On the S12XE, with the minimum LVR level for the input supply voltage equals 3.13V. The device is held in reset for any supply effectively below the lower supply input voltage (= 3.15V), preventing out-of-spec operation. This is the lowest voltage the device can operate at for any functionality.

On S12XE, the maximum allowable decoupling capacitance on V_{DD1} and V_{DD2} is 440nF.

9.1 Autonomous Periodic Interrupt (API)

The API counter has been extended from twelve bits to sixteen bits to extend the available timeout range. In addition, the API can drive directly an output pin at the end of each timeout period. The behavior of the output pin is selectable between a clock and a timeout pulse. The API is backwards compatible (the additional counter bits were unused on S12XD).

10 Pinout Changes

The S12XE pinout is mostly compatible with the S12XD, with all of the IO pins and the majority of supply connections remaining the same. Only four pins have different external connectivity.

10.1 Pins with Different Connectivity

1. S12XD supply V_{DDPLL} (PLL and oscillator supply) changes to S12XE supply V_{DDR} (Voltage regulator supply). On S12XE, connect to 5V/3V3 input supply and provide a decoupling capacitor between V_{DDR} and V_{SS3}.

Table 5. V_{DDPLL} Pin Changes

Package	144 QFP	112 QFP	80 QFP
Pin Number	55	43	31

2. 12XD signal XFC (PLL filter) changes to S12XE supply V_{SSR} (Voltage regulator ground).

Table 6. XFC Pin Changes

Package	144 QFP	112 QFP	80 QFP
Pin Number	56	44	32

3. S12XD signal TEST (Test mode control) changes to S12XE supply V_{DDPLL} (PLL and oscillator supply). On S12XE, provide a decoupling capacitor between V_{DDPLL} and V_{SSPLL}.

Table 7. TEST Pin Changes

Package	144 QFP	112 QFP	80 QFP
Pin Number	60	48	36

4. S12XD signal VREGEN (Internal voltage regulator enable) changes to S12XE signal TEST (Test mode control).

Table 8. V_{REGEN} Pin Changes

Package	144 QFP	112 QFP	80 QFP
Pin Number	127	97	67

10.2 Power Supply Pins with Different Internal Connectivity

1. S12XD supply V_{DD1} (core logic supply) changes to S12XE supply V_{DDF} (flash module supply). On S12XE, also provide a decoupling capacitor between V_{DDF} and V_{SS1}. Do not connect to other supply pins.

Table 9. V_{DD1} Pin Changes

Package	144 QFP	112 QFP	80 QFP
Pin Number	15	13	9

2. S12(X)D supply pair V_{DDR}/V_{SSR} (Voltage regulator supply/ground) changes to S12XE supply pair V_{DDX2}/V_{SSX2} (IO supply/ground). On S12XE, connect V_{DDX2} to 3V3 / 5V and provide a decoupling capacitor between V_{DDX2} and V_{SSX2}.

Table 10. VDDR and VSSR Pin Changes

Package	144 QFP	112 QFP	80 QFP
Pin Number	52/53	40/41	28/29

10.3 ATD Pins with Different Internal Connectivity

See Section 5.2, “ATD Pin Assignments” for detail.

11 Interrupts

The interrupt controller and behavior is compatible with S12XD, with the addition of new non-maskable interrupt support for the SYS instruction, memory protection violation, and XGATE software error vectors.

S12XEP100 interrupt vector table is otherwise backwards compatible with the S12XDP512.

11.1 SYS Instruction Vector

A new non-maskable SYS instruction vector is located at vector base + 0x12. This vector was reserved on S12XD.

- vector base +0x12 SYS – System Call

11.2 MPU Access Violation Vector

The I-bit maskable SRAM32K access violation vector at vector base + 0x60 on S12XD is superseded on S12XE by a non-maskable MPU access violation vector at vector base + 0x14. On S12XE, vector base + 0x60 is a reserved vector.

- vector base +0x14 CPU Access Error

11.3 XGATE Access Violation / Software Error Vector

The I-bit maskable XGATE software error vector at vector base + 0x62 on S12XD is superseded on S12XE by a non-maskable XGATE access violation vector at vector base + 0x16. On S12XE, vector base + 0x62 is a reserved vector.

- vector base +0x16 XGATE access / software error

11.4 New Peripheral Vectors (on 9S12XEP100)

The I-bit maskable reserved vector at vector base + 0xC2 on S12XD is superseded on S12XE by the SCI6 vector.

- vector base +0xC2 SCI6 XGATE Ch 0x42

On S12XE there are additional I-bit maskable vectors for new peripherals from vector base + 0x3C to vector base + 0x5E. These were reserved vectors on S12XD512.

- vector base +0x3C ATD1 compare XGATE Ch 0x1E
- vector base +0x3E ATD0 compare XGATE Ch 0x1F
- vector base +0x40 TIM pulse accumulator input edge XGATE Ch 0x20
- vector base +0x42 TIM pulse accumulator A overflow XGATE Ch 0x21
- vector base +0x44 TIM overflow XGATE Ch 0x22
- vector base +0x46 TIM channel 7 XGATE Ch 0x23
- vector base +0x48 TIM channel 6 XGATE Ch 0x24
- vector base +0x4A TIM channel 5 XGATE Ch 0x25
- vector base +0x4C TIM channel 4 XGATE Ch 0x26
- vector base +0x4E TIM channel 3 XGATE Ch 0x27
- vector base +0x50 TIM channel 2 XGATE Ch 0x28
- vector base +0x52 TIM channel 1 XGATE Ch 0x29
- vector base +0x54 TIM channel 0 XGATE Ch 0x2A
- vector base +0x56 SCI7 XGATE Ch 0x2B
- vector base +0x58 Periodic Interrupt Timer 7 XGATE Ch 0x2C
- vector base +0x5A Periodic Interrupt Timer 6 XGATE Ch 0x2D
- vector base +0x5C Periodic Interrupt Timer 5 XGATE Ch 0x2E
- vector base +0x5E Periodic Interrupt Timer 4 XGATE Ch 0x2F

12 Miscellaneous Modules

The following modules are backwards compatible with the S12XD modules, and also provide enhanced features.

12.1 General Purpose I/O

The S12XE family includes all of the I/O ports available on the S12XD and, depending on pinout, additional ports. The extra ports are:

- PJ3
- Port AD0 — one new register associated with pins connected to the upper eight ATD0 channels
- Port R — associated with the new standard timer module
- Port L — associated with new SCI modules
- Port F — associated with IIC, SCI and chip select outputs

Each of the latter three new ports has module routing registers to allow access to different peripheral configurations in the lower pin count packages.

The ECLK divider chain on PE4 has been extended from divide-by-1 to divide-by-4 on S12XD. It is now, on S12XE, divide-by-1 to divide-by-32, with a further divide-by-16 stage, and is fully backwards compatible with the S12XD family.

12.2 Enhanced Capture Timer (ECT)

The ECT timer on the S12XE is backwards compatible with the one on the S12XD with two exceptions. First, it has an additional output compare pin disconnect (OCPD) register that can support glitch-free initialization of the output state of any output compare channel. On the S12XD, the output compare configuration (OMx = 0, OLx = 0) is described as timer disconnected from output pin logic. This is a typical configuration where the capture compare interrupt is used only for internal interrupt timing. In this case control of the associated port pin is automatically switched to the PIM port control registers.

The second difference from the ECT on the S12XD family is that the output compare flags (CnF) are set under different conditions in the timer cycle. On the S12XD, the CnF flag is set when the main timer (TCNT) value matches the value in the output compare register (IOCn). The CnF flag is set if software writes the IOCn register to the current value of TCNT. On the S12XE, the CnF flag is only set if TCNT is incremented to the value in the IOCn register. Software must write the desired IOCn value before TCNT reaches that count.

On the S12XE, the output compare configuration (OMx = 0, OLx = 0) is more specifically described as no output compare action on the timer output signal. The internal interrupt behavior is the same as on the S12XD, but the OCPD register explicitly controls the connection of the OC channel logic or the IO port control logic to the port pin.

The reset state of the OCPD register is for the OC logic to be connected to the pin when a channel is configured for output compare. For compatibility with S12XD, the relevant OCPD bit must be set during configuration if GPIO functionality is required while using the OC channel as an internal interrupt timer.

12.3 Standard Timer (TIM)

The standard timer on the S12XE is backwards compatible with the one on the S12. It is updated to be a subset of the S12XE ECT module with the addition of the precision prescaler and output compare pin disconnect (OCPD) features.

12.4 IIC

The IIC module has two additional bits to support new general call address and 10-bit addressing features, which are controlled via a new control register IBCR2 located at module base +0x0005. This is a reserved register on S12XD.

The new features default to disabled and the default IIC is fully compatible with S12 and S12XD.

12.5 Periodic Interrupt Timer (PIT)

The programmable interrupt timer on the S12XE has eight timer channels. The PIT on the S12XD has only four. The additional four sets of load and count registers, located from module base +0x0018 to module base +0x0027, are reserved on S12XD.

All PIT channels are disabled at reset and are fully compatible with the four channels on the S12XD.

12.6 Serial Peripheral Interface (SPI)

The SPI on the S12XE additionally supports 16-bit data transfers as well as 8-bit transfers. This is controlled via a new transfer word (XFRW) in a control register (IBCR2 bit 5).

The S12XD 8-bit data register SPIDR is renamed SPIDRL and is used for the least significant eight data bits for 8-bit or 16-bit transfer modes.

In 16-bit transfer mode, the upper byte of the 16-bit data (SPIDRH) is located at module base +0x0004. This is a reserved register on S12XD.

This SPI new feature defaults to disabled and the default mode is fully compatible with S12XD

12.7 Oscillator

Physically, the oscillator configuration is similar on S12XD and S12XE. The oscillator component layout is compatible. However, the pinout change requires a small PCB change.

The oscillator supply (V_{DDPLL}) is 2.5V on S12XD and 1.8V on S12XE.

On S12XE, the minimum allowed crystal or resonator frequency is 4 MHz in amplitude controlled pierce mode and 2 MHz in full swing pierce mode.

As described in the CRG section, on the S12XE, there is a new bit that indicates the selected oscillator configuration.

12.8 External Bus Interface (EBI)

The external bus interface is generally the same from the S12XD to the S12XE. The chip selects have been enhanced.

On the S12XD, there is a global programmable access stretch count for all four chip selects, configurable in EBICTL0. Each chip select line can then be enabled via a single control bit in the MMCTL0 register (CSnE).

On the S12XE, two different access stretch counts can be configured in EBICTL0. Each of the four chip selects can then be programmed individually to use either one of the two counts or the external EWAITE signal, independently. Configuration of each chip select is via a pair of bits in MMCCTL0 register (CSnE1 and CSnE0).

12.9 Debug Module

The debug and BDM modules are compatible on S12XD and S12XE. The S12XE has additional functionality to the S12XD debug module. Refer to the user manual for full details.

12.10 Modules without Feature Enhancements

Most of the modules on the S12XE contain enhanced features, but remain backwards compatible with software written for the S12XD family. The following modules have no new features and are unchanged on the S12XD and S12XE:

- Background Debug Module (BDM)
- Serial Communications Interface (SCI)
- Pulse Width Modulation module (PWM)
- Freescale scalable CAN (msCAN)

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How to Reach Us:

Home Page:
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USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
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