Freescale Semiconductor
Application Note

Document Number: AN3089
Rev. 1, 11/2013

MPC8641D/MPC8641 Design Checklist

This application note describes the generally recommended connections for new designs based on the following Freescale processors:

- MPC8641D
- MPC8641
- MPC8640D
- MPC8640

The design checklist may also apply to future bus- or footprint-compatible processors. It can also serve as a useful guide to debugging a newly-designed system, by highlighting those areas of a design that merit special attention during initial system startup. For updates to this application note, refer to the website listed on the back cover of this document.

NOTE

References to MPC8641D also apply to MPC8641, MPC8640D, and MPC8640, unless otherwise specified.

Contents

1 Introduction

This section outlines recommendations to simplify the first phase of design. Before designing a system with a MPC8641D device, it is recommended that the designer be familiar with the available documentation, software, models, and tools.

2 Power

This application note lists recommended connection features, roughly divided into the following modules:

System	Interrupts, reset, JTAG, exception signals, serial ports, and test pins
Power	VDD (core) and I/O power pins
Memory	DDR1 and/or DDR2 controllers
Ethernet	10/100/1G-bit Ethernet interfaces
Local bus	Flash interface
SerDes	PCI-Express or serial RapidIO interfaces

Signals that are active-low asserted are noted with a overbar.

Table 1 shows the checklist for the system module in the MPC8641D.

Table 1. MPC8641D Design Checklist—System Module

Check	Signal	Notes
Reset		
	$\overline{\text{HRESET}}$	Must be asserted for 100 μs as noted in the *MPC8641 and MPC8641D Integrated Host Processor Hardware Specifications* (MPC8641DEC).
		Merge with any on-board $\overline{\text{HRESET}}$ using wire-OR function, such as LVT08 or FPGA.
		Ensure that JTAG tools are able to assert this input (via $\overline{\text{COP\_HRESET}}$) without also causing $\overline{\text{TRST}}$ to be asserted.
	$\overline{\text{HRESET\_REQ}}$	May be left open if unused.
		Should not be just shorted to $\overline{\text{HRESET}}$; use logic, which enables this only after OVDD is stable.
	$\overline{\text{SRESET0}}$	Pulled up to OVDD if not used.
		Merge with on-board $\overline{\text{SRESET}}$ using wire-OR function, such as LVT08 or FPGA.
		COP typically connects to $\overline{\text{SRESET0}}$ (as the main processor).
	$\overline{\text{SRESET1}}$	Pulled up to OVDD if not used.
		Merge with on-board $\overline{\text{SRESET}}$ using wire-OR function such as LVT08 or FPGA.
		Must be pulled up to OVDD for MPC8641D (non-dual-core).
	$\overline{\text{CHKSTP\_IN}}$	Pulled up to OVDD if not used, else driven from OVDD-referenced output.
		Usually connects to COP header pin #8.

Table 1. MPC8641D Design Checklist—System Module (continued)

Check	Signal	Notes
	$\overline{\text{CHKSTP\_OUT}}$	May be open if unused.
		Usually connects to COP header pin #15.
	$\overline{\text{MCP0}}$	Pulled up to OVDD if not used, else driven from OVDD-referenced output.
		Not always recoverable, so it should not be used as a general-purpose interrupt.
	$\overline{\text{MCP1}}$	Pulled up to OVDD if not used, else driven from OVDD-referenced output.
		Not always recoverable, so it should not be used as a general-purpose interrupt.
		Must be pulled up to OVDD for MPC8641 (non-dual-core).
	$\overline{\text{SMI0}}$	Pulled up to OVDD if not used, else driven from OVDD-referenced output.
		May be used as a recoverable interrupt.
		Typical usage: connect to a thermal monitor alarm, or to a power-down monitor.
	$\overline{\text{SMI1}}$	Pulled up to OVDD if not used, else driven from OVDD-referenced output.
		May be used as a recoverable interrupt.
		Must be pulled up to OVDD for MPC8641 (non-dual-core).
DMA		
	$\overline{\text{DMA\_DREQ[0:1]}}$	Pulled up to OVDD if not used, else driven from OVDD-referenced output.
	$\overline{\text{DMA\_DACK[0:1]}}$	May be open if unused.
	$\overline{\text{DMA\_DONE[0:1]}}$	May be open if unused.
Interrupt/IRQ		
	IRQ(0:7)	Pullup or pulldown to OVDD per application. May not float unconnected.
		Use pulldowns on MPC8641 V1.0 when PCIExpress legacy interrupt modes are used.
	IRQ8 / AUX_CLK_OUT	Pullup or pulldown to OVDD unless using as AUX_CLK_OUT (rare).
		Recommended: Connect to test point with adjacent grounded test point for ALT_CLK_OUT function.
	IRQ9 / $\overline{\text{DMA\_DREQ3}}$	Pullup or pulldown to OVDD whether IRQ or DMA. May not float unconnected.
		Defaults to IRQ function unless DMA is selected in the PMUXCR register.
	IRQ10 / $\overline{\text{DMA\_DACK3}}$	Pullup or pulldown to OVDD required for IRQ function. Pullup recommended for $\overline{\text{DMA\_DACK3}}$ to eliminate spurious interrupts.
		Defaults to IRQ function unless DMA is selected in the PMUXCR register.
	IRQ11 / $\overline{\text{DMA\_DDONE3}}$	Pullup or pulldown to OVDD required for IRQ function.
		Defaults to IRQ function unless DMA is selected in the PMUXCR register.
	IRQ_OUT	Open-drain output requires a pullup and may be wire-OR'ed with other devices.
		May float if unused.
JTAG		

Table 1. MPC8641D Design Checklist—System Module (continued)

Check	Signal	Notes
	COP Header	Connector pin numbering schemes may vary; a physical view from above is as follows: +----------+ COP_TDO ---->|(1) (2)| NC COP_TDI <----|(3) (4)|----> $\overline{\text{COP\_TRST}}$ OVDD_PULLUP <-->|(5) (6)|<--> COP_VDD_SENSE COP_TCK <----|(7) (8)|----> $\overline{\text{CHKSTP\_IN}}$ COP_TMS <----|(9) (10)| NC $\overline{\text{COP\_SRESET}}$ <----|(11) (12)| NC $\overline{\text{COP\_HRESET}}$ <----|(13) (14)| KEY, no pin $\overline{\text{CHKSTP\_OUT}}$ ---->|(15) (16)|<--> GND +----------+
	TMS	May be open if unused (has internal pullup).
		Usually connects to COP header pin #9.
		Try to limit trace lengths to <= 6 inches and avoid crosstalk.
	TCK	May be open if unused.
		Usually connects to COP header pin #7.
		Try to limit trace lengths to <= 6 inches and avoid crosstalk.
	TDI	May be open if unused (has internal pullup).
		Usually connects to COP header pin #3.
		Try to limit trace lengths to <= 6 inches and avoid crosstalk.
	TDO	May be open if unused.
		Usually connects to COP header pin #1.
		May connect to other OVDD/3.3-V JTAG inputs.
		Try to limit trace lengths to <= 6 inches and avoid crosstalk.
		This pin is not released to high impedance during $\overline{\text{HRESET}}$.
	$\overline{\text{COP\_TRST}}$	MUST be asserted before or during $\overline{\text{HRESET}}$ after OVDD is stable.
		This pin may not float unconnected despite internal pullup.
		Usually driven by LVT08 or equivalent, which merges $\overline{\text{COP\_TRST}}$ (from COP header pin #4) with general system $\overline{\text{HRESET}}$.
		Ensure that $\overline{\text{TRST}}$ is driven by the system reset but NOT by $\overline{\text{COP\_HRST}}$.
		Try to limit trace lengths to <= 6 inches and avoid crosstalk.
Serial		
	I2C[1:2]_SDA	Open-drain input/output requires a pullup.
		Only I2C1_SDA is used to access boot sequencer data; otherwise, either port may be used for any purpose.
		Unused ports may float, but inadvertent access to the I2C controller may cause software to stall, so a pullup is strongly encouraged.

Table 1. MPC8641D Design Checklist—System Module (continued)

Check	Signal	Notes
	I2C[1:2]_SCL	Open-drain input/output requires a pullup.
		Only I2C1_SCL is used to access boot sequencer data; otherwise, either port may be used for any purpose.
		Unused ports may float, but inadvertent access to the I2C controller may cause software to stall, so a pullup is strongly encouraged.
	UART[1:2]_SOUT	May remain disconnected if unused.
	UART[1:2]_SIN	Pull down to ground if not used.
	UART[1:2]_RTS	May remain disconnected if unused.
	UART[1:2]_CTS	Pull down to ground if not used.
Debug		
	$\overline{\text{LSSD\_MODE}}$	MUST have a strong pullup (100 Ω to 1 kΩ) to OVDD.
	TEST(0:3)	MUST have a strong pullup (100 Ω to 1 kΩ) to OVDD.
	TRIG_IN	Pullup to OVDD if not connected to a signal source.
		Connect to any event to measure with the performance monitor, or to trigger debugging.
	TRIG_OUT / READY	May be left disconnected if unused.
		If used, must not be asserted low or pulled down during reset (ABIST).
		CONFIG: TRIG_OUT MUST NOT be pulled down: recommend pullup if connected to logic, even logic analyzers.
	D1_MSRCID / LB_SRCID(0:4)	May be left disconnected if unused.
		Usually connected to logic analyzer connectors and configuration options.
		CONFIG: D1_MSRCID[0] is "cfg_mem_debug": optional pulldown to enable MEM debug.
		CONFIG: D1_MSRCID[1] is "cfg_ddr_debug": optional pulldown to enable DDR debug.
		CONFIG: D1_MSRCID[2] MUST NOT be pulled down.
	D1_MDVAL / LB_DVAL	May be left disconnected if unused.
		Usually connected only to logic analyzer connectors.
	D2_MSRCID(0:4)	May be left disconnected if unused.
		Usually connected to logic analyzer connectors.
	D2_MDVAL	May be left disconnected if unused.
		Usually connected to logic analyzer connectors.
	ASLEEP	May be left disconnected if unused.
	CLK_OUT	May be left disconnected if unused.
		Recommend: connect to test point with adjacent grounded test point.
		Note that CLK_OUT is affected by the Global Utilities CLKOUT register as well as the core HID1 register.

Table 1. MPC8641D Design Checklist—System Module (continued)

Check	Signal	Notes
	TEMP_ANODE / TEMP_CATHODE	May be left disconnected if unused.
		Recommend: Connect to a thermal diode measurement logic (ADT7461 or equivalent).
Clocks		
	SYSCLK	Connect to a LVTTL clock, <= 150ps jitter. Note: There are actually two SYSCLK receiver buffers on chip. The PLL receiver buffer is AC coupled and is sensitive to the ramp rate and voltages specified in Table 8 **SYSCLK AC Timing Specifications,** in the Data Sheet, i.e. it is important for the SYSCLK input to swing from 0.4 to 2.7 V at 1.2ns or less. Failure to do so could result in loss-of-lock or failure-to-lock of the PLL. The second SYSCLK input buffer is conventional LVCMOS receiver and drives the common-on-chip processor logic. This input buffer is less sensitive to ramp time and only requires the DC levels of Table 7, **SYSCLK DC Electrical Characteristics**, in the Data Sheet. However, since there is only one SYSCLK input pin, designers should plan for the more restrictive requirement of an input clock which swings between 0.4 and 2.7V at a fast ramp rate.
		Must be stable (not clocking, but high or low) until all power supplies are stable.
		Recommend: Disable/tri-state during PWRGD. Do not tri-state/disable with HRESET.
	RTC	Connect to a LVTTL clock.
		Pullup to OVDD or ground if not used.
Spares		
	Spare	Should have no connection at all. Some schematics may have wired a signal to this pin per early specs, which is incorrect but acceptable.
	Reserved (AD24, AG26)	MUST have a pullup to OVDD.
	No Connects (K24, K25, P28, P29, W26, W27, AD25, AD26)	MUST be left disconnected.

Table 2 shows the checklist for the power module in the MPC8641D.

Table 2. MPC8641D Design Checklist—Power Module

Check	Signal	Notes
VDD: Core Power		

Table 2. MPC8641D Design Checklist—Power Module (continued)

Check	Signal	Notes
	VDD_CORE(0:1)	Connect to a single, or to two independent, 0.95-to-1.1V power supplies (or whatever is appropriate given the hardware specification)
		Single supply: simpler layout, larger current components required, smaller physical size.
		Dual supply: easier dynamic power savings, lower current componentry, larger physical size.
		MPC8641 (non-dual-core): VDD_CORE1 may float or may be grounded, whichever is more convenient.
		Recommend: Support a VDD range of 0.95V-to-1.2V (this allows for compensation of unexpected droop and/or board I-R losses)
		Recommend: 1 oz. copper fills of large surface area on outer layer to connect VDD pins to supply.
		Recommend: 1 cap for each power pin/pad.
		Recommend: Use via-in-pad to place 0402-SMD-caps directly across VDD_COREx and GROUND (see AN3065 for details).
	AVDD_CORE(0:1)	Connect to VDD_CORE(0:1) through a 10 Ω, 1/10W resistor.
		Connect two 2.2uF non-polarized ceramic capacitors to AVDD_COREx side.
		AVDD_CORE1 must connect to ground for non-dual-core devices.
		For boards supporting both MPC8641 and MPC8641D, allow a 0-Ω resistor to be installed in place of one of the 2.2uF capacitors (with the other and the 10-Ω resistor being depopulated).
		Recommend: Route using 10-20 mil traces and keep relatively short (2 cm max).
	SENSE_VDD(0:1)	Single supply: Connect only SENSE_VDD0 to the power-supply sense inputs; leave SENSE_VDD1 floating.
		Dual supply: Connect either SENSE_VDD line to the power-supply sense inputs.
		If the supply does not support feedback, connect SENSE_VDD(0:1) to VDD_CORE(0:1) as extra power, or to test points (die monitoring).
	SENSE_VSS(0:1)	Single supply: Connect only SENSE_VSS0 to the power-supply sense inputs; leave SENSE_VSS1 floating.
		Dual supply: Connect either SENSE_VSS line to the power-supply sense inputs.
		If the supply does not support feedback, or if it supports only a single-ended sense, connect SENSE_VSS(0:1) to ground as extra ground, or to test points (die monitoring).
VDD_PLAT: Platform (Internal IP Blocks) Power		
	VDD_PLAT	Connect to a 1.05V-1.1V power supply
		Recommend: 1 cap for each power pin/pad.
		Recommend: Place 0402-SMD-caps directly across VDD_PLT and GROUND.
	AVDD_PLAT	Connect to VDD_PLAT through a 10 Ω, 1/10W resistor.
		Connect two 2.2uF non-polarized ceramic capacitors to AVDD_PLAT side.
OVDD: LocalBus Power		

Table 2. MPC8641D Design Checklist—Power Module (continued)

Check	Signal	Notes
	OVDD	Connect to OVDD power supply (3.3V).
		Recommend: 1 cap for each power pin/pad.
LVDD: TSEC(1:2) Power		
	LVDD	Connect to 2.5V (RGMII) or 3.3V (others).
		May be bridged with TVDD if needed.
		Optional: Insert a ferrite bead between LVDD and TVDD.
		Recommend: 1 cap for each power pin/pad.
TVDD: TSEC(3:4) Power		
	TVDD	Connect to 2.5V (RGMII) or 3.3V (others).
		May be bridged with LVDD if needed.
		Optional: Insert a ferrite bead between LVDD and TVDD.
		Recommend: 1 cap for each power pin/pad.
SVDD: SerDes Internal Power		
	SVDD	Connect to 1.05V-1.0V power supply.
		Recommend filter between SVDD and other supplies if sharing power supplies.
		Recommend: 1 cap for each power pin/pad.
		Recommend: Use area fills to connect SVDD pins to supply.
	AVDD_SRDS	Connect to SVDD via 1-Ω resistor.
		Add (1) 3nF/3.3nF capacitor and (1) 1.0uF non-polarized capacitors between AVDD_SRDS and ground.
		Recommend: Route using 10-20 mil traces and keep relatively short (2 cm max).
	AGND_SRDS	Connect to common ground.
XVDD: SerDes IO Power		
	XVDD	Connect to 1.05V-1.0V power supply.
		Recommend: filter between XVDD and other supplies if sharing power supplies.
		Recommend: Use area fills to connect XVDD pins to supply.
GVDD: Memory Power		
	D(0:1)_GVDD	Connect to +2.5V power (DDR1) or +1.8V (DDR2).
		If a DDR interface is not needed, the corresponding rail may be connected to ground.
		Recommend: Use area fills to connect GVDD pins to supply.
Ground		
	GND	Connect to a solid plane extending around the MPC8641D to the power supplies.

Table 2. MPC8641D Design Checklist—Power Module (continued)

Check	Signal	Notes
	SGND	Connect to a solid plane extending around the MPC8641D to the power supplies.
	XGND	Connect to a solid plane extending around the MPC8641D to the power supplies.

Table 3 shows the checklist for the DDR controller module in the MPC8641D.

Table 3. MPC8641D Design Checklist—DDR Controller Module

Check	Signal	Notes
DDR1/DDR2		
	Dx_MDQ[0:63]	Connect MDQ0 to DIMM DQ0 or discrete LSB, ... Connect MDQ63 to DIMM DQ63 or discrete MSB.
		Series memory terminations (10-22 ohms) recommended for large discrete memory arrays.
		Series memory terminations NOT recommended for DIMM arrays unless modelling proves it. DIMMs often include series resistors.
		DDR1 ONLY: Connect to 49.9 Ω 1% (or other value ±10%) pullup to VTT[1:2].
		Route data byte lanes length-matched with corresponding lane sets: • Set 0: Dx_MDQ(0:7) + Dx_MDQS(0) + $\overline{\text{Dx\_MDQS}}$(0) + Dx_MDM(0) • Set 1: Dx_MDQ(8:15) + Dx_MDQS(1) + $\overline{\text{Dx\_MDQS}}$(1) + Dx_MDM(1) • Set 2: Dx_MDQ(16:23) + Dx_MDQS(2) + $\overline{\text{Dx\_MDQS}}$(2) + Dx_MDM(2) • Set 3: Dx_MDQ(24:31) + Dx_MDQS(3) + $\overline{\text{Dx\_MDQS}}$(3) + Dx_MDM(3) • Set 4: Dx_MDQ(32:39) + Dx_MDQS(4) + $\overline{\text{Dx\_MDQS}}$(4) + Dx_MDM(4) • Set 5: Dx_MDQ(40:47) + Dx_MDQS(5) + $\overline{\text{Dx\_MDQS}}$(5) + Dx_MDM(5) • Set 6: Dx_MDQ(48:55) + Dx_MDQS(6) + $\overline{\text{Dx\_MDQS}}$(6) + Dx_MDM(6) • Set 7: Dx_MDQ(56:63) + Dx_MDQS(7) + $\overline{\text{Dx\_MDQS}}$(7) + Dx_MDM(7) • Set 8: Dx_MECC(56:63) + Dx_MDQS(8) + $\overline{\text{Dx\_MDQS}}$(8) + Dx_MDM(8)
	Dx_MECC[0:7]	Connect to pullups if not used.
		Series memory terminations (10-22 ohms) recommended for large discrete memory arrays.
		Series memory terminations NOT recommended for DIMM arrays unless modelling proves it. DIMMs often include series resistors.
		DDR1 ONLY: Connect to 49.9 Ω 1% (or other value ±10%) pullup to VTT[1:2].
		Route data byte lanes length-matched with corresponding lane sets:
	Dx_MDQS[0:8]	Route as differential pairs with matching $\overline{\text{Dx\_MDQS}}$[0:8] signal.
		Route differential pair length-matched with corresponding lane sets.
		DDR1 ONLY: Connect to 49.9 Ω 1% (or other value ±10%) pullup to VTT[1:2].
	$\overline{\text{Dx\_MDQS}}$[0:8]	Route as differential pairs with matching Dx_MDQS[0:8] signal.
		Route differential pair length-matched with corresponding lane sets.
		DDR1 ONLY: Connect to 49.9 Ω 1% (or other value ±10%) pullup to VTT[1:2].
	Dx_MDM[0:8]	Route length-matched with corresponding lane sets.
		DDR1 ONLY: Connect to 49.9 Ω 1% (or other value ±10%) pullup to VTT[1:2].

Table 3. MPC8641D Design Checklist—DDR Controller Module (continued)

Check	Signal	Notes
	Dx_MA[0:15]	Connect to MA signals on DIMM or on discrete DIMMs. MA0 = LSB, MA15 = MSB.
		Series resistors are not required.
		Connect to 49.9 Ω 1% (or other value ±10%) pullup to VTT[1:2].
		Recommend: add optional 22pF cap to trace if high-speed/high-load design (see Micron AN TN47-01).
	Dx_MBA[2:0]	Connect to MBA signals on DIMM or on discrete DIMMs.
		Series resistors are not required.
		Connect to 49.9 Ω 1% (or other value ±10%) pullup to VTT[1:2].
		Recommend: add optional 22pF cap to trace if high-speed/high-load design (see Micron AN TN47-01).
	$\overline{\text{Dx\_MRAS}}$	Connect to $\overline{\text{RAS}}$ signals on DIMM or on discrete DIMMs.
		Series resistors are not required.
		Connect to 49.9 Ω 1% (or other value ±10%) pullup to VTT[1:2].
		Recommend: add optional 22pF cap to trace if high-speed/high-load design (see Micron AN TN47-01).
	$\overline{\text{Dx\_MCAS}}$	Connect to $\overline{\text{RAS}}$ signals on DIMM or on discrete DIMMs.
		Series resistors are not required.
		Connect to 49.9 Ω 1% (or other value ±10%) pullup to VTT[1:2].
		Recommend: add optional 22pF cap to trace if high-speed/high-load design (see Micron AN TN47-01).
	$\overline{\text{Dx\_MWE}}$	Connect to $\overline{\text{WE}}$ signals on DIMM or on discrete DIMMs.
		Series resistors are not required.
		Connect to 49.9 Ω 1% (or other value ±10%) pullup to VTT[1:2].
		Recommend: add optional 22pF cap to trace if high-speed/high-load design (see Micron AN TN47-01).
	$\overline{\text{Dx\_MCS}}$[0:3]	Connect to $\overline{\text{CS}}$ signals on DIMM (1 or 2) or on discrete DIMMs.
		Each CS controls one rank or 64-bit wide array of memory.
		Series resistors are not required.
		Connect to 49.9 Ω 1% (or other value ±10%) pullup to VTT[1:2].
		Recommend: add optional 22pF cap to trace if high-speed/high-load design (see Micron AN TN47-01).

Table 3. MPC8641D Design Checklist—DDR Controller Module (continued)

Check	Signal	Notes
	Dx_CKE[0:3]	Connect to CKE signals on DIMM (1 or 2 each) or on discrete DIMMs.
		CKE use follows the use of the CS: each rank gets one CS and one ODT.
		Series resistors are not required.
		Connect to 49.9 Ω 1% (or other value ±10%) pullup to VTT[1:2].
		Recommend: add optional 22pF cap to trace if high-speed/high-load design (see Micron AN TN47-01).
	Dx_MODT[0:3]	Connect to ODT signals on DIMM (1 or 2 each) or on discrete DIMMs.
		ODT use follows the use of the CS: each rank gets one CS and one ODT.
	Dx_MDIC0	Connect to pulldown to GND: 18.2 Ω, 1%.
	Dx_MDIC1	Connect to pullup to GVDD1/GVDD2: 18.2 Ω, 1%.
	Dx_MVREF	Connect to regulated 0.9V reference voltage.
		Recommend: place 1-2 0.1 uF low-ESR capacitors near Dx_MVREF.
		Recommend: route Dx_MVREF with no crosstalk.
	Dx_MCK[0:5]	Route as a differential pair with $\overline{\text{Dx\_MCK}}$[0:5].
		Unused clock outputs should terminated to ground (100 ohms nominal) to minimize EMI.
		Recommend: add a 5pF cap across the DIMM clock pair.
	$\overline{\text{Dx\_MCK}}$[0:5]	Route as a differential pair with Dx_MCK[0:5].
		Unused clock outputs should terminated to ground (100 ohms nominal) to minimize EMI.
		Recommend: add a 5pF cap across the DIMM clock pair.

Table 4 shows the checklist for the eTSEC controller module in the MPC8641D.

Table 4. MPC8641D Design Checklist—eTSEC Controller Module

Check	Signal	Notes
Overview: MPC8641D signal name vs. typical (r)GMII PHY signal name		
	TSECn_COL	COL
	TSECn_CRS	CS
	TSECn_GTXCLK	XCLKO
	TSECn_RX_CLK	RCLK
	TSECn_RX_DV	RDV
	TSECn_RXD[7:4]	RD[7:4]
	TSECn_RXD[3:0]	RD[3:0]
	TSECn_RX_ER	RX_ER
	TSECn_TX_CLK	TX_CLK

Table 4. MPC8641D Design Checklist—eTSEC Controller Module (continued)

Check	Signal	Notes
	TSECn_TXD[7:4]	TD[7:4]
	TSECn_TXD[3:0]	TD[3:0]
	TSECn_TX_ER	TX_ERR
	TSECn_TX_EN	TDV
	Interface Width	17 or 25
TSEC1		
	TSEC1_TXD[0:7] / GPOUT[0:7]	TXD[4:7] may float unconnected for MII+RMII+RGMII modes.
		If TSEC1 not used, may be used as outputs (which also may float open if not used).
		Series terminations may be needed for some boards.
		CONFIG: TXD[0] is "cfg_alt_boot_vec".
		CONFIG: TXD[1] is "cfg_platform_freq.
		CONFIG: TXD[2:4] are "cfg_device_id[5:7]".
		CONFIG: TXD[5] is "cfg_tsec1_reduce".
		CONFIG: TXD[6:7] are "cfg_tsec1_prtcl[0:1]".
	TSEC1_TX_EN	TXEN for all modes except RGMII, where it is TXCTL
		Optional: Series terminations may be needed for some boards.
	TSEC1_TX_ER	TXER may float if not used (RGMII mode).
	TSEC1_TX_CLK	TXCLK may float if not used (RGMII mode).
	TSEC1_GTX_CLK	Serves as TXCLK for most GMII/RGMII PHYs.
		Series terminations may be needed for some boards.
		RGMII requires +2ns delay on TXCLK relative to TXD/TXCTL, but most PHYs have s/w config options to eliminate that.
	TSEC1_CRS	Connect to ground for RMII / GMII / RGMII.
	TSEC1_COL	Connect to ground for RMII / GMII / RGMII.
	TSEC1_RXD[0:7] / GPIN[0:7]	If TSEC1 not used, may be used as inputs. If TSEC/GPIN not used, connect to pulldowns (or do not allow to float).
		RXD[4:7] are received data, except for MII+RMII+RGMII modes, where they should connect to ground (pulldown or direct).
		Series terminations are usually within the PHY
	TSEC1_RX_DV	RXDV for all modes except RGMII, where it is RXCTL
	TSEC1_RX_ER	RXER for all modes except RMII/RGMII, where it should connect to ground (pulldown or direct).
	TSEC1_RX_CLK	RXCLK for all modes except RMII, where it should connect to ground (pulldown or direct).
TSEC2		

Table 4. MPC8641D Design Checklist—eTSEC Controller Module (continued)

Check	Signal	Notes
	TSEC2_TXD[0:7] / GPOUT[0:7]	TXD[4:7] may float unconnected for MII+RMII+RGMII modes.
		If TSEC2 is not used, pins may be used as outputs (which also may float open if not used).
		Series terminations may be needed for some boards.
		CONFIG: TXD2[0:3] are "cfg_rom_loc[0:3]".
		CONFIG: TXD2[4] is "cfg_dram_type[0]".
		CONFIG: TXD2[5] is "cfg_tsec2_reduce".
		CONFIG: TXD2[6:7] are "cfg_tsec2_prtcl[0:1]".
	TSEC2_TX_EN	TXEN for all modes except RGMII, where it is TXCTL
		Optional: Series terminations may be needed for some boards.
	TSEC2_TX_ER	TXER may float if not used (RGMII mode).
		CONFIG: TXER is "cfg_dram_type".
	TSEC2_TX_CLK	TXCLK may float if not used (RGMII mode).
	TSEC2_GTX_CLK	Serves as TXCLK for most GMII/RGMII PHYs.
		Series terminations may be needed for some boards.
		RGMII requires +2ns delay on TXCLK relative to TXD/TXCTL, but most PHYs have software configuration options to eliminate that.
	TSEC2_CRS	Connect to ground for RMII/GMII/RGMII.
	TSEC2_COL	Connect to ground for RMII/GMII/RGMII.
	TSEC2_RXD[0:7] / GPIN[0:7]	If TSEC2 not used, may be used as inputs. If TSEC+GPIN not used, connect to pullups.
		RXD[4:7] are received data, except for MII+RMII+RGMII modes, where they should connect to ground (pulldown or direct).
		Series terminations are usually within the PHY
	TSEC2_RX_DV	RXDV for all modes except RGMII, where it is RXCTL
	TSEC2_RX_ER	RXER for all modes except RMII/RGMII, where it should connect to ground (pulldown or direct).
	TSEC2_RX_CLK	RXCLK for all modes except RMII, where it should connect to ground (pulldown or direct).
TSEC3		

Table 4. MPC8641D Design Checklist—eTSEC Controller Module (continued)

Check	Signal	Notes
	TSEC3_TXD[0:7]	TXD[4:7] may float unconnected for MII+RMII+RGMII modes.
		If TSEC2 is not used, pins may be used as outputs (which also may float open if not used).
		Series terminations may be needed for some boards.
		CONFIG: TXD3[0:1] are "cfg_spare[0:1]".
		CONFIG: TXD3[2] is "cfg_core1_enable".
		CONFIG: TXD3[3] is "cfg_core1_lm_offset".
		CONFIG: TXD3[5] is "cfg_tsec3_reduce".
		CONFIG: TXD3[6:7] are "cfg_tsec3_prtcl[0:1]".
	TSEC3_TX_EN	TXEN for all modes except RGMII, where it is TXCTL
		Optional: Series terminations may be needed for some boards.
	TSEC3_TX_ER	TXER may float if not used (RGMII mode).
	TSEC3_TX_CLK	TXCLK may float if not used (RGMII mode).
	TSEC3_GTX_CLK	Serves as TXCLK for most GMII/RGMII PHYs.
		Series terminations may be needed for some boards.
		RGMII requires +2-ns delay on TXCLK relative to TXD/TXCTL, but most PHYs have s/w config options to eliminate that.
	TSEC3_CRS	Connect to ground for RMII / GMII / RGMII.
	TSEC3_COL	Connect to ground for RMII / GMII / RGMII.
	TSEC3_RXD[0:7]	RXD[4:7] are received data, except for MII+RMII+RGMII modes, where they should connect to ground (pulldown or direct).
		Series terminations are usually within the PHY
	TSEC3_RX_DV	RXDV for all modes except RGMII, where it is RXCTL
	TSEC3_RX_ER	RXER for all modes except RMII/RGMII, where it should connect to ground (pulldown or direct).
	TSEC3_RX_CLK	RXCLK for all modes except RMII, where it should connect to ground (pulldown or direct).
TSEC4		
	TSEC4_TXD[0:7]	TXD[4:7] may float unconnected for MII+RMII+RGMII modes.
		Series terminations may be needed for some boards.
		CONFIG: TXD4[0:3] are "cfg_io_ports[0:3]".
		CONFIG: TXD4[5] is "cfg_tsec4_reduce".
		CONFIG: TXD4[6:7] are "cfg_tsec4_prtcl[0:1]".
	TSEC4_TX_EN	TXEN for all modes except RGMII, where it is TXCTL
		Optional: Series terminations may be needed for some boards.
	TSEC4_TX_ER	If reduced modes are used, TXER may float open.

Table 4. MPC8641D Design Checklist—eTSEC Controller Module (continued)

Check	Signal	Notes
	TSEC4_TX_CLK	TXCLK may float if not used (RGMII mode).
	TSEC4_GTX_CLK	Serves as TXCLK for most GMII/RGMII PHYs.
		Series terminations may be needed for some boards.
		RGMII requires +2ns delay on TXCLK relative to TXD/TXCTL, but most PHYs have s/w config options to eliminate that.
	TSEC4_CRS	Connect to ground for RMII / GMII / RGMII.
	TSEC4_COL	Connect to ground for RMII / GMII / RGMII.
	TSEC4_RXD[0:7]	RXD[4:7] are received data, except for MII+RMII+RGMII modes, where they should connect to ground (pulldown or direct).
		Series terminations are usually within the PHY
	TSEC4_RX_DV	RXDV for all modes except RGMII, where it is RXCTL
	TSEC4_RX_ER	RXER for all modes except RMII/RGMII, where it should connect to ground (pulldown or direct).
	TSEC4_RX_CLK	RXCLK for all modes except RMII, where it should connect to ground (pulldown or direct).
TSEC Clocks		
	EC(1:2)_GTXCLK	125.00 MHz, low-jitter clock source.
		Duty cycle must be within 47–53%.
		A PLL-based source is not recommended.
MI		
	EC_MDC	MI interface clock may need a series termination resistor if the net is very long.
	EC_MDIO	Open-drain, requires a pullup. 1K-1.5K is compatible with most PHYs.
		Pullup values + trace capacitance + IO capacitance may limit IO speed.

Table 4 shows the checklist for the local bus controller module in the MPC8641D.

Table 5. MPC8641D Design Checklist—Local Bus Controller Module

Check	Signal	Notes
Data Bus		

Table 5. MPC8641D Design Checklist—Local Bus Controller Module (continued)

Check	Signal	Notes
	LAD(0:31)	Multiplexed address/data bus -- address must be latched for local flash, etc. use.
		Data bus for data -- may be used directly if lightly loaded; otherwise use a buffer.
		Use an ALVCH32973 to latch the address and buffer the data (2 each for 32-bit bus).
		Use an ALVCH16373 to latch the address alone (1 or 2 devices, depending on addressing requirements).
		LAD(0:7) is the most-significant byte MSB, LAD(24:31) is the least-significant byte (LSB).
		Connect LAD0 to 8-/16-bit flash device D7 (MSB to MSB).
		CONFIG: These bits are sampled for user purposes. If not needed, pulldowns/pullups can be omitted.
	LA(27:31)	Burst address. Required for burst flash, optional for others.
		It is allowed to use LA(27:31) with latched LAD(0:26), or you can latch LAD(0:31).
		CONFIG: These bits configure the PLLs and ***require*** a pullup/pulldown.
	LDP(0:3)	Connects to parity of memory devices.
		LDP(0) associates with LAD(0:7), and so forth.
		CONFIG: These bits configure the PLLs and ***require*** a pullup/pulldown.
Controls		
	LALE	Connects to ALE pin(s) of address bus latches.
		Recommend: Keep routing short; match length relative to LAD bus.
	LBCTL	Connects to direction (DIR) pin of bidirectional bus buffers.
		May be left disconnected if buffers are not used.
	LGPL0/LSDA10	Connects to A10 of SDRAM, if used. NC otherwise
	LGPL1/$\overline{\text{LSDWE}}$	Connects to WE* of SDRAM if used. NC otherwise
		NOTE: This is not used for GPCM (flash, etc.) WE* controls -- use $\overline{\text{WE}}$(0:3)
	LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$	Connects to output enable (OE*, FOE*, G*) for GPCM functions such as flash.
		Connects to RAS* of SDRAM if used.
	LGPL3/$\overline{\text{LSDCAS}}$	Connects to CAS* of SDRAM if used. NC otherwise
		CONFIG: LGPL3+LGPL5 configures "cfg_boot_seq[0:1]" mode.
	LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPERR	NOTE: Always enabled for GPCM (boot flash) -- must have a pullup!
		$\overline{\text{LGTA}}$ may be used to shorten (default) or indefinitely delay (if selected) GPCM cycles.
		$\overline{\text{LGTA}}$ is **not** the same as READY/BUSY* on most flash devices.
	LGPL5	**CONFIG**: LGPL3+LGPL5 configures "cfg_boot_seq[0:1]" mode.
		LGPL5 is not used in most flash-interfaces and can float if not used.

Table 5. MPC8641D Design Checklist—Local Bus Controller Module (continued)

Check	Signal	Notes
	LCS(0:4)	Connects to chip-select pins (CS*, etc.) of local bus devices.
		Recommend: Add a pullup for power-up/power-down transition protection.
	LCS[5] / DMA_DREQ[2]	Connects to chip-select pins (CS*, etc.) of local bus devices.
		Recommend: Add a pullup for power-up/power-down transition protection.
	LCS[6] / DMA_DACK[2]	Connects to chip-select pins (CS*, etc.) of local bus devices.
		Recommend: Add a pullup for power-up/power-down transition protection.
	LCS[7] / DMA_DDONE[2]	Connects to chip-select pins (CS*, etc.) of local bus devices.
		Recommend: Add a pullup for power-up/power-down transition protection.
	LWE(0:3) / LSDDQM[0:3] / LBS[0:3]	GPCM, 8 bits: LWE(0) associates with LAD(0:7), LWE(1) associates with LAD(8:15), and so forth.
		GPCM, 16 bits: LWE(0:1) associates with LAD(0:15), LWE(2:3) associates with LAD(16:31).
		If a device accepts only 16-bit accesses (i.e. a 16-bit wide flash), use LWE(0).
		Recommend: Add pullups for power-up/power-down transition protection.
		CONFIG: LWE(0) configures "cfg_cpu_boot" mode.
		CONFIG: LWE(1) configures "cfg_rio_sys_size" mode.
		CONFIG: LWE(2:3) configures "cfg_host_agt[0:1]" mode.
	LCKE	Connects to CKE of SDRAM, if used. May be left disconnected otherwise
Clock		
	LSYNC_OUT	Generally connects to LSYNC_IN.
		Optional: If LCLK(0:2) are needed, connect to a series-resistor (10-47 ohms) to allow clock skew tuning.
		Optional: If LCLK(0:2) are needed, connect a capacitor (10-47pF) between LSYNC_OUT and GROUND to allow clock delay tuning.
	LSYNC_IN	May not float, should be connected to LSYNC_OUT.
	LCLK(0:2)	Connects to SDRAM SDCLK or other local-bus clock devices.
		May float open if not used.
		Software can disable LCLK outputs to minimize EMI.

Table 6 shows the checklist for the SerDes controller module in the MPC8641D.

Table 6. MPC8641D Design Checklist—SerDes Controller Module

Check	Signal	Notes
PCI Express Mode		

Table 6. MPC8641D Design Checklist—SerDes Controller Module (continued)

Check	Signal	Notes
	SDx_RX[0:7] / $\overline{\text{SDx\_RX}}$[0:7]	Route as differential pair.
		Keep overall length < 12 inches.
		Unused lanes should be connected to ground.
		Unused lanes connected to a PCIExpress slot may float per PCI Express rules.
	SDx_TX[0:7] / $\overline{\text{SDx\_TX}}$[0:7]	Route as differential pair.
		Keep overall length < 12 inches.
		Unused lanes may be disconnected.
		DC blocking capacitors are required per specification and should be placed equally within ~2-3 cm.
	SDx_REF_CLK / $\overline{\text{SDx\_REF\_CLK}}$	Route as differential pair.
		Keep overall length < 12 inches.
		Connect to a 100.00 MHz clock source.
		Clock must be <= 100 ps jitter (cycle-to-cycle) and ±50 edge-to-edge.
		Recommend: Use clocks which exceed the above minimum if possible.
		If SerDes module is not used, connect both to ground.
	Reserved (H30, R32, V28, AG32) (SDx_RSV[0:1])	These pins must be connected to SVDD.
	Reserved (H29, R31, W28, AG31) (SDx_RSV_B[0:1])	These pins must be pulled down to ground with a 300-Ω resistor.
	Reserved (K24, K25, P29, P29 W26, W27, AD25, AD26) (SDx_NC[0:3])	These pins must remain unconnected. Test points are acceptable.
	SDx_DLL_TPA	This pin must remain unconnected. A test point is acceptable.
	SDx_DLL_TPD	This pin must remain unconnected. A test point is acceptable.
	SDx_PLL_TPA	This pin must remain unconnected. A test point is acceptable.
	SDx_PLL_TPD	This pin must remain unconnected. A test point is acceptable.
	SDx_IMP_CAL_TX	Connect a 100 Ω, 1% resistor to ground.
		Keep the trace relatively short (<= 1cm).
		Avoid cross-coupled noise.

Table 6. MPC8641D Design Checklist—SerDes Controller Module (continued)

Check	Signal	Notes
	SDx_IMP_CAL_RX	Connect a 200 Ω, 1% resistor to ground.
		Keep the trace relatively short (<= 1cm).
		Avoid cross-coupled noise.
Serial RapidIO (SRIO) Mode		
	SD2_RX[0:3] / SD2_RX_B[0:3]	Unused in SRIO mode: connect to ground.
		Note that SERDES1 does not support SRIO.
	SD2_RX[4:7] / $\overline{\text{SD2\_RX[4:7]}}$	Route as differential pair.
		Keep overall length < 12 inches.
		Unused lanes should be connected to ground.
		DC blocking capacitors are required per specification and should be placed equally within ~2-3 cm.
	SD2_TX[0:3] / $\overline{\text{SD2x\_TX[0:3]}}$	Unused lanes, leave disconnected.
		Keep overall length < 12 inches.
	SD2_TX[4:7] / $\overline{\text{SD2\_TX[4:7]}}$	Route as differential pair.
		Keep overall length < 12 inches.
		Unused lanes may be disconnected.
	SD2_REF_CLK / $\overline{\text{SD2\_REF\_CLK}}$	Route as differential pair.
		Keep overall length < 12 inches.
		Connect to a 100.0 or 125.00 MHz clock source.
		Clock must be <= 80 ps jitter (cycle-to-cycle) and ±40 edge-to-edge.
		Recommend: Use clocks which exceed the above minimum if possible.
	Reserved (H30, R32, V28, AG32)	These pins must be connected to SVDD.
	Reserved (H29, R31, W28, AG31)	These pins must be pulled down to ground with a 300-Ω resistor.
	Reserved (K24, K25, P29, P29 W26, W27, AD25, AD26)	These pins must remain unconnected. A test point is acceptable.
	SDx_DLL_TPA	This pin must remain unconnected. A test point is acceptable.
	SDx_DLL_TPD	This pin must remain unconnected. A test point is acceptable.
	SDx_PLL_TPA	This pin must remain unconnected. A test point is acceptable.
	SDx_PLL_TPD	This pin must remain unconnected. A test point is acceptable.

Table 6. MPC8641D Design Checklist—SerDes Controller Module (continued)

Check	Signal	Notes
	SDx_IMP_CAL_TX SDx_IMP_CAL_RX	Connect a 100 Ω, 1% resistor to ground.
		Keep the trace relatively short (<= 1cm).
		Avoid cross-coupled noise.
		Connect a 200 Ω, 1% resistor to ground.
		Keep the trace relatively short (<= 1cm).
		Avoid cross-coupled noise.

3 Revision History

Table 7 provides a revision history for this application note.

Table 7. Document Revision History

Rev. Number	Date	Substantive Change(s)
1	11/2013	Added simple acknowledgement that document also applies to MPC8640D and MPC8640. Clarified conflicting SYSCLK requirements.
0	02/2010	Initial public release

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: AN3089
Rev. 1
11/2013