

Power Supply Design Guidelines for the MPC8641 and MPC8641D

by *Networking and Multimedia Group*
Freescale Semiconductor, Inc.
Austin, Texas

This application note is a design guide to assist in creating a high-quality power delivery system for the Power Architecture™-based MPC8641 and MPC8641D integrated host processors. This document does not replace the device reference manual or hardware specifications. References to the MPC8641 apply to both the MPC8641 single-core processor and the MPC8641D dual-core processor, unless otherwise noted.

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1 Overview

The MPC8641 processor family supports one or two cores running at high frequencies, coupled by high-frequency internal bus interfaces. Consequently, the core power supply requirements are more demanding than those for previous generations of Power Architecture™ processors.

In this document, the power delivery system (PDS) includes the power supply, printed circuit board (PCB) plane, and load (in this case, one or two processor cores). When a system is designed, thinking in terms of the PDS helps reinforce the importance of considering the entire system and not just the power supply.

2 Power Supply Requirements

The MPC8641 requires several power supplies for each of several functional subsystems (DDR, Ethernet, SerDes, and so forth) as well as the interconnect fabric itself (the platform voltage). The total number of supplies a system needs depends on the interfaces, the interface voltages required to connect with external peripherals, and the number of those voltages that are common and shareable.

See the *MPC8641 and MPC8641D Integrated Host Processor Hardware Specifications* (MPC8641DEC) for accurate voltage and current requirements (for help obtaining this document, contact a Freescale representative). For convenience, [Table 1](#) provides a snapshot of the MPC8641 power requirements at the date of this application note.

Table 1. MPC8641 Power Requirements¹

Power Source	Symbol	Typical Voltage	Tolerance	P _{MAX}
Core power	V _{DD_CORE0} V _{DD_CORE1}	1.1 V	± 50 mV	23.2 W
PLL filter	AV _{DD_CORE0} AV _{DD_CORE1}	1.1 V	± 50 mV	50 mW
Platform (internal buses)	V _{DD_PLAT} AV _{DD_PLAT}	1.1 V	± 50 mV	6 W
SERDES	SV _{DD} XV _{DD}	1.1 V	± 50 mV	0.71W
DDR2 bus	D1_GV _{DD} D2_GV _{DD}	1.8 V	± 90 mV	0.60 W
Ethernet (4X)	LV _{DD} TV _{DD}	2.5 V	± 125 mV	0.24 W
Local bus	OV _{DD}	3.3 V	± 125 mV	0.33 W

Note:

¹ These figures are subject to change without notice. Consult the latest version of the *MPC8641 and MPC8641D Integrated Host Processor Hardware Specifications*.

Note that [Table 1](#) lists the power requirements for the MPC8641 only; it does not include requirements for external devices, memory, and so forth. At the very least, additional power is needed to drive connected I/O pins, and the internal logic of the other devices is often shared with the MPC8641D supplies.

The application note, *Power Supply Design for Power PC™ Processors (AN2747)*, describes the general principles for PDS designs for many earlier Power Architecture processors. To supplement that document, Table 1 in AN2747 requires additional data to cover the MPC8641D. These values are listed in [Table 2](#).

Table 2. MPC8641 Processor Parameters

Processor	Parameter							No. of VDD pins	Notes
	V _{SUPPLY}	P _{MAX}	I _{MAX}	V _{RIPPLE}	V _{RIPPLEPCT}	di/dt	Z _{TARGET}		
MPC8641 @ 1.5 GHz	1.1 V	28.9 W	26.3 A	± 50 mV	4.5%	0.2 A/ns	2.4 mΩ	28	1, 2
MPC8641D @ 1.5 GHz	1.1 V	49.9 W	45.4 A	± 50 mV	4.5%	0.4 A/ns	1.2 mΩ	56	1

Notes:

- 1 Subject to change without notice.
- 2 Or equivalently MPC8641D with cores powered separately.

As expected from the entries in [Table 2](#), high current transients are present on the VDD_CORE[0:1] power pins. Therefore, designers need to pay careful attention and properly bypass the power pins. There must be a good connection between the BGA pads and the power and ground planes. In particular, the SMD capacitors should have vias directly embedded to the bypass capacitor pads if at all possible.

2.1 Sharing Power Supplies

To reduce the number of supplies needed, accept the trade-offs that occur when non-optimized settings are used. [Table 3](#) shows the MPC8641 power requirements.

Table 3. MPC8641 Power Requirements

Power Source	Symbol	Voltage	Trade-Off Notes
Core Power + PLL Filter	V _{DD_CORE0} V _{DD_CORE1} AV _{DD_CORE0} AV _{DD_CORE1} AV _{DD_PLAT}	1.05 V or 1.1 V	Use of lower voltages may limit core and/or platform/DDR speeds.
Platform (internal buses)	V _{DD_PLAT}		
SERDES	SV _{DD} XV _{DD}		
Memory	D1_GV _{DD} D2_GV _{DD}	1.8 V	Memory could be merged with 2.5 V by configuring for DDR instead of DDR2, but since VTT supplies often supply the I/O power this is not all that useful.
Ethernet	LV _{DD} TV _{DD}	2.5 V or 3.3 V	2.5 V readily usable with PHYs; however, 3.3 V is not suitable for RGMII mode.
Local Bus	OV _{DD}		2.5 V requires low-voltage flash memory and so forth

For sensitive supplies (such as XVDD and SVDD), a key requirement for power sharing is that the planes be relatively isolated. One effective strategy is to route the power planes separately and tie them together at the power source. See [Figure 1](#).

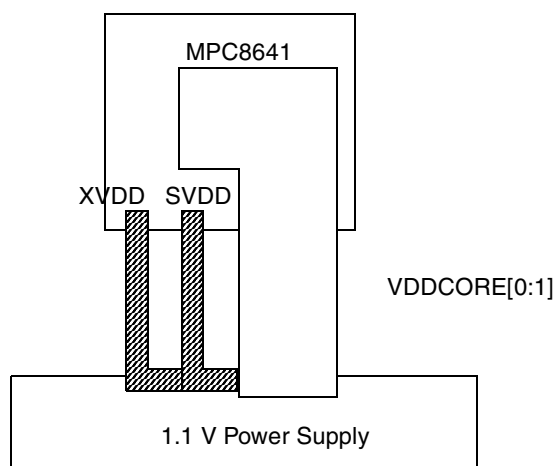


Figure 1. Common Source Split Planes

Another strategy is to use low-pass filters or ferrite beads to eliminate coupled noise, as long as there is sufficient current capacity in the components and connections. In either case, once separated, treat these planes as independent power planes and route and bypass them separately.

2.2 Unused Power Supplies

Note that in some cases, if a design does not need an entire interface, it is permitted to connect the respective rail to ground. [Table 4](#) shows MPC8641 power disconnect options.

Table 4. MPC8641 Unused Power Options

Power Source	Power Pin	Groundable
Core power	V _{DD_CORE0}	No. Core 0 is the only processor active out of reset/boot-hold off, manager and so must always run.
	V _{DD_CORE1}	Yes
PLL filter	AV _{DD_CORE0}	No
	AV _{DD_CORE1}	Yes
Platform (internal buses)	V _{DD_PLAT}	No
	AV _{DD_PLAT}	
SerDes	SV _{DD} XV _{DD}	No
Memory bus	D1_GV _{DD} D2_GV _{DD}	Yes. Memory buses may not be dynamically powered up/down.
Ethernet	LV _{DD} TV _{DD}	Yes
Local bus	OV _{DD}	No (some critical non-local-bus signals are controlled by the OVDD rail)

3 Power Supply Design

After the supply parameters are defined, including required capacity, begin designing the power supplies.

3.1 Non-Core Power Supplies

Start with the easy supplies—that is, everything except VDD_CORE[0:1]. All non-core supplies use less than 10 W and are easily handled by integrated modules or by switching-regulator ICs with integrated FETs. The Argo Navis MPC8641D development platform uses the Texas Instruments TPS54310 to provide the 1.1–1.2 V VDD_PLAT platform voltage, although many other suitable choices are available from Freescale Semiconductor, SemTech, Linear Technology, Zilker Labs, and others. As seen in the Argo Navis schematics, the device requires only an inductor, output filtering capacitors, and a few discrete components. [Figure 2](#) shows an example of the VDD_PLAT supply. The schematic in [Figure 2](#) may serve as a template for VDD_PLAT and other supplies, or smaller and less expensive devices may be used for VDD_SERDES, LVDD, TVDD, and so forth, because their power consumption is much less than VDD_PLAT.

3.2 Core Power Supplies

The core supply needs to deliver power to one or two cores, either as a single supply or as one of two independent supplies. The designer can select either type based on design requirements. [Table 5](#) summarizes the trade-offs between the two approaches.

Table 5. Single/Dual Power Supply Trade-Offs

Supply Type	Advantages	Disadvantages
One PSU for each core	<ul style="list-style-type: none"> Disabled cores can be powered down for maximum power savings. Second PSU can be depopulated if board is built with single-core MPC8641. 	<ul style="list-style-type: none"> Larger size More components
One PSU for all cores	<ul style="list-style-type: none"> Usually smaller size Fewer components 	<ul style="list-style-type: none"> Multi-phase solution may cost more Over-designed for single-core MPC8641 board.

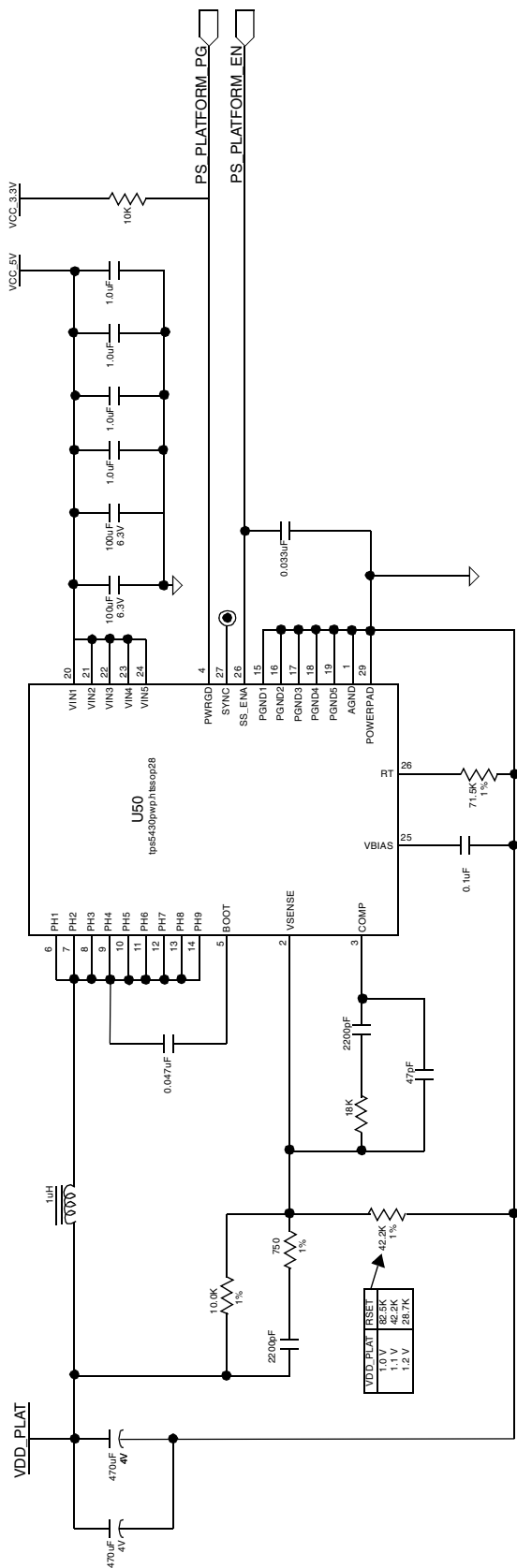


Figure 2. VDD_PLAT and Other Power Supplies

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Figure 3 shows the power supply controller schematic used for the MPC8641D development platform, Argo Navis, which opts for a single supply for both cores. The design is based on the SemTech SC458 two-phase switching power supply controller.

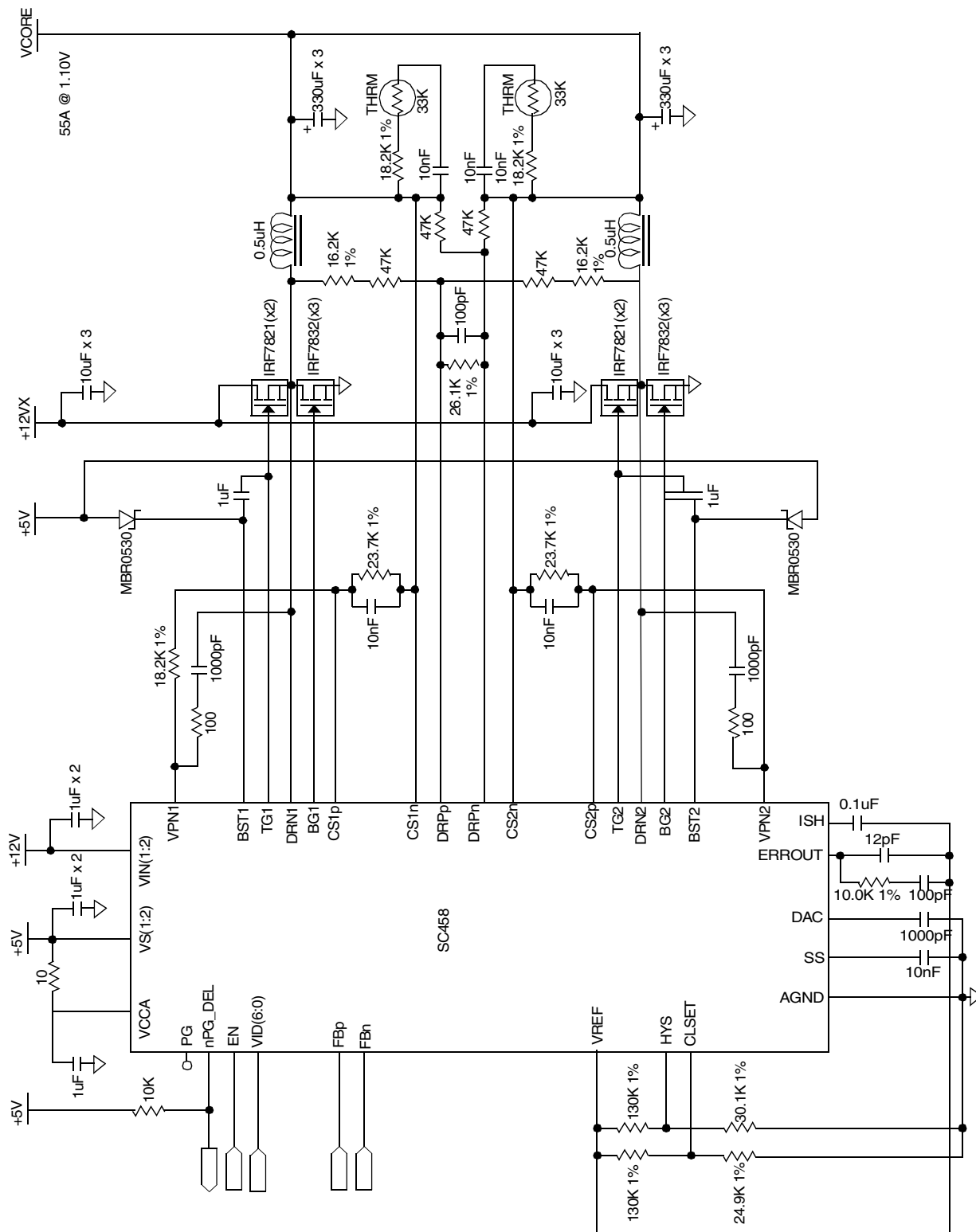


Figure 3. VDD_CORE Supply Example

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4 Power Delivery System

It is not sufficient to drop in a power supply for VDD_CORE[0:1] and other supplies without planning the design of the power planes on the PCB, as well as the number and placement of the high- and low-frequency bypass capacitors that supply power transiently to the MPC8641. Before delving into the details of the power delivery system (PDS), first here are a few summary facts to keep in mind. The MPC8641D has 1023 interconnects arranged as a 32×32 array (with pin A1 missing) in a 1 mm pitch. The BGA pads and vias usually have the physical parameters listed [Table 6](#) (though other dimensions are possible).

Table 6. MPC8641D Escapement Dimensions

Dimension	Size	Notes
Drill Diameter	13 mils	—
Finished Hole Size (FHS)	10 mils	After plating
Pad	19 mils	—
Anti-pad	30 mils	Clearance from via pads to adjacent plane area-fills.
Thermal Relief	33 mils ²	—
Via keepout	23 mils	As above, but for traces on signal (inner) planes.

4.1 Bypass Capacitor Placement

Keep the following points in mind while reading this section:

- This section is based on the padstack dimensions in [Table 6](#). If a different padstack is used, most or all of the numbers derived probably need to be recalculated.
- It is assumed that each BGA connection carries current equally, no matter its proximity to the power supply and/or processor internal power pads. In reality, the current is non-uniformly distributed due to internal BGA-to-die substrate connections and other factors. There are no guaranteeable distributions among the power pins.
- All comments in this section about power planes apply equally to the return ground. Multilayer PCBs often have multiple ground planes, so this restriction is occasionally overlooked; however, the ground return path requirements are exactly equal to the power source path requirements.

Because of the high-current transients on the VDD_CORE[0:1] power pins, take care to bypass these power pins and to provide a good connection between the BGA pads and the power and ground planes. In particular, the SMD capacitors should have pads directly attached to the via ring (or even better, within it using via-in-pad methods). [Figure 4](#) shows the dispersion of VDD_CORE0 and VDD_CORE1. Note that this is an X-ray view, from the top of the board, of the center portion of interest in the 32×32 BGA array.

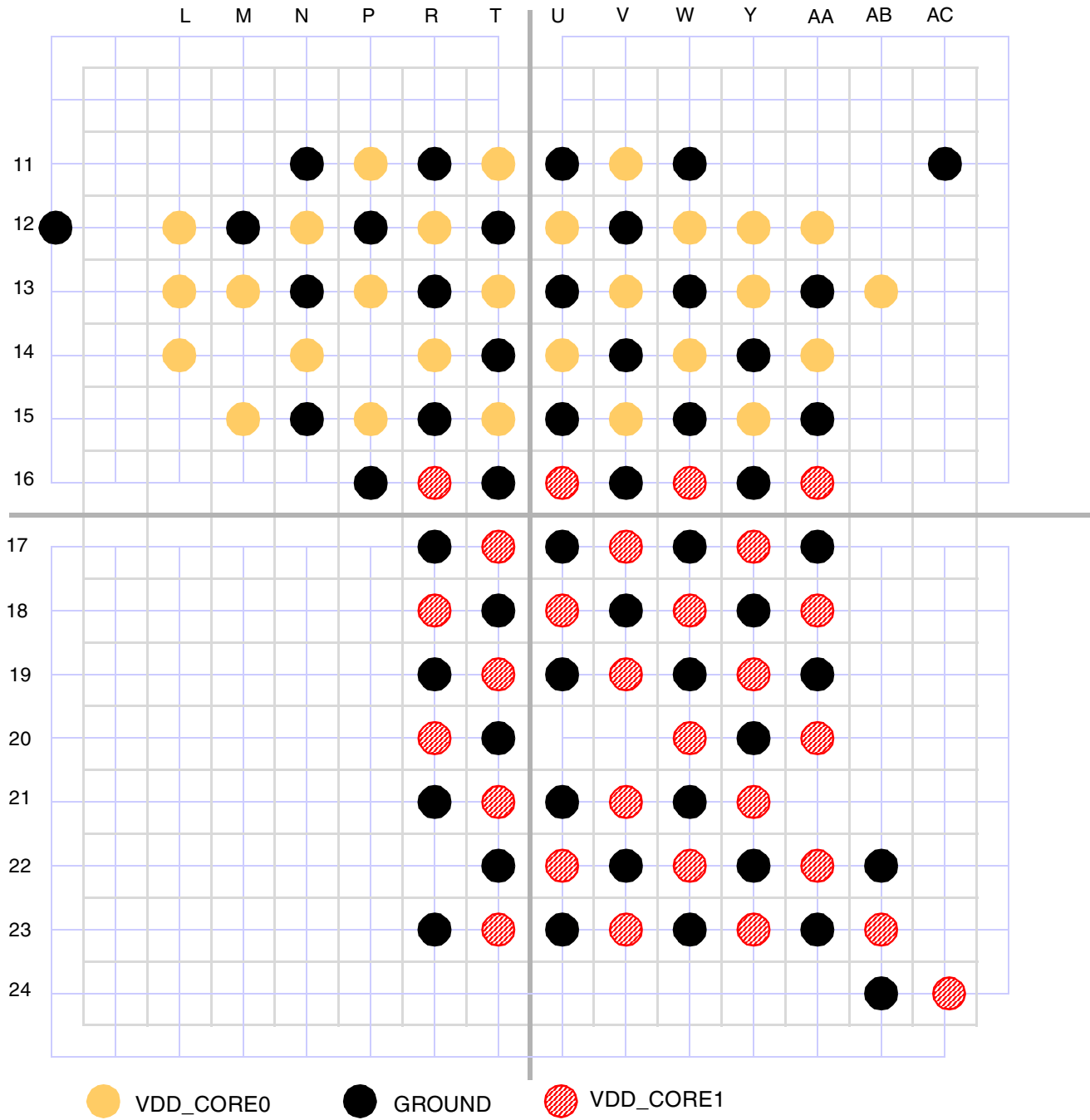


Figure 4. MPC8641 VDD_CORE[0:1] and Ground Pattern

After the power and grounds are escaped, the SMD 0402 capacitors can be placed so that the capacitor pads attach directly to the power vias on the side. Minimize or eliminate the trace between the via and the capacitor pad. [Figure 5](#) shows three possible attachment methods.

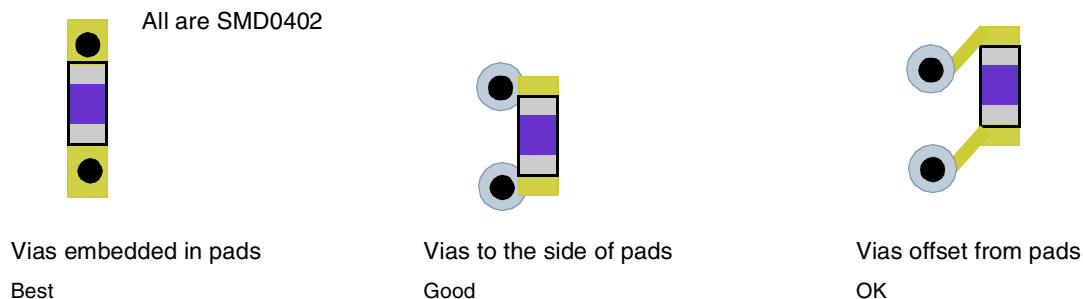


Figure 5. MPC8641 SMD Capacitor Via Placement

Using either of these methods, [Figure 6](#) shows the relative attachment of the SMD 0402 capacitors. Again, this is a view through the top of the board.

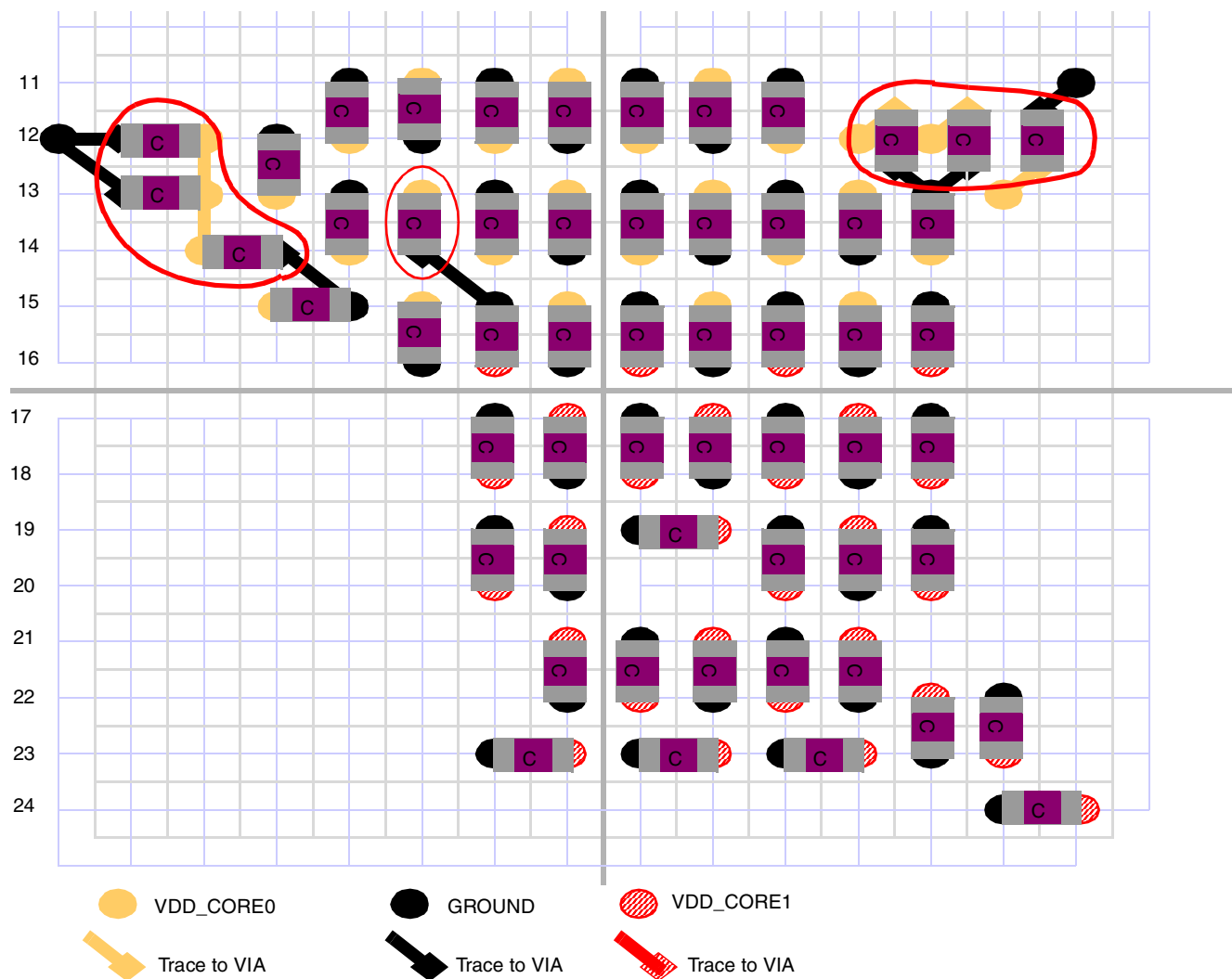


Figure 6. MPC8641 VDD_CORE[0:1] and Ground SMD 0402 Capacitor Placement

This pattern provides an attachment for 56 bypass capacitors, 49 of which connect directly to a via. The other seven are circled in [Figure 6](#). These seven capacitors on the VDD_CORE0 rail cannot be placed directly on a ground via, but instead need a trace to a nearby ground point. The inductance of this trace slightly reduces the effectiveness of these capacitors. Other capacitors, such as those required for VDD_PLAT, VDD_SERDES, and so forth, are not shown but can be attached in the same way.

If the PCB is not permitted to use via-in-pad connections, the capacitors can be shifted to attach to a pad in the area between the BGA pads, similar to the way in which the seven other capacitors are handled. In that case, use the same relative pattern, but each capacitor shifts a little.

4.2 Bulk Capacitors

Bulk capacitors can be placed outside the periphery of the MPC8641 die, as close as reasonably possible. Systems with heatsinks and/or sockets probably need some additional spacing, but the high-frequency capacitors handle the fastest transients, allowing the bulk capacitors to be spaced a little further away. Keep them within 2 cm. [Figure 7](#) shows the MPC8641 VDD_CORE[0:1] and ground SMD0402 capacitor placement.

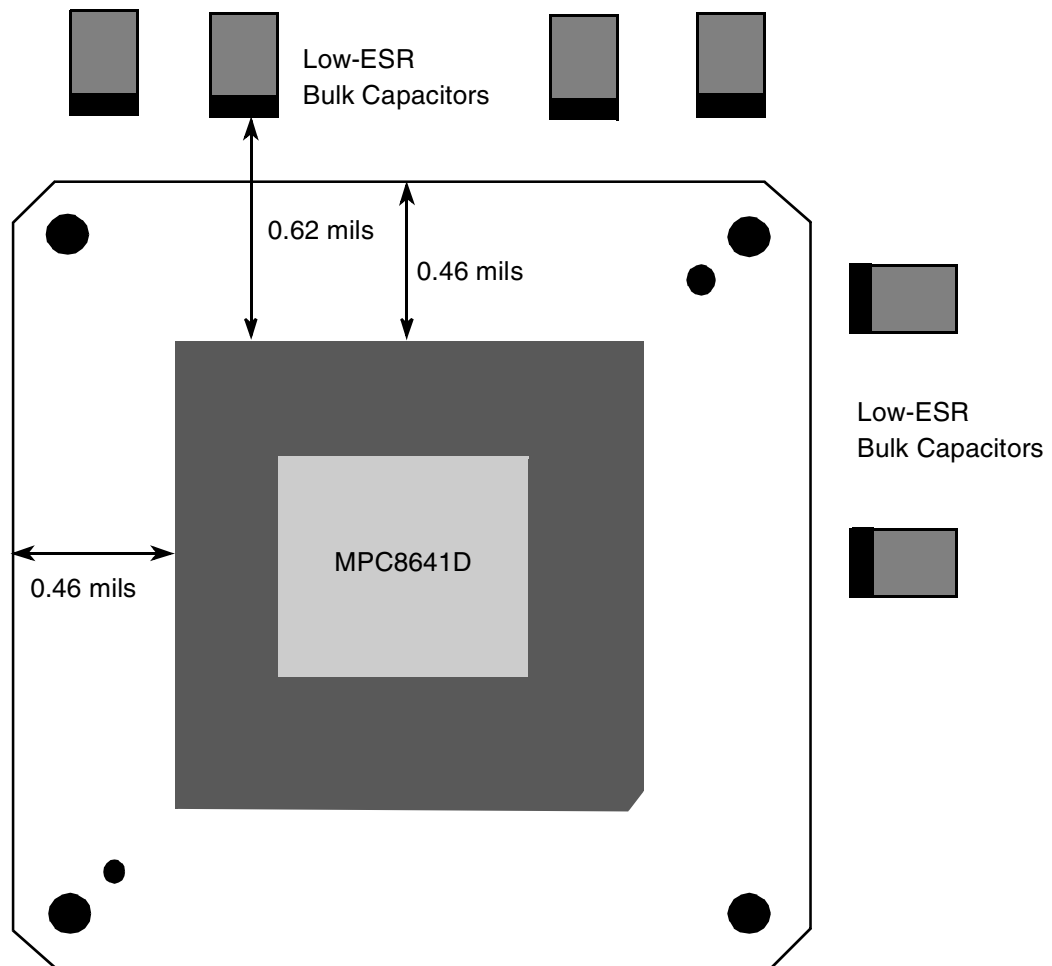


Figure 7. MPC8641 Bulk Capacitor Placement

5 PCB Layout

In addition to bypass capacitor placement, the designer must also consider the wholesale delivery of power to the VDD pins. On most PCBs, the power plane is not actually solid, but is perforated by numerous vias. This is illustrated in [Figure 8](#), where the wide plane is actually only as wide as its narrowest point.

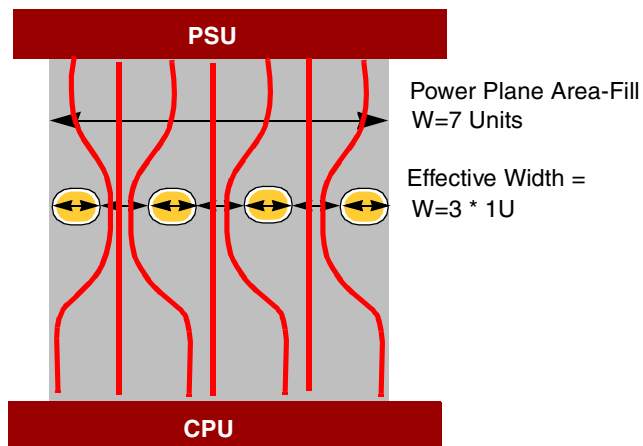


Figure 8. Restricted Current Flow

For many applications, the effect of the vias passing through the power plane on the flow of current is insignificant. However, as the power reaches the outer periphery of the MPC8641, it must flow through the outer array of signal BGA vias. While some BGA pads may not need vias (outer BGA pads may be able to route out on the top layers); in most cases the number of interfering vias ranges from 8 to 11. [Figure 9](#) shows a view of the MPC8641 power pins surrounded by potential via sites.

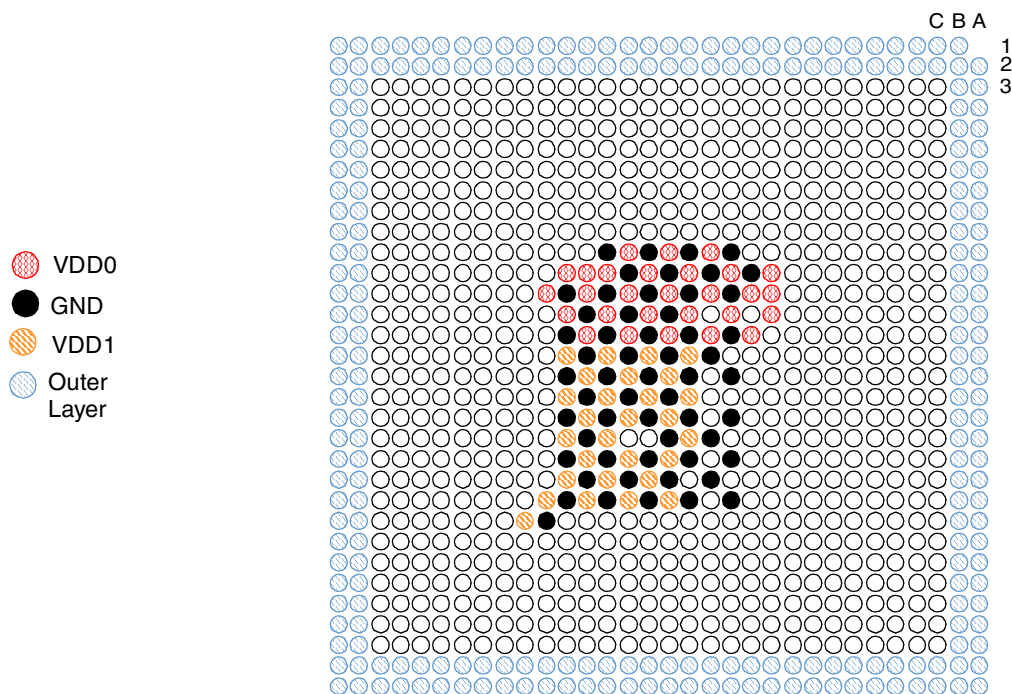


Figure 9. MPC8641D VDD_CORE[0:1] Power Pins Surrounded by Potential Vias

For many layouts, the outer one or two BGA pads do not require vias (assuming dual-track routing); these signals are instead “escaped” on the top layer of the PCB. This is particularly common for the MPC8641D SERDES (Serial RapidIO and PCI Express) ports. Delivering power properly to the power pins requires planning the flow of current around these vias, or more properly, the antivias or antipads that surround the via and cause a hole on the power plane layer. When coupled with a 1-mm spacing, the cross section of the PCB typically resembles that shown in Figure 10.

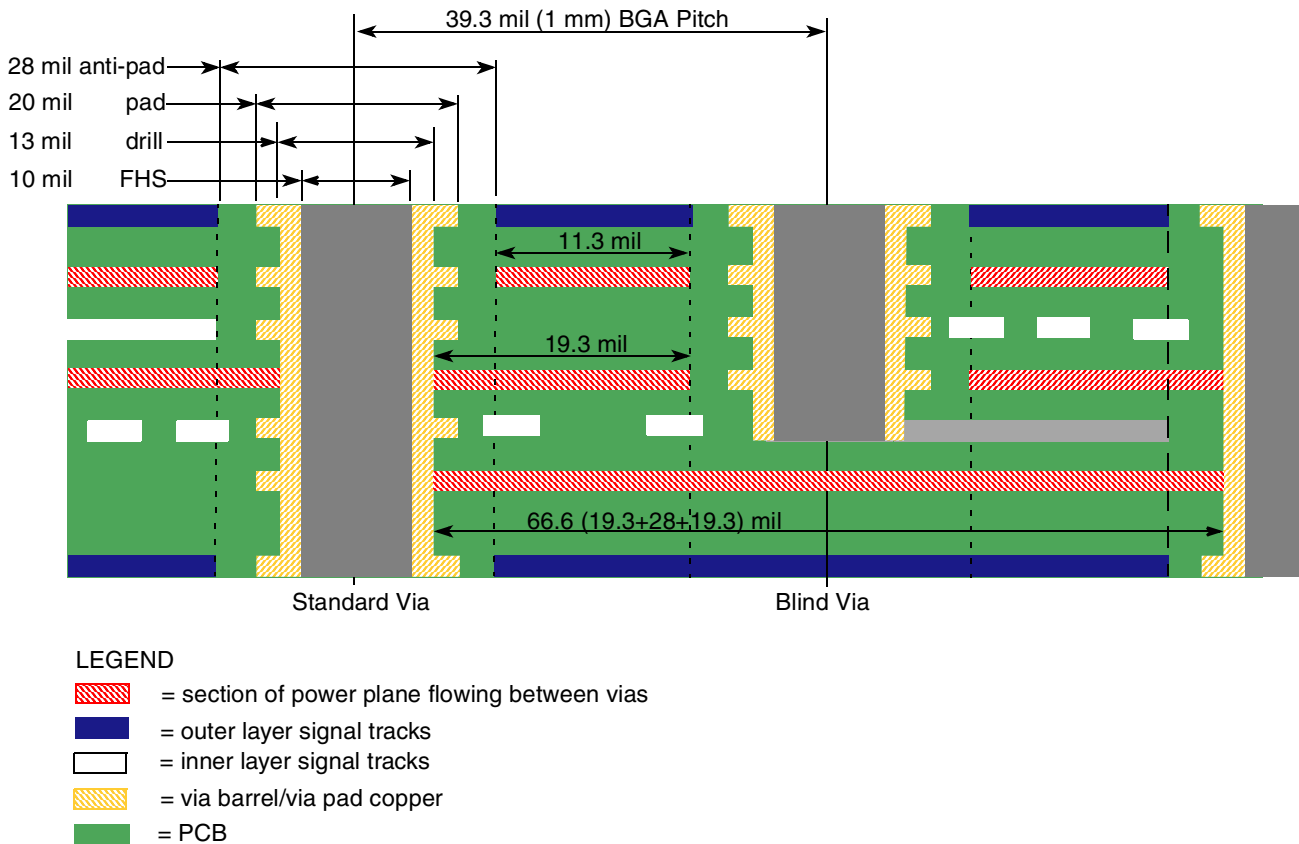
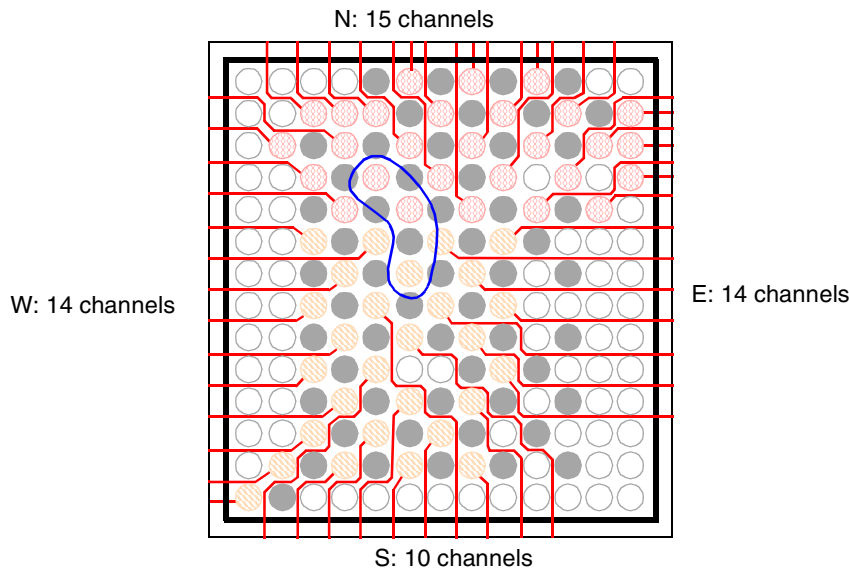


Figure 10. PCB Cross-Section

The anti-pad is larger than the spacing between the via barrels; it is this dimension between the inner via barrels that reduces the width and therefore the current capacity of the trace. In effect, the power plane is not a solid plane but a parallel array of traces with one of the following widths:

- 11.3 mils, when planes must be isolated from both vias
- 19.3 mils, when planes connect to one of the vias
- 66.6 mils, when blind or buried vias do not perforate the power plane

Assuming conventional through-hole vias are used, current must flow around the outer 7–9 rows of vias as shown in Figure 9, to get to the central VCORE vias, as shown in as shown in Figure 11. It does not matter whether these are literal power traces or just symbolic of the flow of current in a solid plane, nor does it matter whether they are on inner or outer layers (at this point).



Maximum number of channels between vias: 1, with 3 exceptions

— = Current Flow Channel

Figure 11. VDD_CORE Inner Current Flow

Figure 11 shows how current can flow from all directions into the VCORE area of the MPC8641D and supply current across a fixed-width PCB trace. Given the approximate physical dimensions and quantity of copper traces available to conduct current between the PDS and the processor, calculations can determine the limits of those traces with respect to temperature rise, copper plating used, and the layer(s) on which the copper resides. As a result, one of the following conditions may be true:

- The connections are sufficient as-is.
- The connections are sufficient given much higher temperature rise.
- The planes must be placed only on the outer layers.
- The connections must use heavier copper plating.
- Two or more parallel power planes are needed.

A combination of some of these approaches may be needed.

The standard formulae to determine the limits of the copper trace are described in the IPC-2221A standard and are given by:

$$I_{(\text{Trace, Outer})} = 0.048 \times (\text{maxTempRise})^{0.44} \times (\text{viaPlating} \times \text{viaDiameter} \times \pi)^{0.725} \quad \text{Eqn. 1}$$

$$I_{(\text{Trace, Inner})} = 0.024 \times (\text{maxTempRise})^{0.44} \times (\text{viaPlating} \times \text{viaDiameter} \times \pi)^{0.725} \quad \text{Eqn. 2}$$

Using these formulae, and using a 11 mil trace as a standard (rounded down from the actual 11.3 mil max trace width), for various layout rules the amount of current that can be safely carried, assuming a maximum temperature rise of 20°C, is shown in [Table 7](#).

Table 7. Current-Carrying Capacity per Standard IPC2221A.

Location	Copper Plating	A/11 mil trace	North (15x)	South (10x)	East/West (14x each)	Total
Outer	0.5 oz.	0.777 A	11.66 A	7.77 A	10.88 A	41.18 A
	1.0 oz.	1.285 A	19.28 A	12.85 A	17.99 A	68.11 A
	1.5 oz.	1.730 A	25.95 A	17.30 A	24.22 A	91.69 A
	2.0 oz.	2.130 A	31.95 A	21.30 A	29.82 A	112.89 A
Inner	0.5 oz.	0.390 A	5.85 A	3.90 A	5.46 A	20.67 A
	1.0 oz.	0.582 A	9.68 A	6.45 A	9.03 A	34.19 A
	1.5 oz.	0.865 A	12.98 A	8.65 A	12.11 A	45.85 A
	2.0 oz.	1.065 A	15.98 A	10.65 A	14.91 A	56.45 A

The shaded areas in [Table 7](#) meet or exceed MPC8641D requirements. This table indicates that using 1oz copper on a single external layer is sufficient, while using 2oz copper on an inner layers is, at best, marginal. Unfortunately, due to the BGA escape pattern, it may be very difficult to provide power planes on the external layers of the board. Given these limitations, the following power plane strategies work:

- 1oz copper area fill on an outer layer 68.1A, max
- 1oz copper area fill on two inner layers 68.4A, max
- 0.5oz copper area fill on three inner layers 62.0A, max

5.1 Via Current Capacity

Unless the power is delivered on the top plane and attaches directly to the BGA pad of the processor (which as noted is fairly difficult to accomplish), power is delivered from one or more PCB planes to the processor through vias. Given the padstack parameters in [Table 6](#) and the number of vias mentioned there (49), the next step to ensure a quality PDS is to evaluate the individual and aggregate via current capacity using the following formula:

$$I_{VIA} = 0.048 \times (\maxTempRise)^{0.44} \times (\text{viaPlating} \times \text{viaDiameter} \times \pi)^{0.725} \quad \text{Eqn. 3}$$

[Table 8](#) shows a few via current capacities for given PCB process parameters.

Table 8. Via capacity

maxTempRise	viaPlating	viaDiameter	I _{VIA}	Notes
10 °C	1 mil	10 mil	1.609 A	Standard
10 °C	1 mil	11 mil	1.724 A	—
10 °C	1 mil	15 mil	2.159 A	—
10 °C	1.5 mil	10 mil	2.159 A	—
20 °C	1 mil	10 mil	2.183 A	—

At 1.609 A/via and with 49 vias, we have a maximum current capacity of 78.86 A, which is clearly sufficient margin for the MPC8641D.

5.2 Alternate Plane Current Capacity

Research performed by Johannes Adam of Flomerics as preparatory work for a revision to one of the rules of the IPC2221 standard (specifically, design rule 2152), found that the formula for outer traces was based upon materials and assumptions no longer prevalent. Additionally, he discovered that the 50 percent derating factor used for inner traces is wholly arbitrary and should be approximately 5 percent. In particular, thermal conduction to adjacent traces and power planes was found to be vastly more important than conduction to free space. Refer to the references section for details on this paper and associated historical data.

At the time of publication, the IPC2221 has not been updated based upon these finding, so the designer can either follow the published standards and accept overly conservative numbers or incorporate the pending changes. Freescale cannot recommend one course over the other and advises designers to consult the original source documentation and decide for themselves. Examining the IEEE paper, “case 5” shows an outer trace of variable width over a 35um (1 oz. copper) plane. This correlates nicely with an external power connection residing over an inner ground plane immediately adjacent to it. Such a plane is desirable not only for power purposes but for routing differential pairs such as those on the SERDES or DDR interfaces. Extracting the data for a 0.3mm trace (~11 mils), and applying a curve fitting process to the data produces the following formula, which is represented in [Figure 12](#):

$$T(\text{trace}) = 19.473 + 3.228IMAX + 4.469IMAX^2 + 0.385IMAX^3 \quad \text{Eqn. 4}$$

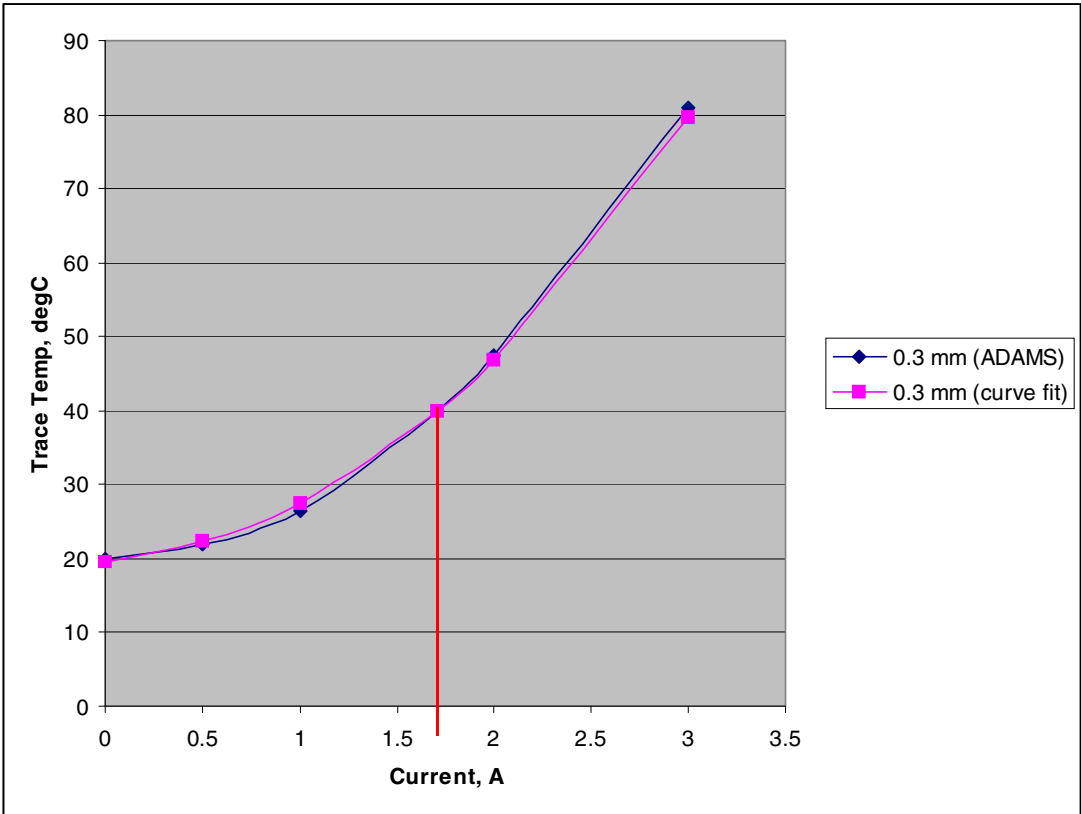


Figure 12. Extrapolated Current Flow

WARNING

This curve is valid only for the 0.3 mm trace. The IPC standard will likely include a more complicated curve equation that accepts both current and trace width as a parameter.

Note that the Y-axis is the total trace temperature. Because we are concerned with a maximum 20 degC rise, the Y-axis starts at 20 as the ambient temperature is also assumed to be 20 degC. The crossover point of 40 degC occurs when I=1.711A. Using this new data, Table 7 can be updated as shown in Table 9.

Table 9. Current-Carrying Capacity Extrapolated from Adams

Location	Copper Plating	A/11 mil trace	North (15x)	South (10x)	East/West (14x each)	Total
Outer	0.5 oz.	1.210 A	18.15 A	12.10 A	16.94 A	64.12 A
	1.0 oz.	1.711 A	25.67 A	17.11 A	23.95 A	90.68 A
	1.5 oz.	2.420 A	n/a			
	2.0 oz.	3.422 A				

Table 9. Current-Carrying Capacity Extrapolated from Adams (continued)

Location	Copper Plating	A/11 mil trace	North (15x)	South (10x)	East/West (14x each)	Total
Inner	0.5 oz.	1.149 A	17.24 A	11.49 A	16.09 A	60.92 A
	1.0 oz.	1.625 A	23.48 A	16.25 A	22.76 A	86.15 A
	1.5 oz.	2.299 A	n/a			
	2.0 oz.	3.251 A				

Clearly, with these results, the following power plane strategies work:

- 0.5 oz. copper area fill on an outer layer next to a solid plane providing 64.1A, max
- 0.5 oz. copper area fill on an inner layer next to a solid plane providing 60.9A, max

The IEEE paper included in the references explains why the classic IPC-275/IPC2221A values for inner current layers are extremely misleading. IPC-2152 is not published at the time of this application note.

5.3 Plane Resonance

The last factor to consider in a PDS design is the length of the power plane. If the distance from the output filtering capacitors of the switching power supply to the bulk capacitance of the processor is (empirically) more than 5 cm, or if the plane is circuitously routed, the plane needs additional high-frequency and bulk capacitance. Consider [Figure 13](#).

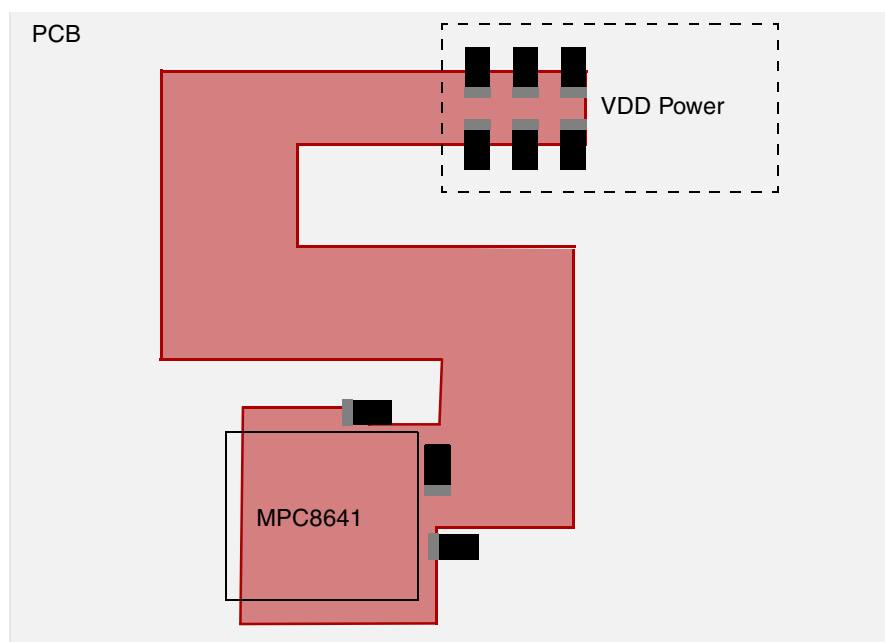


Figure 13. Poor Power Plane Layout

This plane appears to have sufficient capacity between the supply and the MPC8641, but the plane wanders about the PCB. Like any signal, voltage does not propagate instantly along a trace. Because neither the power supply nor the stored energy in the plane nor its capacitors can respond instantly to the high di/dt

demands of the processor, the plane resonates in a discharge/recharge cycle. A better plane route is shown by the dotted bold line in [Figure 14](#). If this route is not possible because of other design requirements, then adding bulk and bypass capacitors along the path helps eliminate resonance issues.

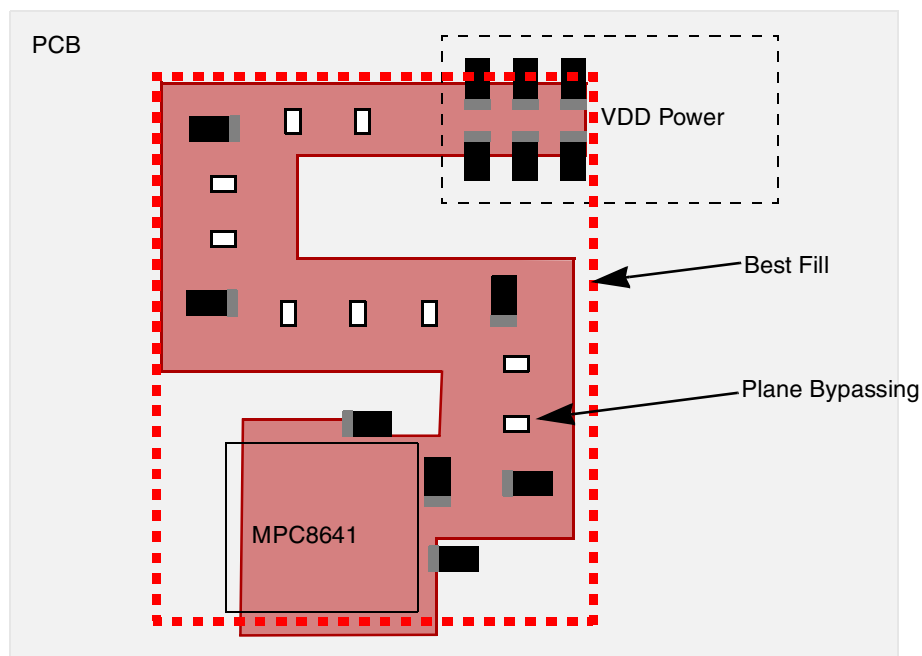


Figure 14. Improved Power Plane Layout

[Table 10](#) summarizes these design issues.

Table 10. Power Plane Resonance Treatments

Distance from PSU to CPU	Special Considerations
≤ 3cm	None, but it may be possible to eliminate the bulk capacitors because the output filtering capacitors of the power supply are equally effective.
≤ 5 cm	None
> 5 cm	Add 1 low-ESR bulk capacitor every 4 cm or when the plane makes right-angle turns. Add 1 low-ESR HF capacitor every 1 cm.

Note that these rules of thumb are voided by unusual layout (such as twisting paths or excessive vias), so general good design principles are still needed.

6 Summary

In this document, the goal is to determine the minimum width and area necessary to deliver a sufficient amount of power to the processor under various constraints. However, it is almost always desirable to use thicker copper plating and/or larger area plane fills whenever practical and possible because this reduces I-R losses between the power supply and the processor. Allowing the temperature of the power plane to rise by 50°C has a side effect of dissipating 2.4 W of power (assuming a plane length of 4 inches). Reducing the allowed temperature rise by increasing the plane width decreases wasted power. Therefore,

References

heavier and wider power planes are generally desirable both for energy efficiency and performance reasons. I conclude with the recommendations listed in [Table 11](#).

Table 11. VDD_CORE Plane Recommendations

Preference	Recommendation
Best	Use a single 1.0-oz. copper plane/area-fill for VDD_CORE on an outer layer routed over a 1.0-oz. copper ground plane (per current IPC standards).
Second	Use a single 1.0-oz. copper plane/area-fill for VDD_CORE on an inner layer routed over a 1.0-oz. copper ground plane (assuming proposed IPC revisions are acceptable).
Third	Use two 1.0-oz. copper plane/area-fills for VDD_CORE on an inner layer routed over two 1.0-oz. copper ground planes (each pair can be relatively isolated—for example, the PWR/GND pair on layers 2 and 3 and the PWR/GND pair on layers 10 and 11).

7 References

Many thanks to Joseph Muczynski, Principal Hardware Engineer of Performance Technologies and to Steve Kulbeck of IONDesign for their time and insight. [Table 12](#) lists useful resources for further reading.

Table 12. References

Document	Source
Freescale Semiconductor, <i>Power Supply Design for PowerPC™ Processors</i> (AN2747) Freescale Semiconductor	http://www.freescale.com/files/32bit/doc/app_note/AN2747.pdf
IPC Standards: IPC-D-275 IPC-2221A IPC-2152	www.ipc.org
<i>New Correlations Between Electrical Current and Temperature Rise in PCB Traces</i> Johannes Adam, Flomerics Ltd.	20th IEEE SEMI-THERM Symposium 0-7803-8363-X/04/\$20.00 ©2004 IEEE www.flomerics.com/flotherm/technical_papers/t341.pdf
<i>Current-Carrying Capacity</i> , Martin Tarr, University of Bolton	www.ami.ac.uk/courses/ami4817_dti/u02/pdf/meah0221.pdf
<i>Decoupling Capacitors, a Designer's Roadmap to Optimal Decoupling Networks for Integrated Circuits</i> (CSC240_MUCCIOLI) Freescale Semiconductor	Available through a Freescale representative
Argo Navis, ARGONAVISSCH (Argo Navis schematics)	TBD
Argo Navis, ARGONAVISDW (Argo Navis design workbook)	TBD
<i>3-V to 6-V Input, 3-A Output Synchronous-Buck PWM Switcher with Integrated FETs (SWIFT™)</i> (TPS54310) Texas Instruments	http://focus.ti.com/docs/prod/folders/print/tps54310-q1.html

Table 12. References (continued)

Document	Source
Interactive trace-width calculator	http://circuitcalculator.com/wordpress/2006/01/31/pcb-trace-width-calculator
<i>DC Line Resistance and Current Carrying Capacity</i> Merix Inc.	http://www.merix.com

8 Revision History

Table 13 provides a revision history for this application note.

Table 13. Document Revision History

Rev. Number	Date	Description
2	01/2010	In Table 4, "MPC8641 Unused Power Options," clarified that XVDD/SVDD are not permitted to be connected to ground.
1	01/2008	In rows 1 through 3 of Table 3, "MPC8641 Power Requirements," changed the voltage to "1.05 V or 1.1 V" and changed the Trade-Off Notes to "Use of lower voltages may limit core and/or platform/DDR speeds." Throughout, updated bibliographic references.
0	05/2007	Initial release.

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