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Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages

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INTRODUCTION

The purpose of this application note is to provide Freescale Semiconductor customers with a guideline for solder reflow mounting of high power RF transistors and integrated circuits in over-molded plastic (OMP) packages. This document will aid customers in developing an assembly process suitable for their design as well as their manufacturing operation. Each Power Amplifier (PA) design has its own unique performance requirements. Similarly, each manufacturing operation also has its own process capabilities. Therefore, each design and assembly may require some fine-tuning. The intent of this application note is to provide the information our customers need to establish the process that is most suitable for their design and compatible with their manufacturing operations.

When designing and manufacturing PA systems, electrical, thermal, quality, and reliability factors must be considered. Using the guidelines presented here, customers should be able to develop a manufacturable assembly process that can do the following:

- Create an interface that is thermally and electrically much more conductive than thermal grease between the device source contact and system ground.
- Provide a thermal ground that will conduct the dissipated heat efficiently from the high power RF device to the system sink.
- Develop a consistent electrical ground to provide a stable RF performance over the life of the PA.
- Obtain a high quality solder joint between the device leads and the solder pads on the printed circuit board (PCB) as well as between the heat spreader of the device and the carrier to ensure good field reliability.
- Maintain the package integrity during assembly as well as in field use.

Throughout this application note, certain terminology is used. Following are definitions of some of these terms.

TERMINOLOGY DEFINITIONS

- Base Transceiver Station (BTS) — A system making cellular communication possible in a given cell.
- Carrier — Can either be pallet or coin. This metal piece forms part of the thermal and electrical connection. The carrier is attached to the PCB.
- Coin — A carrier that is smaller than the PCB.
- Flange or Heat Spreader — The exposed metal, primarily copper, part of the OMP package. The die is attached to the top of the heat spreader, and the exposed plated bottom is soldered to the carrier.
- Heat Sink — The carrier that is typically attached to a finned heat sink. The heat sink forms the part of the thermal path that carries heat away from the device and to the cooling air.
- Integrated Metal Carrier (IMC) — A metal pallet that is bonded to the PCB.
- Over-Molded Plastic (OMP) packages — A package encapsulates the die and consists of a mold compound, wire bonds, leads, and the heat spreader.
- Pallet — A carrier that is slightly larger than the PCB.
- Power Amplifier (PA) — An electronic assembly module that takes in the input signal, amplifies the signal, and feeds it to the antenna.
- Power Device — An RF Power device, usually an Si-based LDMOS discrete device, a multi-stage IC device, or a GaAs or GaN device.
- Printed Circuit Board (PCB) — The electrical interconnection between the RF Power devices and other electrical devices that are part of a PA.

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BACKGROUND

Semiconductor devices were first manufactured using metal-ceramic headers in hermetic, metal-can packages. Over-molded plastic (OMP) packages manufactured using a transfer molding technique became available as the integrity of the die level passivation and the purity of the mold compounds improved. Freescale has provided low frequency power devices using exposed pad OMP packages for over 35 years. Many of these devices have been qualified to the highest quality standards in the commercial semiconductor industry; namely, automotive quality standards such as the Automotive Electronics Council (AEC) specifications for under the hood applications. In the mid-1990s, Freescale pioneered the introduction of high power OMP packaging technology in high frequency, high power applications. Later, we advanced this technology from discrete devices to multi-lead integrated circuit (IC) devices. Today, we offer RF Power transistors and IC devices in OMP packages that are capable of an RF output of over 100 Watts and a frequency range up to 3.8 GHz.

This document focuses on the process of soldering OMP packages. Until the early 1990s, the industry trend was to bolt down RF Power devices. In the mid-1990s, high power RF devices that could be soldered instead of bolted down became available. Soldering devices offers many advantages:

- The soldered interface provides better thermal performance as well as electrical grounding. This means that the high power devices have a lower junction temperature and better RF performance when mounted in a PA with a soldered interface.

- The reduction in junction temperature for all semiconductor devices results in an increase in a device's Mean-Time-To-Failure (MTTF). For Si-based devices, each 10°C to 20°C reduction in junction temperature typically results in a doubling of the MTTF.

- Solder reflow mounting of the RF power device can be integrated with the reflow of the remainder of the components of the PA.

As demand for OMP packages increased dramatically, extensive effort has been made to automate the assembly and test operations from piece part manufacturers to semiconductor assembly factories. The added benefit of automation in manufacturing RF Power devices is that much tighter tolerances are possible in OMP packages than were previously feasible in air cavity (AC) packages.

Freescale offers LDMOS RF Power transistors as well as RFIC devices that can be assembled into a PA using the following assembly methods:

- Bolt down or clamp of a high power RF device in the PA assembly

- Solder reflow of a high power RF device in the PA assembly

- Surface mounting of a high power RF device in the PA assembly

This application note focuses on the solder reflow assembly method in which the device source contact is soldered to a metal carrier and the leads are soldered to pads on the PCB. This assembly method is a slight modification from industry-standard surface mount assembly technology. In surface mount technology, the device leads are formed to provide all of the solder joints on the top surface of the PCB. In the solder reflow assembly process, the solder joint for the source contact is in a lower cavity, and the solder joint for the leads are on the top surface of the PCB. Figure 1 shows a typical device dropped through the opening in the PCB. The leads are soldered to the PCB, and the source contact or the heat spreader is soldered to a metal carrier. These devices are available in a variety of lead sizes, lead pitch, and number of leads (2 to 16 leads).
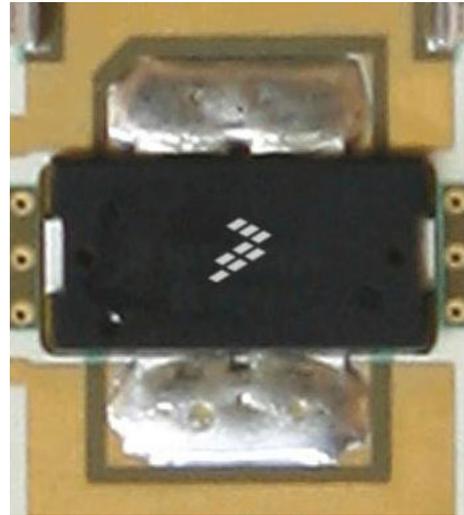
Figure 1. Typical Application of Freescale RF Power Device in Over-Molded Plastic Packages Soldered to a PCB as Well as to Carrier

The OMP package is designed for an RF Power device utilizing either silicon (LDMOS) or GaAs technology. The packaging technology is a conventional over-molded plastic process, commonly used in most semiconductor packages. The technology and material (such as lead frame, die attach, wire bond, and mold compounds) have been used in many applications and are known to provide robust semiconductor packages. These plastic packages are now used for power devices with a variety of frequencies in harsh environments with no reliability degradation. Figure 2 shows a typical over-molded plastic package device.


Figure 2. Typical RF Power Plastic Device Compatible for Solder Reflow Process (Case 1265, TO-270-2)

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The most commonly used OMP packages for RF Power devices designed for the solder reflow assembly method are the OM‑780 (Case 2021), TO‑270 (Case 1265) and the TO‑270WB (Cases 1486, 1618, and 1886). Other OMP packages designed for bolt down such as the TO‑272 (Cases 1264A and 1337) and the TO‑272WB (Cases 1329, 1484, and 1617) can also be assembled using the solder reflow assembly method. All electrical contact surfaces of these packages (e.g., TO‑272WB) are solderable with the same plating as used in packages designed purely for solder reflow (e.g., TO‑270WB).

PACKAGE CONSTRUCTION

As mentioned earlier, RF Power devices are manufactured in both AC and OMP packages. Figure 3 shows the schematic representing a typical cross‑section of an OMP package.
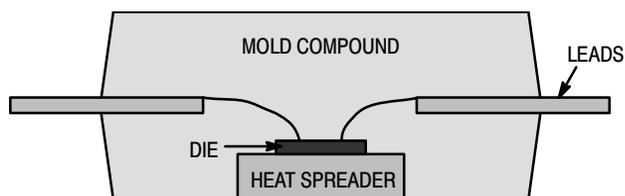
Figure 3. Over‑Molded Plastic Package Construction for Power Devices

In an OMP package, the Si die is typically attached to a Cu alloy heat spreader using high Pb‑based soft solder. The die and wire bonds are in direct contact with a mold compound. The lead finish is Matte Sn.

Both AC and OMP packages are RoHS compliant. Both are non‑hermetic packages. The key differences between the two package technologies are as follows.

- In AC packages, the Si die is typically attached to a CuW or other composite metal heat spreader using a AuSi‑based eutectic die attach. In OMP packages, the Si die is typically attached to a Cu alloy heat spreader using high Pb‑based soft solder.
- In AC packages, the die and wire bonds are surrounded by a low die‑electric constant material such as air (hence, the name). In OMP packages, the die and wire bonds are in direct contact with a higher die‑electric constant mold compound.

The case outline dimensions show that the tolerances for key features such as seating plane height (SPH) and lead coplanarity are significantly tighter for OMP packages than for AC packages. The tighter tolerances can also permit automation of the next‑level assembly, such as the assembly of the PA board. These tighter tolerances should reduce variability in RF performance.

CARRIER DESIGN CONSIDERATIONS

Figure 4 shows an example of a test board in which the PCB is bonded to a carrier with a cavity. In this particular case, the carrier is the same size as the PCB and is bonded to the PCB underside with an electrically conductive bond

layer. The carrier is an integral part of the system and has thermal and electrical functions. RF Power devices dissipate thermal energy that must be removed from the device through the back‑side of the device. The carrier is an important part of the thermal structure because it spreads the heat to a larger area while dissipating it to the ultimate sink. Also, the carrier provides an electrical ground connection for the device. (The PCB shown in Figure 4 is a test circuit, not a power amplifier. The test circuit is designed to accommodate both bolt down and solder reflow devices.)
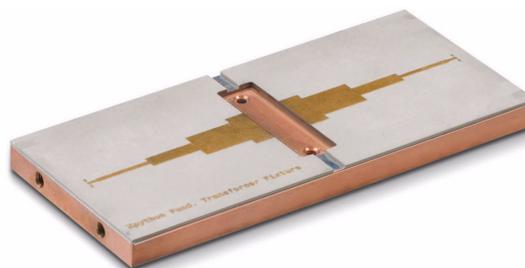
Figure 4. Example of Test PCB Bonded to Carrier with Cavity to Accommodate RF Power Device

Two types of special PCB carriers are used to dissipate heat from the power devices: the integrated metal carrier (IMC) pallet and the coin.
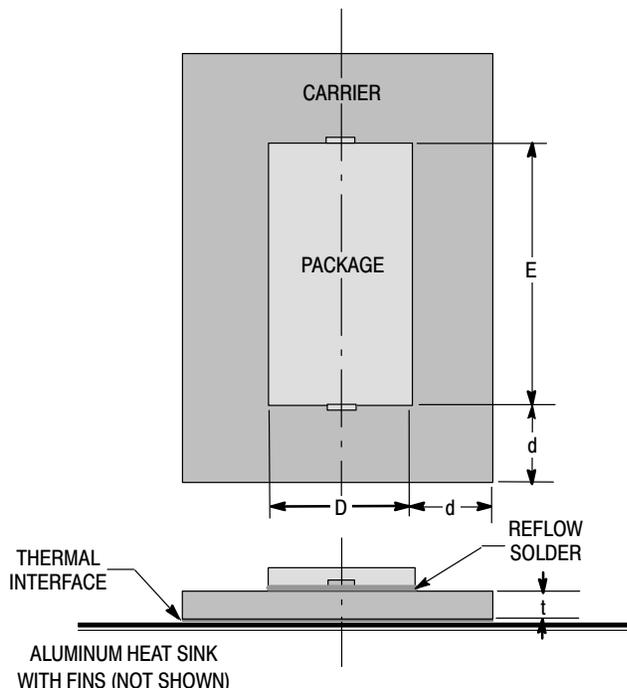
In one type of PCB assembly, the conventional PCB is attached to a carrier that is the same size or slightly larger than the PCB similar to the test circuit shown in Figure 4. This is known as an IMC or pallet. The metal carrier is made from mostly copper or aluminum material. The metal is plated to provide a solderable surface. A copper pallet is typically plated with Ni followed by Au. The Au thickness is fairly small and is commonly known as Au flash. The aluminum material is typically plated by a zincation process, followed by a Ni and Au flash layer. The purpose of the Au flash layer is to prevent the Ni from oxidizing and to keep it solderable. In addition to the plating layers mentioned previously, other plating materials used in the industry are also available (e.g., Ag). Vendors familiar with plating technology can provide alternatives and a cost benefit analysis of the plating schemes. The carrier in Figure 4 is unplated copper.

The second type of PCB assembly has a carrier of forged or machined metal coin that is also plated with Ni and Au. The coin is usually designed to be larger than the RF Power device but typically much smaller than the PCB. The coin should have sufficient perimeter area so it can be bonded to the ground plane of the PCB. Typically, the coin also has a bolt hole on each side of the RF Power device so it can be bolted to the PA module or a finned heat sink to provide good thermal and electrical grounding for the coin.

The choice between a coin and an IMC pallet is purely driven by cost. Typically, if the total footprint area of the RF Power devices is a significant portion of the PCB area, the IMC pallet is more cost‑effective. If the total footprint area of the RF Power devices is not a significant portion of the PCB area and if the coin size can be standardized, the coin is a cost‑effective solution.

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GEOMETRICAL DESIGN OF THE CARRIER

In a thermal pathway, the carrier is inserted between the RF Power device and the aluminum heat sink for thermal management as shown in Figure 5. A properly designed carrier can significantly improve the thermal performance of the system. Normally, the carrier is made of metals with high thermal conductivity such as copper alloys — C101, C102, or C151 — or aluminum.

With a metal carrier, two important dimensions affect thermal performance of the system: (a) thickness "t," and (b) extension "d" (shown in Figure 5). A parametric study was conducted using Finite Element Analysis (FEA) for various values of "t" and "d." A typical 100 Watt RF Power device in the TO-270WB package (Case 1486) was used as the vehicle for this evaluation. In the evaluation, the thickness value was varied between 0.125 mm to 5.0 mm, and the extension "d" was varied between 0.0 mm to 10.0 mm. The package foot-print is approximately 9 mm by 18 mm.

The evaluation was carried out for two different materials: copper (C102 alloy, conductivity 390W/m-K) and wrought aluminum (conductivity 206 W/m-K). The evaluation results in terms of normalized junction to heat sink thermal resistance with a copper carrier are shown in Figure 6. Similar results for an aluminum carrier are shown in Figure 7. In both cases, the thermal resistance between junction to heat sink is normalized by the value of the thermal resistance between junction and heat sink with no carrier ("t" = 0.0 mm). The normalized thermal resistance between junction to sink is plotted vs. carrier extension "d" for different thicknesses of copper (Figure 6) and aluminum (Figure 7) material. These figures are a guide for designing an effective carrier to reduce the total thermal resistance. A more detailed analysis for each specific design is highly recommended.

Figure 5. Typical Carrier Inserted Between Device and Aluminum Heat Sink
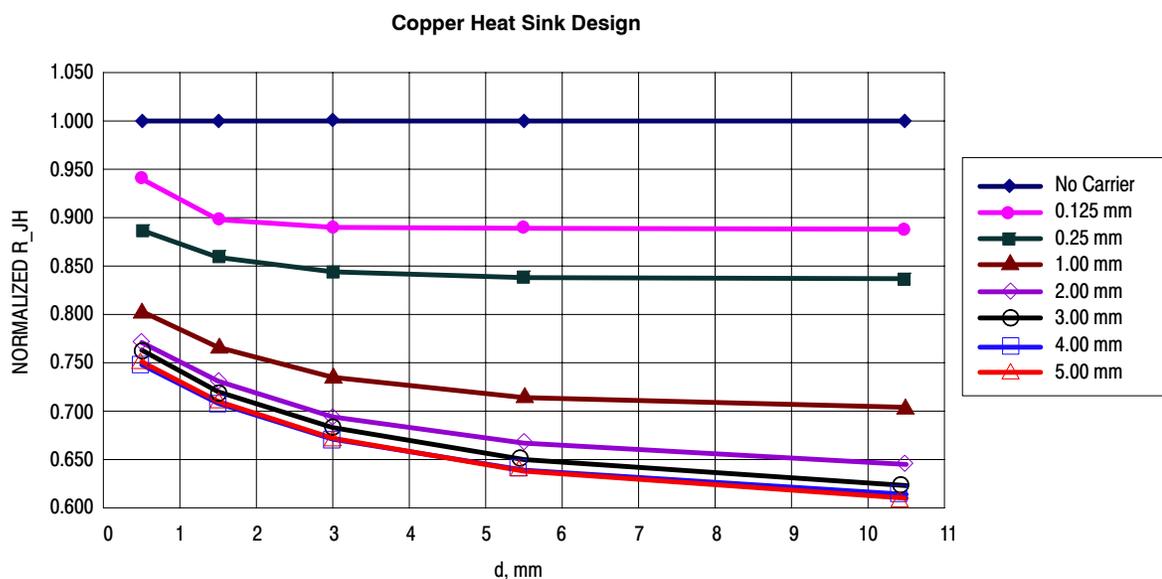
Figure 6. Parametric Study Results for Copper Carrier

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Aluminum Heat Sink Design
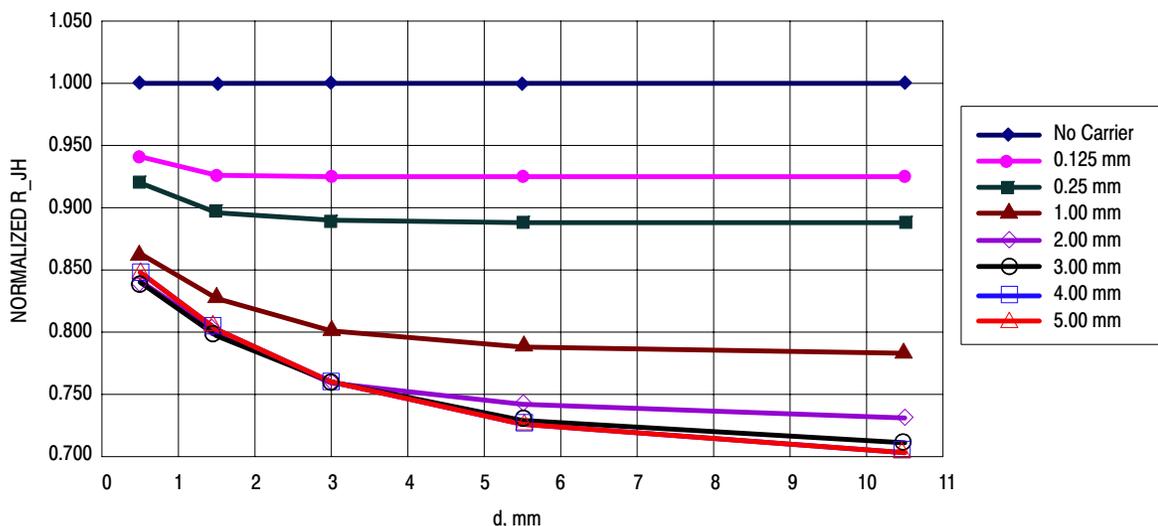
Figure 7. Parametric Study Results for Aluminum Carrier

From the analysis conducted for a 100 Watt RF Power device in a TO‑270WB package (Case 1486), we can state following:

- A copper carrier is more efficient in reducing the total thermal resistance between junction and sink. Aluminum carriers provide slightly less reduction in total system thermal resistance than copper carriers.

- For both copper and aluminum carriers, thickness "t" is recommended to be 3.0 mm minimum. As Figures 6 and 7 illustrate, the additional benefit in terms of thermal performance improvement becomes insignificant when the thickness of the carrier is increased above 3.0 mm for either copper or aluminum.

- The extension "d" of the carrier past the device width is recommended to be 5.5 mm minimum for both copper and aluminum. Increasing the size of the carrier on each side of the device greater than 5.5 mm show only slight improvement but not significant improvement.

Based on this analysis, we recommend using a copper carrier that is 3.0 mm thick and a minimum of 5.5 mm wider than the package footprint on all sides. Mechanical considerations, such as sufficient bond line width, etc., should also be included in the design of the carrier.

Besides the footprint of the carrier, the next most important dimension is the cavity depth or pedestal height. If the PCB thickness is less than the seating plane height of the RF Power device, the bottom surface of the RF Power device will be seated below the backside of the PCB. In such instances, the carrier must have a cavity that accommodates the protruding portion of the RF Power device. If the PCB thickness is larger than the device seating plane height, the carrier must have a pedestal that connects to the bottom of the RF Power device. In either instance, multiple components are combined to form an assembly so the stack‑up tolerance becomes a serious concern.

A simple analysis to determine the cavity depth is to use the worst‑case tolerance analysis and determine the optimum cavity depth. However, this approach is not very practical because it will result in the dimension of cavity depth with a much larger range than normally necessary. Also, the probability of all the extreme dimensions occurring simultaneously is extremely low.

A better approach is to determine the standard deviation of the protrusion using the square root of sum of the square method. This method gives a somewhat more realistic evaluation of dimensional tolerances. In performing this analysis, it is ideal to know the mean and standard deviation of the distribution of the critical dimensions, e.g., PCB thickness. If the actual distribution is not known, it is assumed that the dimension follows a normal distribution whose mean is at the nominal dimension and the tolerance band represents $\pm 3\sigma$ variation. The assumption that the tolerance band is six times the standard deviation is conservative, because it does not account for process shift. In real life, the tolerance band for a process is defined by process shift plus the standard deviation of the distribution. In order to have a good yield (>90%), the processes are controlled to provide a standard deviation, which is less than one‑third of the required tolerance. For example, if a given component dimension is specified as 0.1″ (2.54 mm) $\pm$0.003″ (0.076 mm), we will assume that the dimension is normally distributed with the mean at a nominal value of 0.1″ (2.54 mm) and a standard deviation of 0.001″ (0.025 mm). This method is illustrated in Figure 8 and Tables 1 and 2.

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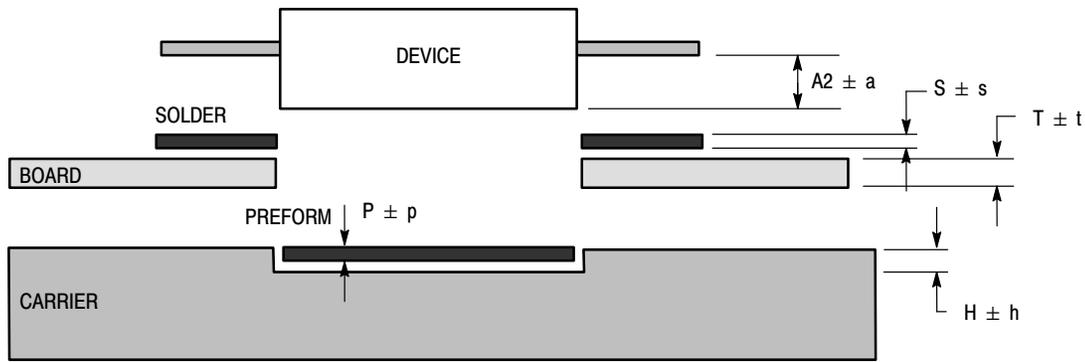
Figure 8. Exploded View Showing Criteria and Tolerances for Calculating Cavity Dimensions

Figure 8 shows that the cavity depth "H" for a complete balance system should be equal to device protrusion (T + S − A2 − P). This is possible if the assemblies are made one at a time and the cavity depth is customized for each assembly. For mass production, the distribution of "H" should overlap the distribution of (T + S − A2 − P). In the method here, we have selected a device in Case 1486 as an example. The nominal dimensions and tolerances are listed for key components.

Table 1. Dimensional Tolerances for Key Component Dimensions

Components	Dimension	Nominal	± Tolerance	Nominal	± Tolerance
		inch	inch	mm	mm
PCB	T	0.032	0.0030	0.81	0.076
Solder Joint (leads)	S	0.002	0.0010	0.05	0.025
RF Device	A2	0.041	0.0010	1.04	0.025
Solder Preform	P	0.002	0.0005	0.05	0.013
Cavity Depth	H	?	0.0010	?	0.025

A good way to perform this analysis is to create a spread sheet in which different options can be evaluated. Table 2 is an example of a spreadsheet which the dimensions in inches are taken from Table 1. In this example, the bond line thickness between the backside of the PCB and the carrier is assumed to be negligible. If it is a significant part of the stack-up, it can be added to the evaluation.

Table 2. Evaluation of Cavity Depth "H"

Components	Dimension	Nominal	± Tolerance	Minimum	Maximum	Std. Dev.
		inch	inch	inch	inch	inch
PCB	T	0.032	0.003	0.029	0.035	0.0010
Solder Joint (leads)	S	0.002	0.001	0.001	0.003	0.0003
RF Device	A2	0.041	0.001	0.040	0.042	0.0003
Solder Preform	P	0.002	0.0005	0.002	0.003	0.0002
Cavity Depth	H	???	0.001			
Protrusion (T + S – A2 – P)						
Worst Case		-0.009		-0.003	-0.015	
SRSS (3*σ)		-0.009		-0.006	-0.012	0.0011
SRSS (2*σ)		-0.009		-0.007	-0.011	0.0011
Cavity Depth Options (H)						
		0.006	0.001	0.005	0.007	
		0.007	0.001	0.006	0.008	
		0.008	0.001	0.007	0.009	
		0.009	0.001	0.008	0.010	
		0.010	0.001	0.009	0.011	
		0.011	0.001	0.010	0.012	
		0.012	0.001	0.011	0.013	

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From the example in Table 2, we can state that the device bottom will protrude below the backside of the PCB an average of 0.009″ (0.23 mm). The standard deviation for the distribution of the protrusion is 0.0011″ (0.028 mm). If we use a ±3σ spread, which will cover 99.7% of the population, the device will protrude anywhere between 0.006″ (0.14 mm) to 0.012″ (0.31 mm). If we use a ±2σ spread, which will cover 95.4% of the population, the device will protrude anywhere between 0.007″ (0.17 mm) to 0.011″ (0.29 mm).

We know that the machining tolerance for the cavity depth is ±0.001″ (0.025 mm). Thus, if the cavity depth is specified at 0.006″ (0.15 mm), the carrier will be produced with a cavity depth of anywhere between 0.005″ (0.13 mm) and 0.007″ (0.18 mm). Under these circumstances, a large number of assemblies will protrude much more than the cavity depth, resulting in solder flow out and a potential issue of solder bridging between the source contact and gate or drain side leads. On the other end, if the cavity depth is specified as 0.012″ (0.30 mm), a large number of assemblies will have no contact between the bottom of the device and the solder preform, leaving either a void or no solder wetting without bending the leads significantly. Our tolerance analysis reveals an obvious fact — the stack-up tolerances are being dominated by one or two components. In this example, the tolerance in the PCB thickness is dominating the stack-up analysis.

For this example, we recommend selecting a cavity depth specification of 0.010″ ± 0.001″ (0.25 mm ± 0.025 mm). In this case, the cavity distribution and the protrusion distribution overlap each other. In the worst case, the cavity depth would still not be too deep for the device to make contact with the solder preform. In the best case, the cavity depth would be close to nominal device protrusion. In the event that the PCB distribution is running toward the high end of the range, the variation can be adjusted by using two preforms instead one without changing the cavity dimensions. That kind of change can be accommodated by reprogramming the pick-and-place equipment rather than changing the hardware.

The purpose of the discussion here in selecting the cavity depth dimension is to highlight the importance of this dimension on the device performance. A cavity that is too deep will result in potential voiding in the solder joint at source contact. A cavity that is too shallow will result in solder flowing out and creating solder bridging. The customer is advised to examine their assemblies very carefully in determining the cavity depth or pedestal height dimension specification.

PC BOARD LAYOUT CONSIDERATION

For the soldered-down RF Power device, the leads must be soldered on the top surface of the PCB, and the heat spreader must be soldered to the carrier. This requires a slot, or opening, in the PCB through which the RF Power device protrudes. The case outline drawing shows the length and width dimensions at the bottom surface of the leads. The minimum dimensions (nominal minus milling or punching tolerance for the PCB) for the slot should be at least 0.002″ (0.05 mm) in the shorter dimension and 0.003″ (0.076 mm) in the longer dimension larger than the maximum dimension of the package.

For example, Case 1329 shows dimension "D" as the length of the package and dimension "E2" as the width of the package underside. The maximum value of "D" is listed as 0.932″ (23.67 mm); therefore, the minimum slot length should be 0.935″ (23.75 mm). Similarly, the maximum value of dimension "E2" is 0.350″ (8.89 mm), so the minimum slot width should be 0.352″ (8.94 mm). Normally, there is a corner radius in the slot based on the mill or router diameter. This radius value should also be considered when defining the size of the slot. The length dimension of the slot can be enlarged so that the corner radius will clear the body of the RF device. In general, for RF performance and for consistency, the slot width should not be much larger than the package body. In addition, there will be a corner radius at the bottom of the cavity in the carrier. This radius between the bottom of the cavity and the vertical wall is usually not very large and should not affect the slot dimension. It is important that this corner radius is considered in determining the slot dimension. If the corner radius is too large, it may require opening the cavity size but not increasing the PCB slot dimension due to RF performance considerations. Case outline drawings are available in the data sheet for each device.

The top surface of the PCB has solder pad areas for soldering the leads to the traces on the PCB. It is good manufacturing practice to pull back these metal traces from the edge of the slot. PCB manufacturers should provide a design rule on how far these metal traces should be pulled back. In the absence of a PCB design rule, Freescale recommends that the metal in the solder pad area should be at least 0.010″ or 0.25 mm from the edge of the slot. The outside edge of the solder pad should be longer than the outside tip of the leads by a minimum of 0.010″ (0.25 mm). Similarly, the design rules from the PCB supplier and the assembly process should be followed on the width direction in terms of how close the two adjacent pads of metal should be to define the pad width. In the absence of a PCB design rule, we recommend that the metal in the solder pad area should be at least 0.010″ (0.25 mm) wider than the lead width. For multi-lead IC devices (such as Case 1329), however, this may not be feasible due to the close proximity of some leads.

Another concern is the opening in the solder mask. The industry has two common practices: using a solder mask defined pad or using a copper defined pad. In the solder mask defined pad method, the solder mask overlaps the underlying metal pad, which is slightly larger than the solder mask opening. In the copper defined pad, the solder mask opening is slightly larger than the exposed metal pad. The type of solder mask opening used is entirely based on the PCB supplier's preference and the preference of the PA board assembly operation. In either case, we recommend that the design rules from the PCB suppliers as well as the assembly process should be followed for the solder mask opening. The dimensions given here are for solder mask defined pad. Typically, the difference between a solder mask opening and a copper pad is 0.003″ (0.076 mm) per side.

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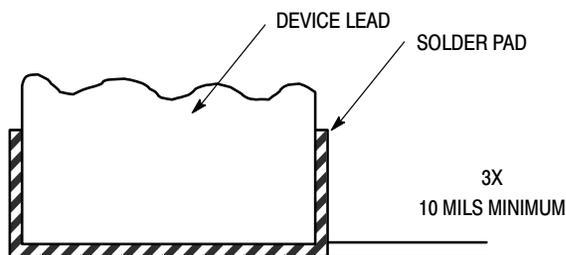
Figure 9. Pad Size for Gate and Drain Side Leads

The recommended solder pad dimensions as well as the slot dimensions for the case outlines of various plastic parts are shown in Appendix A. These dimensions are to be used as a guide and should be validated with the design rules from the PCB supplier as well as the assembly process. In case of conflict, the PCB supplier design rules should supersede the recommendations in Appendix A.
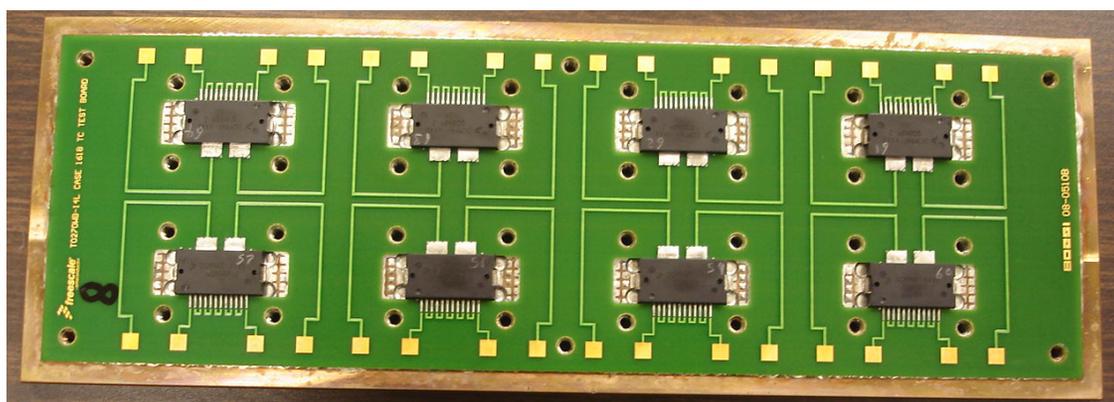
PCB TO CARRIER ATTACH

The coin and the pallet are both attached to the underside of the PCB using either a high temperature solder or a conductive adhesive such as Ag-filled epoxy. If solder is used to attach the coin or the pallet to the PCB before the component reflow, the solder selected must have a higher melting temperature than the solder used for the components on the PCB. Alternatively, the PCB and the carrier can be reflowed at the same time as the rest of the component using the same solder.

One method of attaching the PCB to the carrier is known as "sweat solder." Sweating is the attachment or bonding of two substrates using solder. Cleaned surfaces of the carrier are coated with solder paste containing no-clean flux. A PCB and a carrier with solder paste are exposed to solderable heat in a conduction furnace (large hot plate) and are sweated directly together. Typically, flux is used in the solder paste to provide surface activation and to remove surface oxide during soldering. The solvents from the paste evaporate before solder reflow. Alignment between the PCB and the carrier is usually achieved by inserting alignment pins into holes at multiple locations. A small amount of

pressure is evenly applied using a spring-loaded clamping device or a weighted object with sufficient pressure to keep both substrates in contact with each other during soldering and cool-down operations. The PCB/carrier assembly is heated above the solder melt temperature. The assembly is then cooled below the melt temperature of the solder, either by removing it from the heat or by lowering the heat while it is still under pressure.

The most common solder alloy used for sweat soldering is 95Sn5Sb with a liquidous temperature of 240°C. This alloy will typically require a sweat soldering temperature of 255°C, which is above the liquidous temperature. The liquidous temperature of this solder is well above the reflow temperature of SnPb eutectic alloy, but it is not higher than the reflow temperature used for Pb-free alloys. Very few solder alloys are available that have a liquidous temperature above the reflow temperature of the 260°C needed for Pb-free soldering.

An alternative method, particularly for Pb-free soldering, is to join the device, the PCB, and the carrier all in a one-pass solder operation. One pass refers to soldering the OMP package to the carrier and the PCB in the same heating cycle that joins the PCB to the carrier. Figure 10 shows an example of this process. In this example, Pb-free solder alloy SAC305 (Sn3.0Ag0.5Cu) was used for the bond layer between the PCB and the unplated copper carrier. The copper carrier was unplated and was cleaned with mild acid to remove the surface oxide just before assembly. This is possible for small quantity samples, but for a production run, the carrier must be protected from oxidation by plating, such as Au flash over Ni. In the assembly process, solder paste was printed on the carrier top surface after cleaning. In addition, the solder paste was screen-printed on the top side of the PCB using the proper stencil. The PCB was put on top of the carrier, and a few of the bolts were finger-tightened to hold the PCB and carrier together. After the PCB was aligned to the carrier, the devices were placed on top of the PCB with their leads aligning to the PCB solder pads. The whole assembly was then put through the reflow furnace to reflow both solder layers. The large mass of the copper carrier required a longer reflow furnace cycle. The reflow profile used to reflow the carrier is shown in Figure 11.
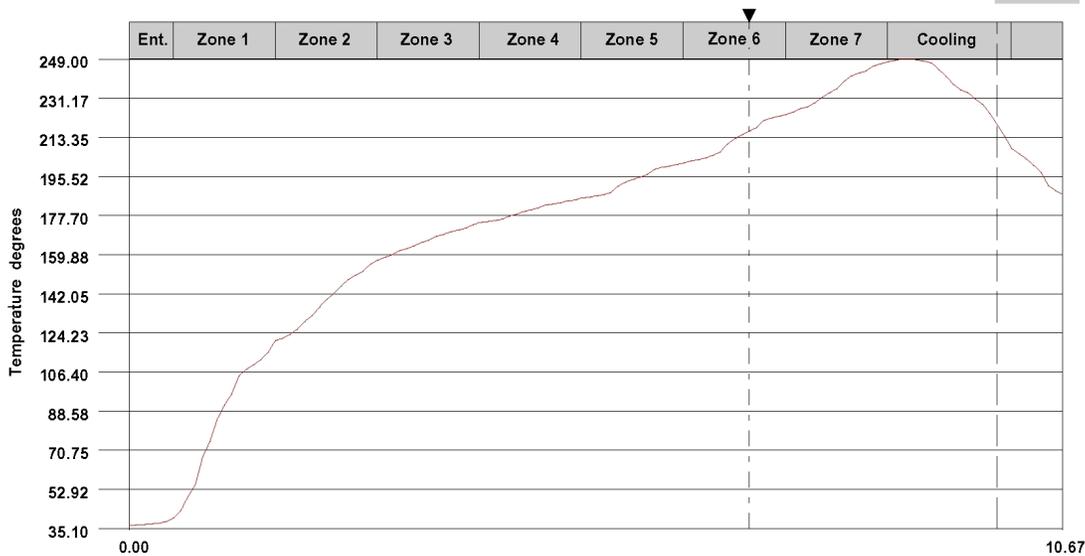

Figure 10. Example of One-Pass Soldering of PCB Device and Carrier

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Figure 11. Solder Reflow Profile for One‑Pass Pb‑Free (SnAgCu) Soldering of OMP Devices with PCB and Carrier Shown in Figure 10

Another alternative for bonding a metal carrier to the PCB is the use of conductive adhesive. Various conductive epoxy materials are available in paste form or in a B‑stage film. Conductive epoxies are typically filled with silver (Ag) particles or flakes. The film can be precut to a specific shape, which makes it highly suitable for use with coin. Paste can be screen‑printed on the pallet and is cheaper than film, but film provides a uniform bond line thickness compared to paste. A solder bond layer provides an electrically more conductive layer between the ground plane of the PCB and the carrier compared to epoxy film. In this process, the conductive epoxy paste or film is applied to the carrier. The carrier and the PCB are then aligned and held down by a small amount of pressure and heated to a cure temperature for certain duration. Each material has its own cure profile, but most epoxies are cured below 200°C. The cure profile recommended by the epoxy supplier should always be followed.

The cost of Ag‑filled epoxy is fairly high because of the use of a precious metal and because cutting precise shapes creates some waste of material. To reduce cost, a non‑conductive epoxy is substituted in place of conductive epoxy. When non‑conductive epoxy is used, alternative electrical connections are required between the PCB ground plane and the carrier. This is likely to affect the RF performance of the power amplifier. We do not recommend using non‑conductive epoxy without evaluating its impact on RF performance and stability of the PA.

SOLDER MATERIAL

RF devices are soldered to the land areas on the PCB and the carrier in one heating process. Solder is used for the electrical and thermal connection from the device to the carrier. Solder is available in preform and paste options. Freescale recommends solder preforms for the attachment of the device heat spreader (source contact) to the carrier in the carrier cavity and solder paste for the connections between the device leads and the PCB land area. The paste is made from solder material, binder, solvent, and flux. The preforms are pre‑cut solder foils typically provided with a coating of flux. The solder paste tends to create more voids in the solder joint than solder preform due to the presence of binders and solvents. For this reason, Freescale recommends using preform at the source contact. That solder joint is part of the prime heat dissipation path, and a reduction in void at that joint will result in lowering the total system thermal resistance.

Common solders used in the industry until recently were Sn‑Pb alloys. In the last few years, due to RoHS regulation from various government entities, many customers have been switching to Pb‑free solder alloys. The most common Pb‑free alloy used in such applications is SAC305 with a liquidous temperature of 221°C. When reflowed, the solder forms a metallurgical joint with Cu in the device as well as Ni or Cu from the carrier.

No-clean flux is recommended because it does not require a subsequent aqueous cleaning process. Fluxes that must be cleaned in a subsequent step can leave water residue in the cavity and under the PCB. Because high power RF devices are reflowed on the PCB with all other components, Freescale does not recommend that the PCB be washed to remove the flux. We recommend that solder paste with only no‑clean flux should be used.

Solder preforms are precut or stamped to precise shapes and delivered in a tape and reel for use in a pick‑and‑place system to populate the PCB. Solder paste is available in jars and is typically printed in a pattern to coincide with solder land areas on the PCB. The patterning is done using a stainless steel stencil. The stencil is typically laser‑cut to precise patterned openings which allow solder paste to pass through and deposit on the PCB in the same shape as the opening. Stencil thickness is defined by the pitch of the component leads. Typically, RF Power devices do not have a pitch that is as fine as some digital components on the PCB. The PCB in Figure 10 was screen‑printed with a 0.006″ (0.15 mm) thick laser‑cut stencil. When using solder paste, the binders and solvents evaporate during the reflow, and the finished solder joint is typically 45% to 55% of the printed volume. Solder preforms retain all of their volume during the reflow process.

PCB ASSEMBLY PROCESS

So far we have described how to design a carrier and its cavity or pedestal to accommodate the difference between the solder joint at the source contact and the solder joint between the gate and drain side leads and the PCB land areas. We have also described guidelines for the PCB layout as well as different alternatives for attaching a PCB to a carrier. The next step is to follow a standard surface mount process to dispense the solder pattern, pick‑and‑place the devices on a PCB, and reflow the entire assembly in a belt furnace. A typical solder reflow assembly process flow is shown in Figure 12. One key difference for this process from a surface mount assembly process is that the device source contact is soldered to a surface lower than the top of the PCB. Due to the lower surface level as well as the need to reduce void levels in the solder joint at the source contact, we recommend using solder preform instead of solder paste. The preforms are typically precut or stamped to the required size and delivered in tape and reel. They are usually dispensed using the pick‑and‑place equipment just before the RF Power device is placed in the PCB slot. Other than that, the process is very similar to the surface mount assembly process that is a very common assembly technique currently used in the electronics industry.
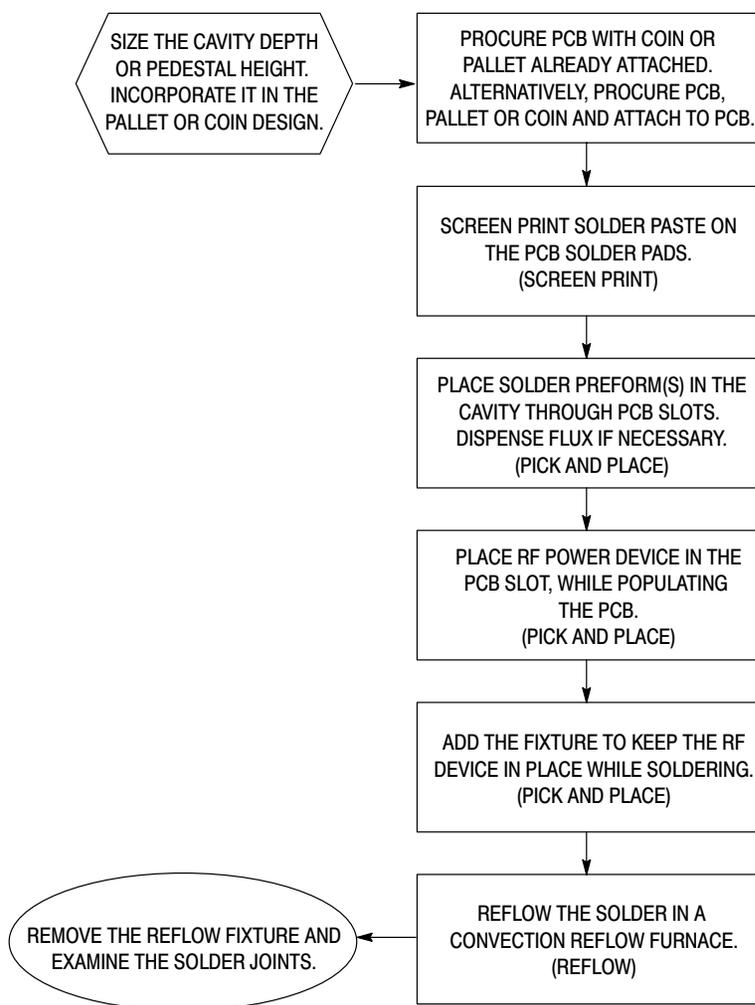
SIZE THE CAVITY DEPTH OR PEDESTAL HEIGHT. INCORPORATE IT IN THE PALLET OR COIN DESIGN. →

PROCURE PCB WITH COIN OR PALLET ALREADY ATTACHED. ALTERNATIVELY, PROCURE PCB, PALLET OR COIN AND ATTACH TO PCB.

↓

SCREEN PRINT SOLDER PASTE ON THE PCB SOLDER PADS. (SCREEN PRINT)

↓

PLACE SOLDER PREFORM(S) IN THE CAVITY THROUGH PCB SLOTS. DISPENSE FLUX IF NECESSARY. (PICK AND PLACE)

↓

PLACE RF POWER DEVICE IN THE PCB SLOT, WHILE POPULATING THE PCB. (PICK AND PLACE)

↓

ADD THE FIXTURE TO KEEP THE RF DEVICE IN PLACE WHILE SOLDERING. (PICK AND PLACE)

↓

REFLOW THE SOLDER IN A CONVECTION REFLOW FURNACE. (REFLOW)

← REMOVE THE REFLOW FIXTURE AND EXAMINE THE SOLDER JOINTS.

Figure 12. Typical Process Flow for Assembly of PCB using Solder Reflow Method

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As with all surface mount plastic packages, care must be taken in terms of storage and handling of the devices. Freescale typically qualifies the OMP packaged devices to Moisture Sensitivity Level (MSL) 3 at 260°C reflow temperature. The MSL criteria is defined in IPC/JEDEC Joint Industry Standard J‑STD‑020D.1, March 2008. Devices rated below MSL 1 are delivered in a vacuum pack. The storage, handling, packing, and use of OMP packages should be according to the requirement of IPC/JEDEC Joint Industry Standard J‑STD‑33B.1. We strongly recommend using the storage, floor life, re‑baking requirements, etc., as specified by this standard. These JEDEC standards are available for download at www.Jedec.org.

Freescale uses the JEDEC‑specified solder profile in qualifying its devices. The JEDEC criteria is shown in Table 3.

Table 3. JEDEC J‑STD‑020D.1 Solder Reflow Profile Requirements

Profile Feature	Pb‑free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	150°C 200°C 60‑120 seconds
Ramp‑up rate (T_L to T_p)	3°C/second max
Liquidous temperature (T_L) Time (t_L) maintained above T_L	217°C 60‑150 seconds
Peak package body temperature (T_p)	< 260°C
Time (t_p)* within 5°C of the specified classification temperature (T_c)	30* seconds
Ramp‑down rate (T_p to T_L)	6°C/second max
Time 25°C to peak temperature	
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.	

Typically, the solder supplier will provide a recommended profile for use with their paste and preforms. A specific profile used for the assembly will depend on the reflow furnace capabilities and the thermal mass going through the furnace. Freescale RF Power devices are qualified to survive three reflows that meet the criteria shown in Table 3.

For production use, most common reflow ovens are often convection or conduction types. In convection ovens, the boards with carriers are often put in boats, or holders, and sent on a moving belt though the oven. The convection oven has different zones in which the air or nitrogen‑rich gas is heated independently. This results in a controlled profile of specific temperatures that the PCB experiences for specific times. Examples of these profiles are shown in Figures 11 and 13. In a conduction oven, the heat transfer occurs by conducted heat from the platen in the oven to the substrate on which the PCB and carrier sit. The method of heating is therefore not from heated air or gases, but from the direct heat transfer from the bottom of the carriers to the PCB. Instead of a conveyor belt, sweeper mechanisms move the substrate from zone to zone, creating a temperature profile.

Other types of heating, such as IR furnaces or vapor phase reflow, are not appropriate methods for this product. Vacuum furnaces may be used in laboratory situations but are not suitable for production volumes.

In all cases, the profile must be optimized for the specific PCB assemblies based on parameters such as total thermal mass going through the furnace, furnace capabilities, temperature restrictions for key components, and size of the PCB. At the beginning of the assembly operation, the system is characterized with dummy units going through the reflow operation. Thermocouples are attached to the dummy units at critical solder joint locations. All thermocouple profiles are monitored to determine optimum process parameters, such as the temperature of each individual zone and the belt speed. Figures 11 and 13 show typical profiles that show temperature vs. time plot at a given location on the PCBs. It also identifies parameters such as different zones of the furnace, temperature in the zones and the peak reflow temperature, total time, belt speed, and time at critical temperature (e.g., time above solder melting temperature).

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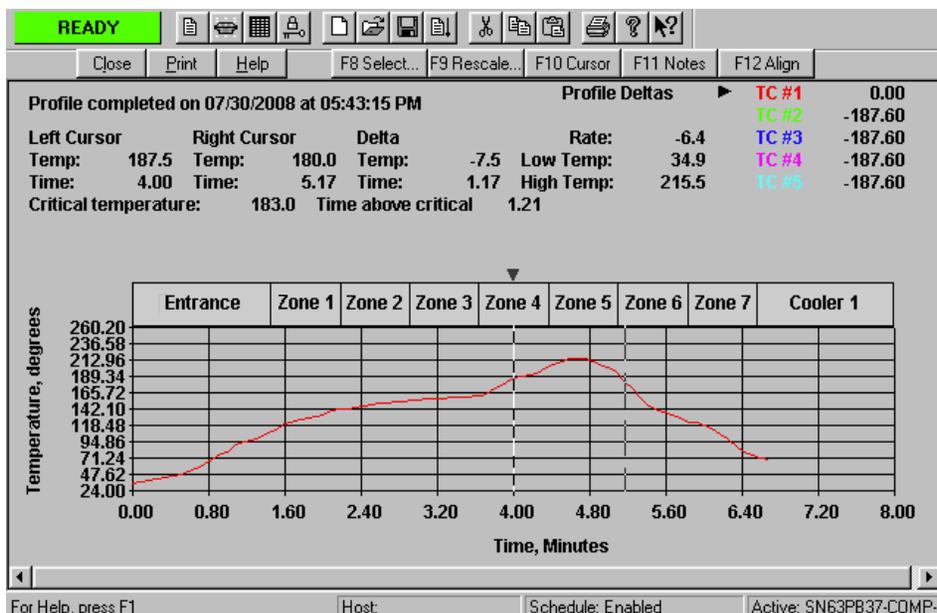
Figure 13. Typical Solder Reflow Profile for Eutectic SnPb Solder

For the solder reflow process, a fixture is usually needed to (a) keep the device in place while running though the reflow furnace, (b) prevent the device from lifting off due to buoyancy forces when the solder melts, and (c) keep the leads in contact with the solder paste so it forms a good solder joint. The amount of force needed depends on the amount and type of solder used and the soldering process. An experiment was designed to examine the effects of downward force on solder quality. The heat spreaders of TO‑272WB‑4 packages were soldered to a copper plate. Two types (eutectic 63/37 Sn/Pb solder and SAC305 solder) of 0.004″ (0.10 mm) thick solder preforms were used for the solder layer. No‑clean flux was applied to the heat spreader and the copper plate. The parts were reflowed in a convection oven to the profiles shown in Figure 13 for SnPb and Figure 11 for Pb‑free solders. In the design matrix, four different values of weights (0, 2.5, 5.0, and 10 grams) in addition to self‑weight were chosen. Based on the voiding observed and the solder flow outside the package footprint, it was determined that 2.5 grams of weight above the self‑weight of the component provided the best solder joint. The voiding was minimal at self‑weight plus 2.5 grams of weight. With just the self‑weight alone, the void distribution was higher. Increasing the weight caused more solder flow out as well as more voids.

In general, Freescale recommends a slight downward force equivalent to 2.5 grams of weight on a TO‑270WB package to increase solder joint quality. Adding weight on top of the device is possible and can be accomplished within the pick‑and‑place operation. One problem with using weight alone is that it may move during the reflow process. Instead, a clip can be used to hold the part in place as well as to apply slight downward force. One typical clip design is shown in Figure 14. This type of clip is much simpler than the cumbersome structure shown in the previous version of this Application Note.

It is important to ensure that any force applied does not flex or bend the leads more than 0.015″ (0.38 mm) from their received nominal position. Excessive bending of the leads can result in mechanical failure of the device.
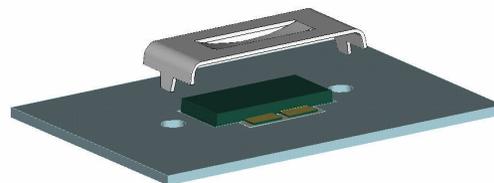
Figure 14. Typical Fixture or Clips for use During Solder Reflow

SOLDER JOINT INSPECTION

Inspection of the solder joint in the cavity between the package flange and the heat sink cannot be accomplished by a simple optical inspection. Two methods have been assessed for investigating this joint. Both X‑ray transmission and scanning acoustical microscopy look through the carrier to image the solder attach layer.

Transmission X‑ray has been recently demonstrated to show voids of less than 10 mils through up to 0.25″ (6.0 mm) thick copper. Figure 15 demonstrates a typical X‑ray image of solder voiding. In this demonstration, a T0‑272WB‑4 was mounted on a 0.210″ (5.33 mm) thick copper plate using purposely voided eutectic SnPb solder. The assembly was analyzed using an Insight‑130™ X‑ray system from FocalSpot, Inc. This system used 130 KeV at 123 mA with an input detector image intensifier to a 10X magnification level. X‑ray is a viable tool because it can be done in air. Many of the larger X‑ray systems can accommodate PCBs up to 20″ × 24″.

X‑ray inspection does have some drawbacks. Because the X‑rays are transmitted through the piece, all artifacts in the path of the X‑rays are captured. Any die attach voids or other artifacts will be captured and subject to interpretation. Also, an X‑ray image of a void‑free solder is very difficult to

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interpret. Even state-of-the-art X-ray equipment cannot penetrate thicknesses greater than 0.25″ (6.0 mm).

Scanning acoustical microscopy has been used to identify voids in the solder layer through a Cu heat sink up to 0.25″ thick. A main drawback to this method is that it uses water to transmit the energy. The introduction of finished PCBs into a water bath is considered a substantial field risk. Acoustic microscopy also has the same limitations in terms of the thickness they can penetrate as X-ray. Freescale does not recommend use of this method to determine the quality of solder joint on devices that are going to be deployed in the field. Acoustic microscopy is only recommended for destructive analysis of PA PCBs.
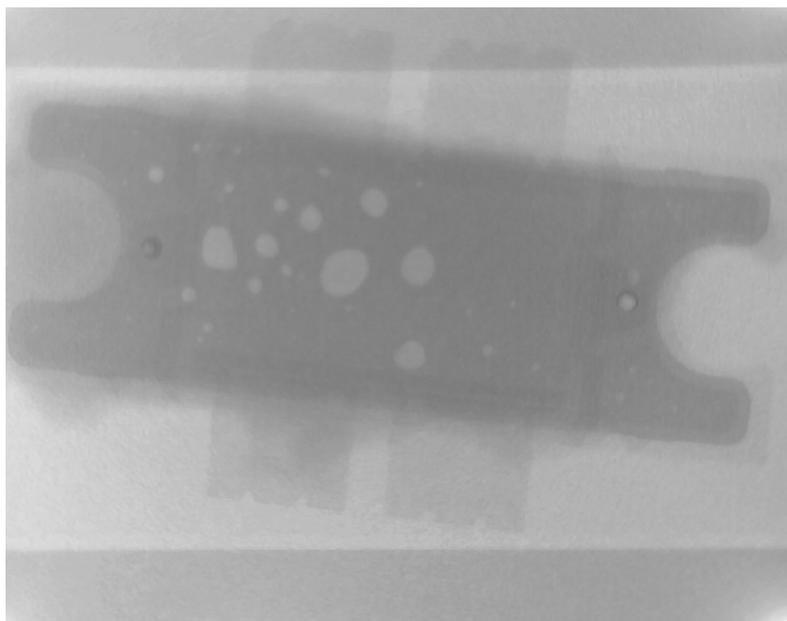
Figure 15. X-Ray Image Showing Voids in Solder Attach for TO-272WB-4 Mounted on 0.210″ (5.33 mm) Thick Copper Plate. (The image was taken on a FocalSpot, Inc. system. Used with permission.)

RELIABILITY OF THE SOLDER JOINT

To determine the quality of the solder joint created using the process described in this application note, a test PCB was created in which the gate and drain side leads were connected to create a daisy chain. Figure 16 shows the close-up view of one of the eight units on the PCB. In the device, the drain side leads were already internally connected at the lead frame post area. A dummy die was used in the device, and the adjacent leads were wire bonded to the same pad on the die, creating a short circuit between the two adjacent leads. Pins 1 and 2 (from left) on the gate side were shorted internally, while pins 2 and 3 were shorted externally at the PCB level. This continues through the extreme right lead (pin 12). Pins 1 and 2, 3 and 4, 5 and 6, 7 and 8, 9 and 10, and 11 and 12 were shorted internally by wire bonds. Pins 2 and 3, 4 and 5, 6 and 7, 8 and 9, and 10 and 11 were shorted externally when the device was soldered to the PCB. Both ends were connected to the trace and corresponding probe pads. As described earlier, the PCB was bonded to the copper carrier, and the devices were soldered to the PCB in a one-step process using SAC305 Pb-free solder alloy.
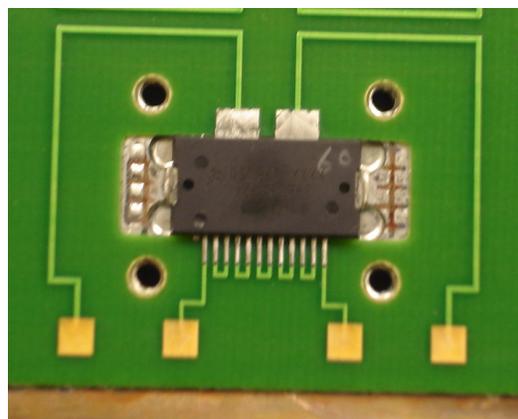
Figure 16. Close-Up View of one of the Daisy-Chained Devices Soldered to a Copper Carrier and the PCB

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After assembly, the devices were examined visually, and the solder joint resistance was measured using a four‑point Kelvin probe connected to an HP 3478A multimeter system. After the resistance was recorded, the carrier with the PCB and eight devices soldered to the PCB and carrier were put through temperature cycling. The temperature cycles were conducted with extreme temperatures of 125°C and ‑40°C. The dwell time at each temperature extreme was 15 minutes. This assures a minimum 10 minutes at temperature and less than 5 minutes for temperature transition. If one of the solder joints were to fail partially, the resistance would increase. If the solder joint were to fail completely, it would create an open circuit. The temperature cycling was continued for 1,000 cycles. Figure 17 shows the electrical resistance data in ohms at 0 cycle, 500 cycles, and 1,000 cycles. This figure shows no significant change in the electrical resistance from 0 cycle to 1,000 cycles, indicating that the solder joints are electrically intact. There may be small cracks, if any, but there was no effect on the electrical resistance measurement of the solder joint. The electrical resistance measurements for 16 devices under test were plotted as a box‑and‑whisker plot (Figure 17). In this type of plot, the box represents the 25th percentile and 75th percentile of the data. The whisker portion extends to a maximum of 1.5 times the height of the box on each side or to the most extreme data point. The shift in the value of the electrical resistance is no more than 1 milli‑ohm (less than 0.3%) from the initial cycle to post‑1,000 cycles. This value is smaller than gage repeatability and reproducibility for the measurement system.
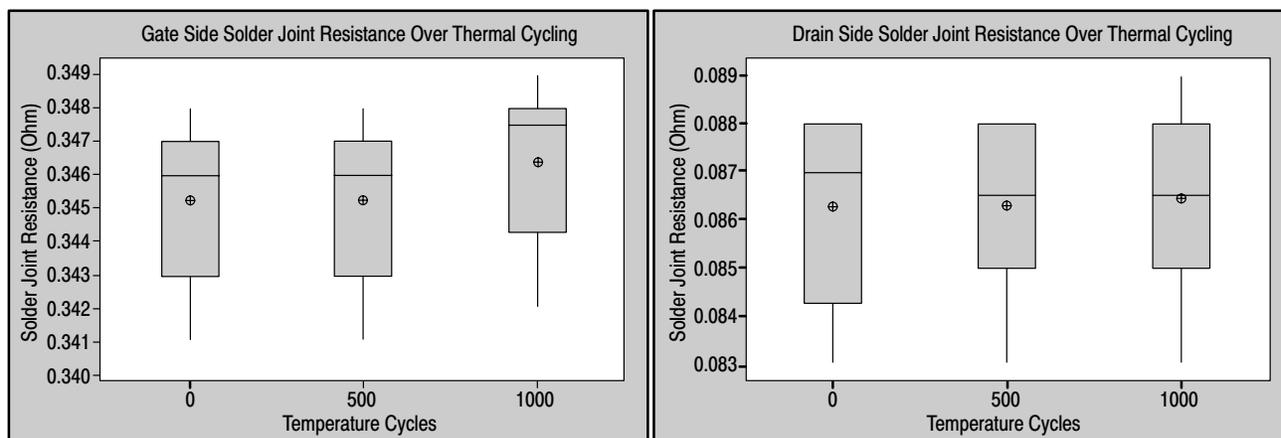
Figure 17. Box‑and‑Whisker Plot of Electrical Resistance of Gate Side and Drain Side Daisy Chain Circuit Indicating no Shift in Resistance or Solder Joint Cracking

SUMMARY

This application note provides the information needed to develop a robust assembly process for mounting RF Power devices in over‑molded plastic packages in customer PA applications by soldering to PCBs and carriers. Consideration was given to factors such as materials selection, mechanical design parameters, assembly methodologies, and inspection tools. Successfully integrating the guidelines provided here can lead to an assembly process that can yield:

- A reliable solder joint at the source contact to provide low thermal resistance for the system.

- A low source impedance to provide stable RF performance.

- A reliable solder joint at the leads that will withstand extensive thermal cycling in field use.

- A cost‑effective automated assembly process that will provide superior thermal and electrical performance even though the initial bill of material cost may be higher.

- Controlling design factors such as PCB tolerances and pad layout can minimize impact on solder joint reliability and placement interaction between the package, the PCB, and the carrier. Material selection and assembly process choices lead to high quality and reliable solder joints, which results in a lower‑cost system level solution and improved performance for the PA assembly.

Appendix A. PCB Layout Recommendations
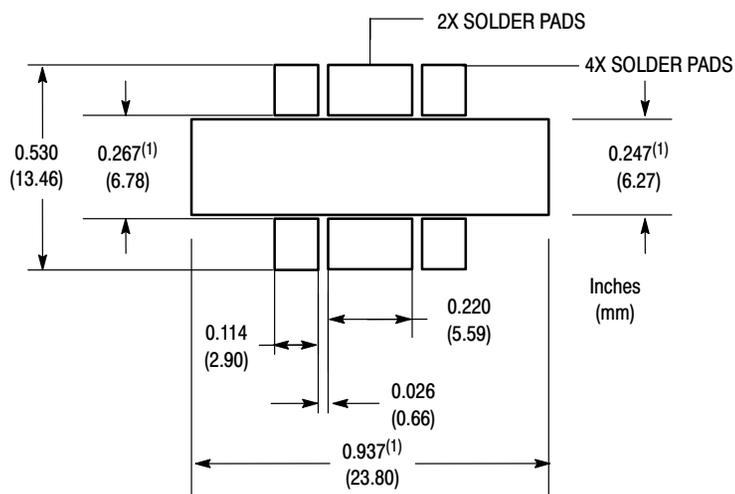
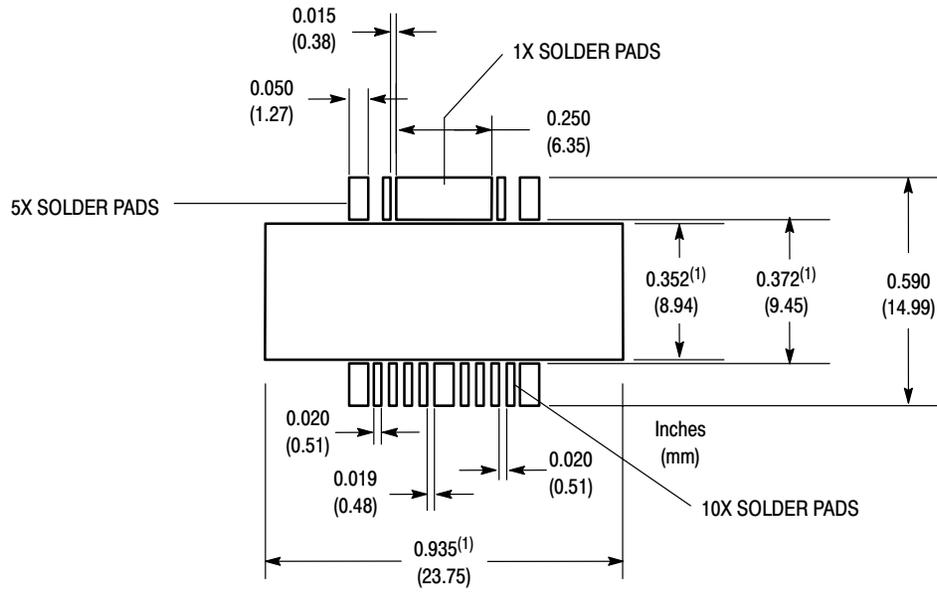1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A‑1. Case 1264A (TO‑272‑6)
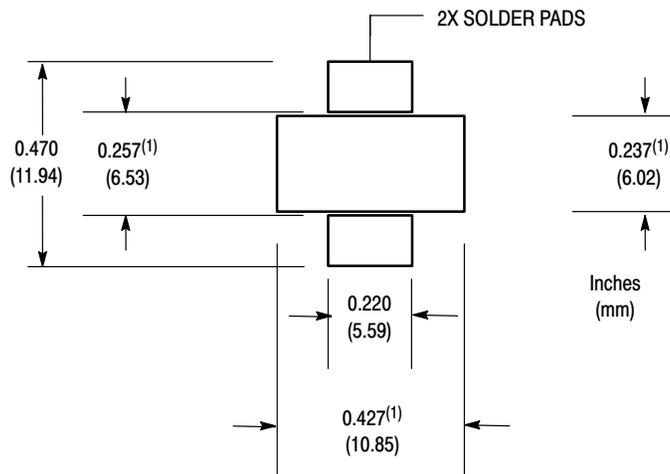
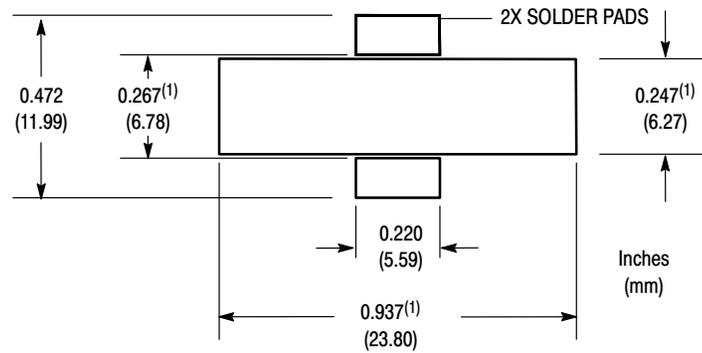1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A‑2. Case 1265 (TO‑270‑2)

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Appendix A. PCB Layout Recommendations (continued)

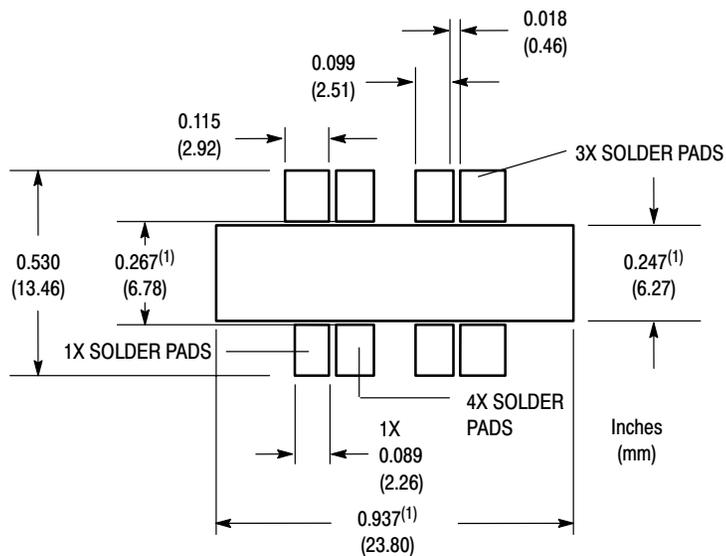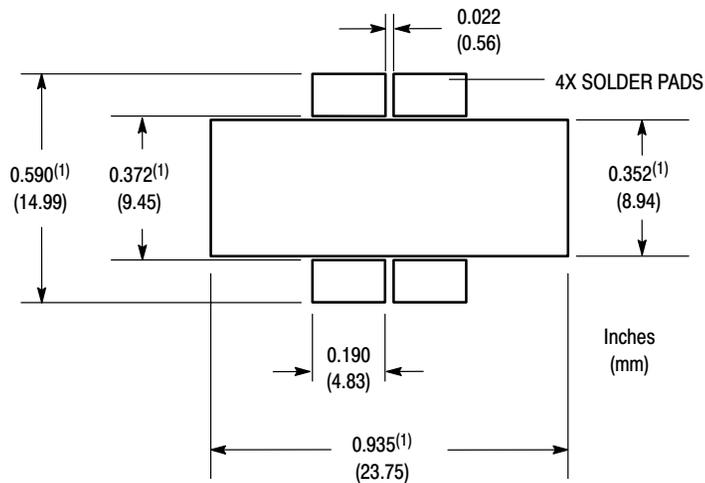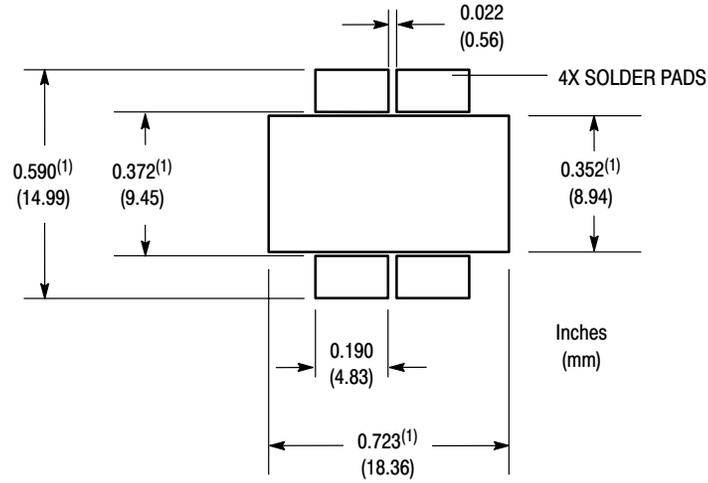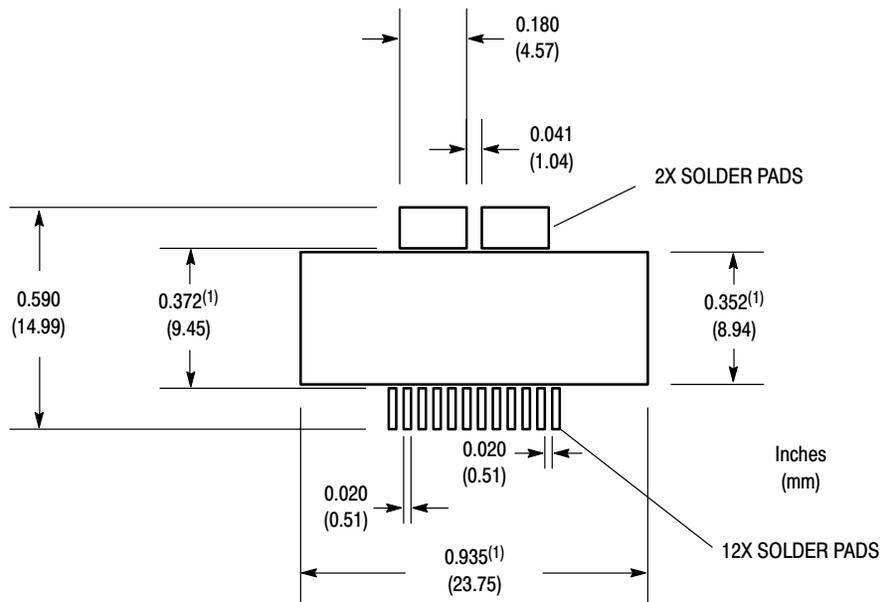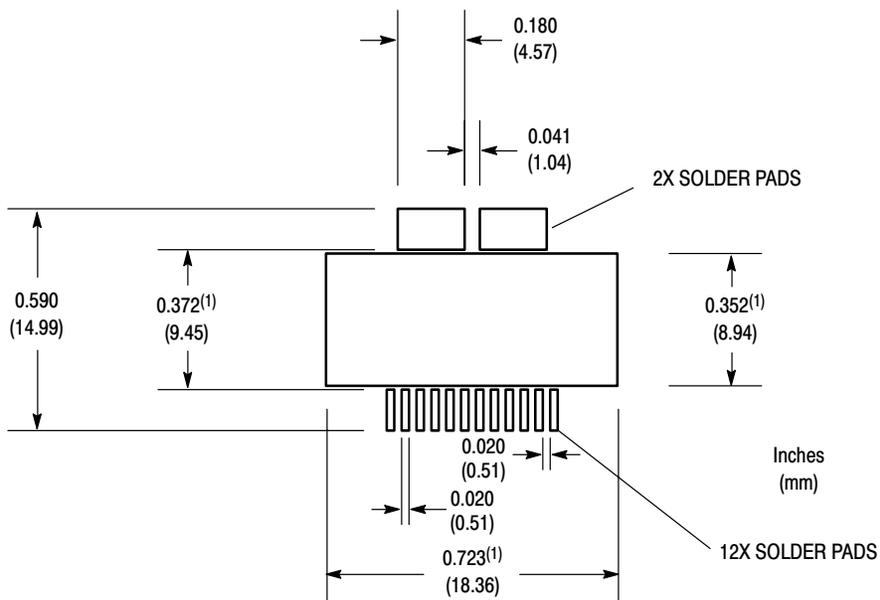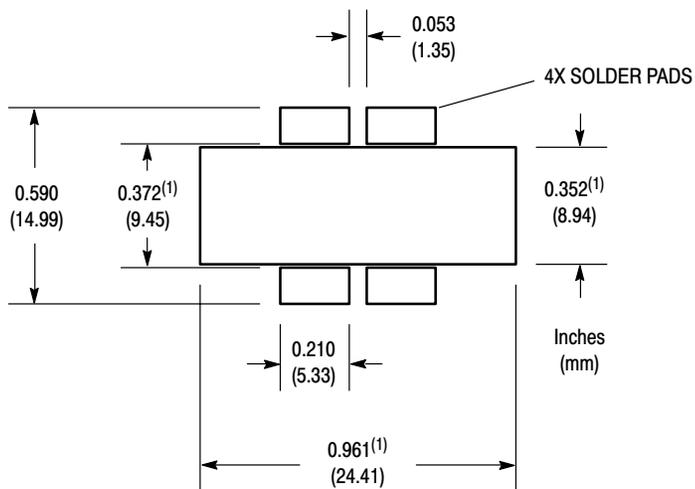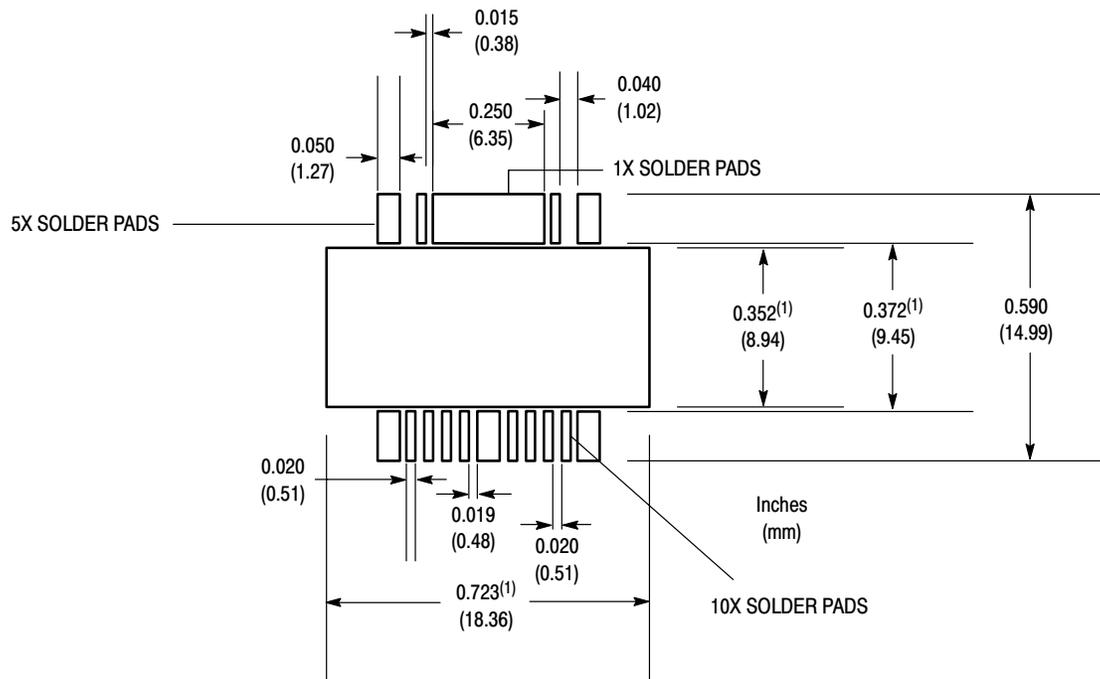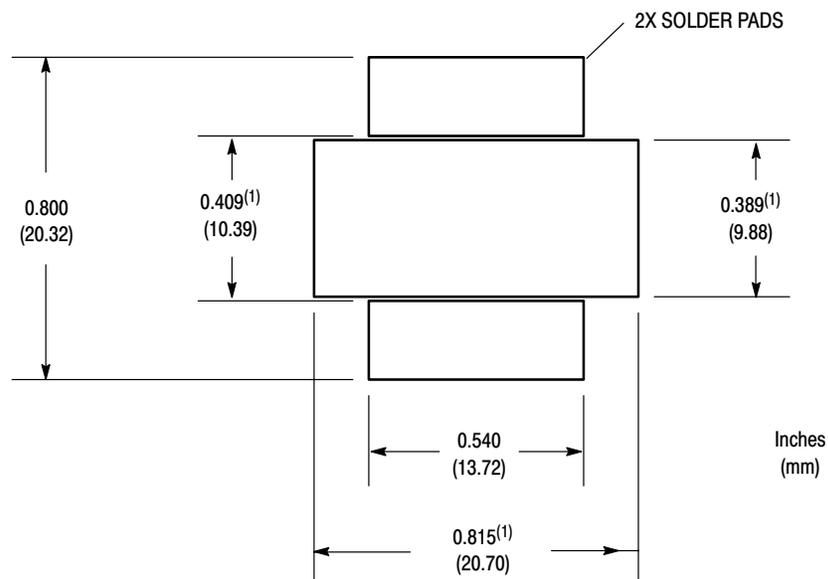1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A-3. Case 1329 (TO-272 WB-16)

1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A-4. Case 1337 (TO-272-2)

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1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A‑5. Case 1366A (TO‑272‑8)

1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A‑6. Case 1484 (TO‑272 WB‑4)

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Appendix A. PCB Layout Recommendations (continued)

0.022
(0.56)

4X SOLDER PADS

0.590[1]
(14.99)

0.372[1]
(9.45)

0.352[1]
(8.94)

0.190
(4.83)

Inches
(mm)

0.723[1]
(18.36)

1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A‑7. Case 1486 (TO‑270 WB‑4)

0.180
(4.57)

0.041
(1.04)

2X SOLDER PADS

0.590
(14.99)

0.372[1]
(9.45)

0.352[1]
(8.94)

0.020
(0.51)

0.020
(0.51)

Inches
(mm)

12X SOLDER PADS

0.935[1]
(23.75)

1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A‑8. Case 1617 (TO‑272 WB‑14)

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1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A‑9. Case 1618 (TO‑270 WB‑14)

1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A‑10. Case 1730 (TO‑270 WBL‑4)

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Appendix A. PCB Layout Recommendations (continued)

0.015 (0.38)

0.040 (1.02)

0.250 (6.35)

0.050 (1.27)

1X SOLDER PADS

5X SOLDER PADS

0.352[1] (8.94)

0.372[1] (9.45)

0.590 (14.99)

0.020 (0.51)

0.019 (0.48)

0.020 (0.51)

Inches (mm)

0.723[1] (18.36)

10X SOLDER PADS

1. Slot dimensions are minimum dimensions and exclude milling tolerances.

Figure A-11. Case 1886 (TO-270 WB-16)

2X SOLDER PADS

0.800 (20.32)

0.409[1] (10.39)

0.389[1] (9.88)

0.540 (13.72)

Inches (mm)

0.815[1] (20.70)

1. Slot dimensions are minimum dimensions and exclude milling tolerances

Figure A-12. Case 2021 (OM-780-2)

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