AN13950

TDA80xx EMVCo related measurements and calculations

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Document Information

Information	Content
Keywords	TDA8035, TDA8034, EMVCo, Low-Frequency-Oscillator
Abstract	Measuring the internal low-frequency-oscillator of the TDA8034/35 and calculating the frequency of it. With the measured frequency the RSTIN timing for the activation procedure can be adjusted.

Revision history

Revision history

Rev	Date	Description
v.1.0	20230523	Initial version.

1 Introduction

Due to changes in the EMVCo test specification [1] which is ultimately tightening the window for pulling RST high. EMVCo compliancy fails on TDA8034 and TDA8035 could be observed.

This document describes:

- the changed EMVCo requirements and the impact of it
- the actual situation of the current TDA products and why some might fail in EMVCo reset cases
- and how to overcome this issue

1.1 EMVCo requirements

The current EMVCo specification 4.3d ([1]), and later, enhanced the minimum clock frequency from 3.1 MHz to 4.7 MHz. The maximum clock frequency remains on 5 MHz.

The acceptance criteria for RST is following, where t_1 refers to CLK applied and t_2 to RST high:

Acceptance criteria

The following acceptance criteria shall be met under all environmental and test conditions:

1. The time between t_1 and t_2 is between 40'000 and 45'000 clock cycles.
2. Each sequence of commands and answers is performed correctly.

Figure 1. EMVCo acceptance criteria

This results in a tighter window for pulling RST high in the activation, or reset procedure.

Before:

- Max: Every clock cycle is 1/3.1M - 45.000 clock cycles are **14.516 ms** (45.000/3.1M)
- Min: Every clock cycle is 1/5M - 40.000 clock cycles are equal to **8 ms** (40.000/5M)

Now:

- Max: Every clock cycle is 1/4.7M - 45.000 clock cycles are equal to **9.574 ms** (45.000/4.7M)
- Min: Every clock cycle is 1/5M - 40.000 clock cycles are equal to **8 ms** (40.000/5M)

1.2 Actual situation

Due to the frequency spread of the internal low-frequency-oscillator, the EMVCo requirement might not be met, if the actual running frequency of the oscillator is too low or high.

The host MCU is in control of CMDVCC and RST, but the CLK signal is controlled by the TDA and unknown to the MCU. EMVCo requires that after 40.000 to 45.000 clock cycles RST is pulled high. When CLK is started depends on the internal low-frequency-oscillator, but the actual clock frequency is unknown to the MCU.

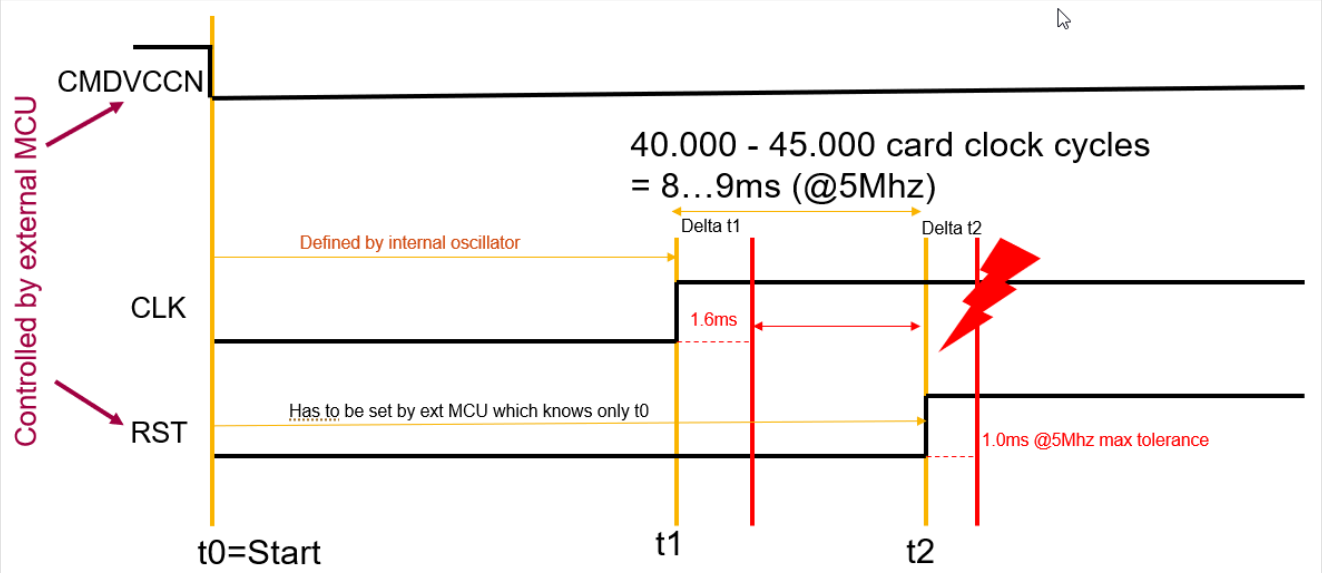

Figure 2. CMDVCC, CLK, and RST control

If the low-frequency-oscillator is running on the minimum frequency side, CLK will be raised later and RST is ultimately pulled high, from the host MCU, too early. Vice versa, if the low-frequency-oscillator is running more on the maximum side of its frequency, CLK will be raised earlier and RST ultimately will be pulled high, from the MCU, too late.

1.3 Counter measure

To overcome this situation, one solution is that the host MCU is aware of the low-frequency-oscillators frequency and takes it into account for the time CMDVCC → RST.

On following pages the measurement, calculation and the conclusion will be explained.

Other TDAs

At the current version of the document, this proposal is explained by using a TDA8035. This solution can be used for all TDA products by adjusting the calculation respectively to the TDAs data sheet.

2 Measurements

There is no direct way to measure the internal low-frequency-oscillator's frequency. But the debounce time of PRESN to OFFN is directly related to the internal low-frequency-oscillators frequency.

By measuring the time between the PRESN and OFFN signal, the frequency can be calculated.

Table 1. TDA pinout

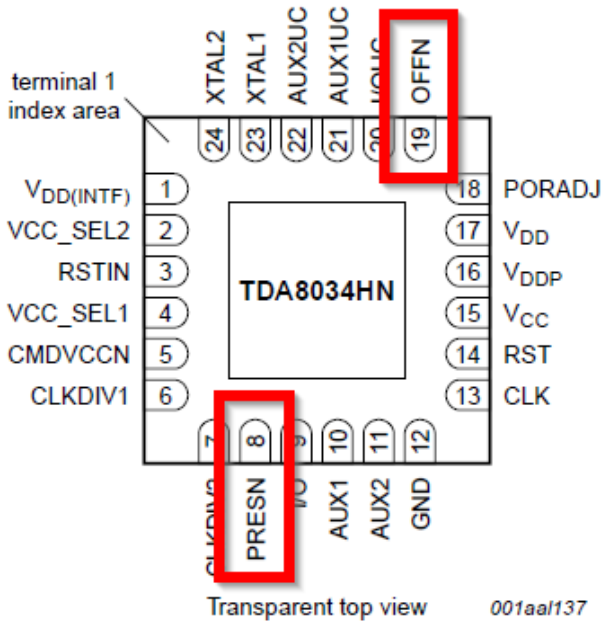

Figure 3. TDA8034 pinning

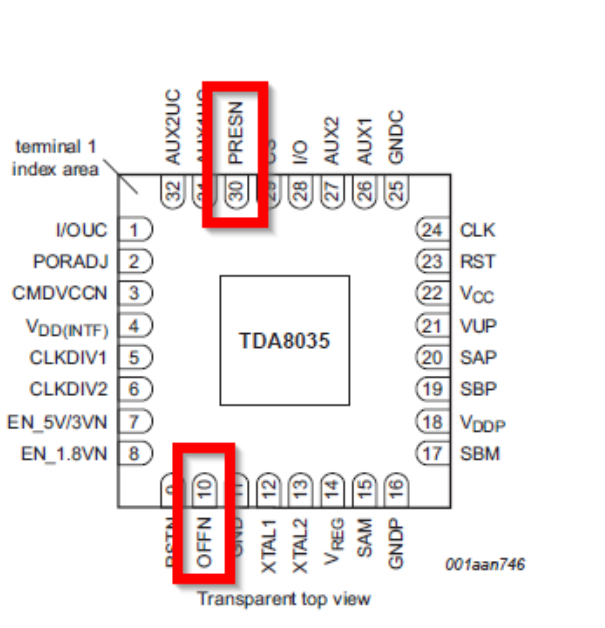

Figure 4. TDA8035 pinning

Usually the PRESN is not connected to the host MCU and only OFFN is known. But for this calculation it is necessary to measure the time between PRESN and OFFN. There are several ways how this can be achieved. Manual measuring, routing PRESN to the MCU or triggering PRESN at a well-known time.

For future designs, it is recommended to route PRESN to an MCU input to measure this timing at need.

In figure Figure 5 the time between PRESN high → low to OFFN low → high has been measured, on a TDA8035 with **3.9337 ms**.

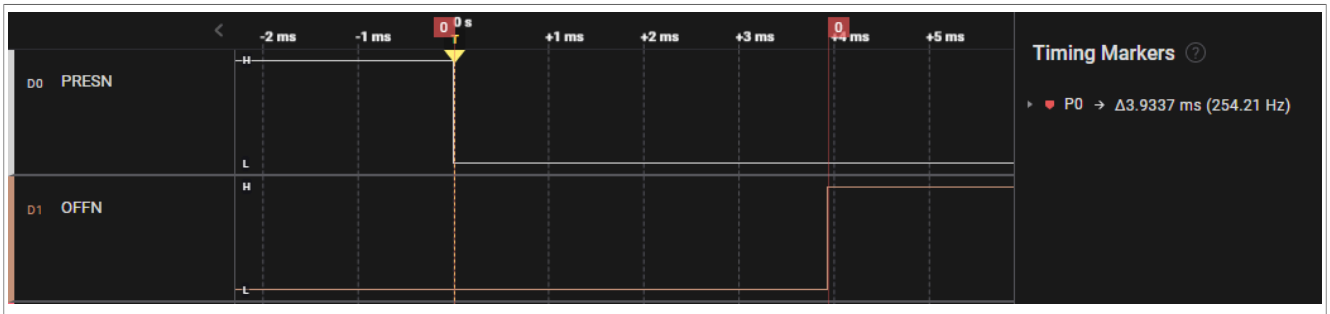

Figure 5. TDA8035 PRESN to OFFN measurement

Note: If the time is measured by the host MCU (PRESN → OFFN), it has to be made sure that this time is measured as accurate as possible. Interrupt latency, a polling approach, or an RTOS may introduce a delay significant enough to falsify the result. An accuracy of 0.1 ms can be considered as good enough.

3 Calculation

From the debounce time (see [2], [3]) we can calculate the frequency of the internal oscillator.

Table 2. Calculation formula of $f_{osc(int)\_Low}$ of TDA8035

Symbol	TDA8035	TDA8034
t_{deb}	$tdeb = 1280 * \frac{1}{f_{osc(int)\_Low}}$ (1)	$tdeb = 640 * \frac{1}{f_{osc(int)low}}$ (2)
$f_{osc(int)\_Low}$	$f_{osc(int)\_Low} = 1280 * \frac{1}{tdeb}$ (3)	$f_{osc(int)low} = 640 * \frac{1}{tdeb}$ (4)

With the time of 3.9337 ms measured in Figure 5, the resulting frequency of the TDA8035s internal low-frequency-oscillator is: **325.39 kHz**

$$1280 * \frac{1}{3{,}9337ms} = 325{,}39\ kHz \quad (5)$$

With the known frequency of the internal low-frequency-oscillator and the activation sequence from the data sheet (see [2] [8.7 Activation sequence]), the time until CLK rises can be calculated and the internal MCU timer for RST adjusted accordingly.

At Figure 6, the timing is calculated. Where 'act.' is the column with the actual measured frequency of the low-frequency-oscillator, compared to the calculation of the minimum, typical and maximum frequency.

Signal	Frequency	act.	min.	typ.	max.
	Toscint(freq high)	2500	2500	2500	2500
	Tosc(freq low)	325,39	230	315	430
	fXtal	5000	5000	5000	5000
	x	0,002	0,002	0,002	0,002
	Marker				
	T = 64 x Toscint (freq high)	0,026	0,026	0,026	0,026
CMDVCC	t0 = start				
VUP	t1 = t0 + 768 x Tosc(freq low)	2,360	3,339	2,438	1,786
VCC	t2 = t1 + 3T/2	2,399	3,378	2,476	1,824
I/O	t3 = t1 + 10T	2,616	3,595	2,694	2,042
CLK	t4 = t3 + x	**2,618**	3,597	2,696	2,044

Figure 6. TDA8035 activation sequence calculation

Note: This calculation is for the **TDA8035**. For the TDA8034 it is slightly different, see [3] chapter [8.7 Activation sequence].

4 Conclusion

With the known frequency of the internal low-frequency-oscillator and the activation sequence from the data sheet, the time until CLK rises can be calculated and the internal MCU timer for RST adjusted accordingly.

To have the best possible margin, it is recommended to target an RST low → high transition at 42.500 cycles. At 5 MHz card clock (fXtal at Figure 6) this results in **8.5 ms**.

With the calculated time until CLK rise (see Figure 6) and the goal to have 8.5 ms between CLK rise and RST rise a total time of 2.6 + 8.5 = **11.1 ms** from CMDVCC low to RST high shall be used.

5 TDA8034

The TDA8034s internal low-frequency-oscillator according to its data sheet ([3]):

Internal oscillator						
$f_{osc(int)}$	internal oscillator frequency	Shutdown mode	100	150	200	kHz
		active state	2	2.7	3.2	MHz

Figure 7. TDA8034 internal oscillator

The activation sequence necessary for the calculation of CLK rise:

8.7 Activation sequence

The following device activation sequence is applied when using an external clock; see Figure 7:

1. Pin CMDVCCN is pulled LOW (t0).
2. The internal oscillator is triggered (t0).
3. The internal oscillator changes to high frequency (t1).
4. V_{CC} rises from either 0 V to 3 V or 0 V to 5 V on a controlled slope (t2).
5. Pins I/OUC, AUX1UC and AUX2UC are driven HIGH (t3).
6. The clock on pin CLK is applied to the C3 contact (t4).
7. Pin RST is enabled (t5).

Calculation of the time delays is as follows:

- $t1 = t0 + 384 \times {}^{1}/_{f_{osc(int)low}}$
- $t2 = t1$
- $t3 = t1 + 17T / 2$
- t4 = driven by host controller; > t3 and < t5
- $t5 = t1 + 23T / 2$

Remark: The value of period T is 64 times the period interval of the internal oscillator at high frequency ($^{1}/_{f_{osc(int)high}}$); t3 is called $t_{d(start)}$ and t5 is called $t_{d(end)}$.

Figure 8. TDA8034 activation sequence

6 TDA8035

The TDA8035s internal low-frequency-oscillator "osc(int)_Low" according to the data sheet [2] has following values:

Internal oscillator						
$f_{osc(int)}$	internal oscillator frequency	inactive state: osc(int)_Low	230	315	430	kHz
		active state: osc(int)_High	2.0	2.5	3.0	MHz

Figure 9. TDA8035 internal oscillator

The activation sequence according to the data sheet [2]:

8.7 Activation sequence

The following sequence then occurs with crystal oscillator (see Figure 8):

$T = 64 \times T_{oscint}$ (freq high)

1. CMDVCCN is pulled low (t0)
2. Crystal oscillator start-up time (t0).
3. The internal oscillator changes to its high frequency and DC-to-DC starts
   $t1 = t0 + 768 \times T_{osc\ (freq\ low)}$
4. V_{CC} rises from 0 to selected V_{CC} value (5 V, 3 V, 1.8 V) with a controlled slope ($t_2 = t_1 + 3T/2$)
5. I/O, AUX1 and AUX2 are enabled ($t_3 = t_1 + 10T$), until now, they were pulled LOW
6. CLK is applied to the C3 contact ($t_4 = t_3 + \times$) with 200 ns < × < 10 × $1/f_{Xtal}$
7. RST is enabled ($t_5 = t_1 + 13T$).

Figure 10. TDA8035 activation sequence

Used in the calculation Figure 6 "TDA8035 activation sequence calculation".

7 References

[1] EMV Contact Terminal Level 1 Type Approval Version 4.3d December 2021
[2] TDA8035 High integrated and low power smart card interface Rev. 3.1 - 30 June 2016
[3] TDA8034 Low power smart card interface Rev. 3.5 - 13 March 2020

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Tables

Figures

Contents

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