AN13249

i.MX 8QuadMax Current Drain with Low- and High-Power Use Cases

Rev. 1 — 22 July 2021

Application Note

Contents

1 Introduction

This application note presents current drain measurements of the i.MX 8 QuadMax Application Processor utilizing several low- and high-power use cases. The NXP MEK (Multisensory Evaluation Kit) Platform was utilized for test bench data collection.

You can use the *i.MX 8QuadMax Automotive and Infotainment Applications Processors* data sheet as a companion document with this application note. See the Operating Ranges table in the data sheet.

The data presented in this application note is based on empirical measurements taken on a small sample size of processor revision B0 silicon. Due to the sample size, the presented results are not guaranteed across all process, voltage, and temperature ranges.

2 System Power Tree

The i.MX 8 QuadMax processor has several power supply domains (voltage supply rails). The following table shows how some of the independent power rails of the processor are merged on the MEK design. Power rails referenced in this application note use MEK schematic power rail net names.

Table 1. Processor Power Domains Consolidation on PCB

MEK Schematic Power Rail Net Name	Associated Processor and Peripheral Supply
VCC_SNVS	VDD_SNVS_4P2
VCC_SCU_1V8	VDD_SCU_1P8 + VDD_SCU_XTAL_1P8 + VDD_ANAx_1P8 + VDD_SCU_ANA_1P8 + VDD_CP_1P8
VCC_CPU1	VDD_A72
VCC_CPU0	VDD_A53
VCC_GPU0	VDD_GPU0
VCC_GPU1	VDD_GPU1
VCC_MEMC	VDD_MEMC
VCC_MAIN	VDD_MAIN + VDD_MIPI_CSIx_1P0 + VDD_MIPI_DSIx_1P0 + VDD_MIPI_DSIx_PLL_1P0 + VDD_LVDSx_1P0
VCC_DDRIO0	VDD_DDR_CH0_VDDQ + VDD_DDR_CH0_VDDQ_CKE + External LPDDR4 DRAM VDDQ & VDD2

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Table 1. Processor Power Domains Consolidation on PCB (continued)

MEK Schematic Power Rail Net Name	Associated Processor and Peripheral Supply
VCC_DDRIO1	VDD_DDR_CH1_VDDQ + VDD_DDR_CH1_VDDQ_CKE + External LPDDR4 DRAM VDDQ & VDD2
VCC_1V8	1V8[1]
VCC_3V3	3V3[2]

1. VDD_PCIE_IOB_1P8, VDD_ADC_1P8, VDD_ADC_DIG_1P8, VDD_HDMI_RX0_1P84, VDD_HDMI_TX0_1P8, VDD_LVDS0_1P8, VDD_LVDS1_1P8, VDD_MIPI_CSI0_1P8, VDD_MIPI_CSI1_1P8, VDD_MIPI_DSI0_1P8, VDD_MIPI_DSI1_1P8, VDD_MLB_1P8, VDD_PCIE_LDO_1P8, VDD_PCIE_SATA0_PLL_1P84, VDD_PCIE0_PLL_1P8, VDD_PCIE1_PLL_1P8, VDD_USB_HSIC0_1P8, VDD_ANA0_1P8, VDD_MIPI_CSI_DIG_1P8xx, VDD_ENET1_1P8_2P5_3P3, VDD_ENET0_1P8_3P3, VDD_EMMC0_1P8_3P3, VDD_USDHC_VSELECT_1P8_3P3, VDD_ESAI0_MCLK_1P8_3P3, VDD_ESAI1_SPDIF_SPI_1P8_3P3, VDD_LVDS_DIG_1P8_3P3, VDD_M4_GPT_UART_1P8_3P3, VDD_MIPI_DSI_DIG_1P8_3P3, VDD_QSPI0_1P8_3P3, VDD_SPI_SAI_1P8_3P3. 2 x DRAM VDD1, eMMC VCCQ, and several low-power peripheral devices are powered by VCC_1V8.
2. VDD_HDMI_RX0_VH_RX_3P3, VDD_HDMI_TX0_DIG_3P3, VDD_USB_OTG1_3P3, VDD_USB_OTG2_3P3, VDD_USB_SS3_TC_3P3, VDD_PCIE_DIG_1P8_3P3, VDD_ENET_MDIO_1P8_3P3 (VDD_ENET_MDIO_1P8_2P5_3P3), VDD_FLEXCAN_1P8_3P3, VDD_MLB_DIG_1P8_3P3, VDD_QSPI1A_1P8_3P3. . The LDO that generates VCC_EXT_LDO_USB for processor HSIC is powered by VCC_3V3. In addition, the ENET PHY, PCIe 100 MHz reference clock generator, and several low-power peripheral devices are powered by VCC_3V3.

3 Test Cases, Hardware, and Data

Data is presented utilizing several low-power and high-power use cases as described in the next subsections. Junction temperature conditions of 25ºC, 105ºC, and 125ºC are shown in the tables. In the following tables, some entries appear lower at high temperature as readings are impacted by several factors including noise and the 60-second measurement interval for average current. DRAM current includes both the processor and DRAM chip.

Hardware utilized is a modified NXP MEK (Multisensory Evaluation Kit) Platform. Additional series resistors are added on MEK power rails at the PMIC inductor sites to facilitate current measurement. The exception is VCC_SCU_1V8 where the series resistor site is used. Data is obtained by measuring voltage drop across 0.025 Ω series resistors on each supply rail, then dividing by the resistor value to derive current. The tolerance of the 0.025 Ω resistors is 1%.

VCC_SCU_1V8 setpoint is 1.7 V, as defined in the *i.MX 8QuadMax Automotive and Infotainment Applications Processors* data sheet.

With the exception of KS0, data is representative of several samples both from randomly-selected devices and matrix lots. Data is presented as the minimum and maximum values extracted from raw data for the samples selected.

3.1 KS0 – Low-Power Key State 0

KS0 is defined by the following conditions.

- VDD_SNVS = 4.2 V, all other supplies = 0 V
- 32.768 kHz oscillator enabled
- RTC (Real-Time Clock) running
- Tamper not active

Summarized data on > 1000 processor samples are presented. Data is presented as minimum and maximum values extracted from ATE (Automated Test Equipment) data.

Table 2. KS0 Results

		125 ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Max Average Current (mA)	Min Average Current (mA)
VCC_SNVS	4.2	0.047	0.007

3.2 KS1 – Low-Power Key State 1

KS1 is defined by the following conditions.

- RAM and I/O state retained
- 32.768 kHz oscillator enabled
- 24 MHz oscillator, PLLs, and ring oscillators off
- DRAM in self-refresh, associated I/Os disabled
- PHYs in idle state
- MEMC, A53, A72, and GPUs not powered
- VCC_MAIN = 0.8 V

Table 3. KS1 Results

		25ºC		105ºC		125ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Max Peak Current (mA)	Min Average Current (mA)	Max Peak Current (mA)	Min Average Current (mA)	Max Peak Current (mA)	Min Average Current (mA)
VCC_MAIN	0.8	12.1	2.0	96.3	31.7	148	58
VCC_CPU0 (A53)	0	-	-	-	-	-	-
VCC_CPU1 (A72)	0	-	-	-	-	-	-
VCC_GPU0	0	-	-	-	-	-	-
VCC_GPU1	0	-	-	-	-	-	-
VCC_DDRIO0	1.1	1.6	1.1	4.6	3.6	6.6	6.4
VCC_DDRIO1	1.1	1.6	1.3	4.9	3.8	6.9	6.8
VCC_MEMC	0	-	-	-	-	-	-
VCC_1V8	1.8	7.5	7.3	9.4	8.7	11	10

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Table 3. KS1 Results (continued)

		25ºC		105ºC		125ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Max Peak Current (mA)	Min Average Current (mA)	Max Peak Current (mA)	Min Average Current (mA)	Max Peak Current (mA)	Min Average Current (mA)
VCC_3V3[1]	3.3	107	106	109	105	109	109
VCC_SCU_1V8	1.7	6.0	2.3	6.7	2.5	7.0	2.9

1. Approximately 88 mA is consumed by the PCIe 100 MHz reference and ENET PHY peripheral devices across temperature. With these 2 devices removed from one board, KS1 VCC_3V3 system current drain measured approximately 20 mA across temperature. Although not measured, the PCA9511 I2C buffer data sheet indicates typical supply current of 3.5 mA each. Two of these devices are on the VCC_3V3 rail.

3.3 KS2 – Low-Power Key State 2

KS2 is defined by the following conditions.

- Linux operating
- 1 x A53 powered, running at 900 MHz
- 2 x A72 not powered
- GPUs powered and idling
- Screens are off, no display traffic occurring

Table 4. KS2 Results

		25ºC		105ºC		125ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Max Peak Current (mA)	Min Average Current (mA)	Max Peak Current (mA)	Min Average Current (mA)	Max Peak Current (mA)	Min Average Current (mA)
VCC_MAIN	1.0	596	586	900	882	1135	1118
VCC_CPU0 (A53)	1.0	31	19	112	95	175	151
VCC_CPU1 (A72)	0	-	-	-	-	-	-
VCC_GPU0	1.1	22	22	252	229	442	420
VCC_GPU1	1.1	21	21	245	228	415	415
VCC_DDRIO0	1.1	80	61	81	63	87	64
VCC_DDRIO1	1.1	77	60	81	63	80	64

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Table 4. KS2 Results (continued)

		25ºC		105ºC		125ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Max Peak Current (mA)	Min Average Current (mA)	Max Peak Current (mA)	Min Average Current (mA)	Max Peak Current (mA)	Min Average Current (mA)
VCC_MEMC	1.1	625	514	957	834	1118	1013
VCC_1V8	1.8	252	235	258	241	266	248
VCC_3V3[1]	3.3	125	125	128	128	128	128
VCC_SCU_1V8	1.7	55	54	53	52	53	52

1. Approximately 88 mA is consumed by the PCIe 100 MHz reference and ENET PHY peripheral devices across temperature. Although not measured, the PCA9511 I2C buffer data sheet indicates typical supply current of 3.5 mA each. Two of these devices are on the VCC_3V3 rail.

3.4 KS3 – Low-Power Key State 3

KS3 is defined by the following conditions.

- Linux operating, command prompt
- 1 x A53 CPU powered and idling @ 900 MHz
- 2 x A72 not powered
- Both GPUs powered but idle
- One 1080p screen active, displaying static image
- GPU not rendering an active, changing frame buffer

Table 5. KS3 Results

		25ºC		105ºC		125ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Max Peak Current (mA)	Min Average Current (mA)	Max Peak Current (mA)	Min Average Current (mA)	Max Peak Current (mA)	Min Average Current (mA)
VCC_MAIN	1.0	619	602	929	900	1175	1128
VCC_CPU0 (A53)	1.0	64	19	127	96	183	150
VCC_CPU1 (A72)	0	-	-	-	-	-	-
VCC_GPU0	1.1	179	23	1132	235	1776	398
VCC_GPU1	1.1	211	22	1002	234	1457	394

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Table 5. KS3 Results (continued)

		25ºC		105ºC		125ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Max Peak Current (mA)	Min Average Current (mA)	Max Peak Current (mA)	Min Average Current (mA)	Max Peak Current (mA)	Min Average Current (mA)
VCC_DDRIO0	1.1	181	133	185	135	185	136
VCC_DDRIO1	1.1	181	132	186	134	202	138
VCC_MEMC	1.1	1187	1119	1554	1456	1768	1660
VCC_1V8	1.8	257	245	263	252	268	260
VCC_3V3[1]	3.3	125	125	128	128	129	128
VCC_SCU_1V8	1.7	82	55	81	53	81	52

1. Approximately 88 mA is consumed by the PCIe 100 MHz reference and ENET PHY peripheral devices across temperature. Although not measured, the PCA9511 I2C buffer data sheet indicates typical supply current of 3.5 mA each. Two of these devices are on the VCC_3V3 rail.

3.5 PS0 – Power State 0

PS0 is defined by the following conditions.

- 4 x A53 = 1 V running Coremark @ 900 MHz
- 2 x A72 power-gated off

Table 6. PS0 Results

		25ºC		105ºC		125ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Maximum Peak Current (A)	Minimum Average Current (A)	Maximum Peak Current A)	Minimum Average Current (A)	Maximum Peak Current (A)	Minimum Average Current (A)
VCC_MAIN	1.0	0.667	0.585	1.367	0.881	1.780	1.099
VCC_CPU0 (A53)	1.0	0.506	0.440	0.913	0.610	1.114	0.716
VCC_CPU1 (A72)	1.0	0.001	0.001	0.001	0.001	0.001	0.001
VCC_GPU0	1.1	0.066	0.020	0.551	0.236	0.830	0.392
VCC_GPU1	1.1	0.081	0.019	0.636	0.233	0.948	0.388
VCC_DDRIO0	1.1	0.094	0.059	0.097	0.062	0.103	0.064

Table continues on the next page...

Table 6. PS0 Results (continued)

		25ºC		105ºC		125ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Maximum Peak Current (A)	Minimum Average Current (A)	Maximum Peak Current A)	Minimum Average Current (A)	Maximum Peak Current (A)	Minimum Average Current (A)
VCC_DDRIO1	1.1	0.094	0.060	0.099	0.063	0.100	0.065
VCC_MEMC	1.1	1.085	0.517	1.568	0.827	1.406	0.994
VCC_1V8	1.8	0.262	0.239	0.273	0.244	0.281	0.251
VCC_3V3[1]	3.3	0.127	0.125	0.130	0.128	0.130	0.128
VCC_SCU_1V8	1.7	0.054	0.053	0.054	0.051	0.058	0.050

1. Approximately 0.088 A is consumed by the PCIe 100 MHz reference and ENET PHY peripheral devices across temperature.

3.6 PS1 – Power State 1

PS1 is defined by the following conditions.

- 4 x A53 = 1.1 V running Coremark @ 1.2 GHz
- 2 x A72 power-gated off

Table 7. PS1 Results

		25ºC		105ºC		125ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Maximum Peak Current (A)	Minimum Average Current (A)	Maximum Peak Current A)	Minimum Average Current (A)	Maximum Peak Current (A)	Minimum Average Current (A)
VCC_MAIN	1.0	0.668	0.586	1.356	0.873	1.773	1.083
VCC_CPU0 (A53)	1.1	0.859	0.684	1.669	1.043	2.026	1.266
VCC_CPU1 (A72)	1.0	0.001	0.001	0.001	0.001	0.001	0.001
VCC_GPU0	1.1	0.067	0.020	0.542	0.231	0.821	0.386
VCC_GPU1	1.1	0.082	0.019	0.626	0.226	0.937	0.379
VCC_DDRIO0	1.1	0.091	0.060	0.092	0.064	0.110	0.063
VCC_DDRIO1	1.1	0.189	0.064	0.168	0.063	0.101	0.065

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Table 7. PS1 Results (continued)

		25ºC		105ºC		125ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Maximum Peak Current (A)	Minimum Average Current (A)	Maximum Peak Current A)	Minimum Average Current (A)	Maximum Peak Current (A)	Minimum Average Current (A)
VCC_MEMC	1.1	0.818	0.545	1.542	0.855	1.894	0.987
VCC_1V8	1.8	0.263	0.252	0.277	0.257	0.280	0.249
VCC_3V3[1]	3.3	0.128	0.126	0.130	0.128	0.130	0.128
VCC_SCU_1V8	1.7	0.076	0.073	0.078	0.076	0.078	0.075

1. Approximately 0.088 A is consumed by the PCIe 100 MHz reference and ENET PHY peripheral devices across temperature.

3.7 PS2 – Power State 2

PS2 is defined by the following conditions.

- 4 x A53 = 1 V running Coremark @ 900 MHz
- 1 x A72 = 1 V running Coremark @ 1.06 GHz
- 1 x A72 power-gated off

Table 8. PS2 Results

		25ºC		105ºC		125ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Maximum Peak Current (A)	Minimum Average Current (A)	Maximum Peak Current (A)	Minimum Average Current (A)	Maximum Peak Current (A)	Minimum Average Current (A)
VCC_MAIN	1.0	0.670	0.586	1.357	0.875	1.768	1.082
VCC_CPU0 (A53)	1.0	0.509	0.429	0.908	0.585	1.110	0.683
VCC_CPU1 (A72)	1.0	0.482	0.422	0.740	0.499	0.889	0.597
VCC_GPU0	1.1	0.067	0.020	0.542	0.243	0.817	0.395
VCC_GPU1	1.1	0.082	0.019	0.628	0.231	0.946	0.384
VCC_DDRIO0	1.1	0.124	0.066	0.125	0.070	0.148	0.074
VCC_DDRIO1	1.1	0.126	0.064	0.126	0.067	0.124	0.070
VCC_MEMC	1.1	1.071	0.612	1.977	0.974	2.280	1.068

Table continues on the next page...

Table 8. PS2 Results (continued)

		25ºC		105ºC		125ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Maximum Peak Current (A)	Minimum Average Current (A)	Maximum Peak Current (A)	Minimum Average Current (A)	Maximum Peak Current (A)	Minimum Average Current (A)
VCC_1V8	1.8	0.263	0.251	0.274	0.246	0.282	0.252
VCC_3V3[1]	3.3	0.128	0.125	0.130	0.128	0.130	0.128
VCC_SCU_1V8	1.7	0.059	0.057	0.058	0.055	0.058	0.055

1. Approximately 0.088 A is consumed by the PCIe 100 MHz reference and ENET PHY peripheral devices across temperature.

3.8 PS3 – Power State 3

PS3 is defined by the following conditions.

- 4 x A53 = 1.1 V running Coremark @ 1.2 GHz
- 1 x A72 = 1.1 V running Coremark @ 1.6 GHz
- 1 x A72 power-gated off

Table 9. PS3 Results

		25ºC		105ºC		125ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Maximum Peak Current (A)	Minimum Average Current (A)	Maximum Peak Current (A)	Minimum Average Current (A)	Maximum Peak Current (A)	Minimum Average Current (A)
VCC_MAIN	1.0	0.672	0.588	1.358	0.875	1.771	1.118
VCC_CPU0 (A53)	1.1	0.857	0.659	1.658	1.032	2.040	1.257
VCC_CPU1 (A72)	1.1	0.930	0.792	1.661	1.244	2.035	1.496
VCC_GPU0	1.1	0.067	0.020	0.537	0.218	0.820	0.375
VCC_GPU1	1.1	0.083	0.019	0.623	0.214	0.945	0.368
VCC_DDRIO0	1.1	0.167	0.068	0.171	0.069	0.146	0.071
VCC_DDRIO1	1.1	0.137	0.069	0.131	0.074	0.148	0.068
VCC_MEMC	1.1	1.179	0.590	1.981	0.932	2.029	1.121
VCC_1V8	1.8	0.264	0.242	0.276	0.248	0.285	0.252

Table continues on the next page...

Table 9. PS3 Results (continued)

		25ºC		105ºC		125ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Maximum Peak Current (A)	Minimum Average Current (A)	Maximum Peak Current (A)	Minimum Average Current (A)	Maximum Peak Current (A)	Minimum Average Current (A)
VCC_3V3[1]	3.3	0.128	0.125	0.130	0.128	0.130	0.128
VCC_SCU_1V8	1.7	0.092	0.088	0.095	0.091	0.096	0.092

1. Approximately 0.088 A is consumed by the PCIe 100 MHz reference and ENET PHY peripheral devices across temperature.

3.9 PS4 – Power State 4

PS4 is defined by the following conditions.

- 2 x GPUs running GLmark2

Table 10. PS4 Results

		25ºC		105ºC		125ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Maximum Peak Current (A)	Minimum Average Current (A)	Maximum Peak Current (A)	Minimum Average Current (A)	Maximum Peak Current (A)	Minimum Average Current (A)
VCC_MAIN	1.0	0.798	0.678	1.504	0.991	1.857	1.201
VCC_CPU0 (A53)	1.1	0.488	0.163	1.291	0.482	1.627	0.676
VCC_CPU1 (A72)	1.0	0.542	0.046	2.107	0.171	3.060	0.326
VCC_GPU0	1.1	2.110	0.977	2.821	1.486	3.181	1.662
VCC_GPU1	1.1	2.048	1.142	3.369	1.624	3.957	1.829
VCC_DDRIO0	1.1	0.627	0.405	0.658	0.392	0.625	0.416
VCC_DDRIO1	1.1	0.645	0.494	0.670	0.521	0.649	0.513
VCC_MEMC	1.1	1.807	1.533	2.563	1.881	2.949	2.100
VCC_1V8	1.8	0.282	0.251	0.290	0.258	0.296	0.264
VCC_3V3[1]	3.3	0.128	0.125	0.130	0.128	0.130	0.130
VCC_SCU_1V8	1.7	0.134	0.113	0.135	0.116	0.137	0.115

1. Approximately 0.088 A is consumed by the PCIe 100 MHz reference and ENET PHY peripheral devices across temperature.

3.10 PS5 – Power State 5

PS5 is defined by the following conditions.

- 4 x A53 = 1.1 V running Coremark @ 1.2 GHz
- 1 x A72 = 1.1 V running graphics @ 1.6 GHz
- 1 x A72 power-gated off
- VPU decoding HEVC 3840 x 2160 @ 60 fps
- AACLC @ 48 kHz, 6 channels audio

Table 11. PS5 Results

		25ºC		105ºC		125ºC	
MEK Schematic Power Rail Net Name	Voltage (V)	Maximum Peak Current (A)	Minimum Average Current (A)	Maximum Peak Current (A)	Minimum Average Current (A)	Maximum Peak Current (A)	Minimum Average Current (A)
VCC_MAIN	1.0	1.535	1.374	2.252	1.683	2.635	1.294
VCC_CPU0 (A53)	1.1	0.893	0.702	1.668	1.058	2.038	1.225
VCC_CPU1 (A72)	1.1	1.127	0.364	1.809	0.802	2.338	1.116
VCC_GPU0	1.1	1.690	0.904	3.097	1.080	3.221	1.690
VCC_GPU1	1.1	2.035	1.013	2.921	1.390	3.868	0.584
VCC_DDRIO0	1.1	0.694	0.582	0.718	0.568	0.690	0.582
VCC_DDRIO1	1.1	0.719	0.619	0.722	0.639	0.685	0.609
VCC_MEMC	1.1	1.952	1.643	2.708	1.997	2.952	2.407
VCC_1V8	1.8	0.284	0.257	0.295	0.264	0.300	0.129
VCC_3V3[1]	3.3	0.128	0.125	0.130	0.128	0.130	0.130
VCC_SCU_1V8	1.7	0.137	0.125	0.133	0.117	0.137	0.127

1. Approximately 0.088 A is consumed by the PCIe 100 MHz reference and ENET PHY peripheral devices across temperature.

4 Supply Current for I/O

A general equation for estimated current drain of an I/O supply rail is as follows.

I = N x C x V x R x F

Where:

N – Number of I/O powered by the supply rail

C – Equivalent external capacitive load

V – I/O supply voltage

R – Data change rate (for example use 0.5 for ½ of the clock rate)

F – Clock rate

I is in Amps, C in Farads, V in Volts, and F in Hertz.

5 References

- i.MX 8QuadMax Automotive and Infotainment Applications Processors
- MCIMX8QM-CPU MEK Platform

6 Revision history

Table 12. Revision history

Revision number	Date	Substantive changes
1	22 July 2021	• Updated footnotes in Table 1 • Added footnotes in Table 3, Table 4, Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, and Table 11
0	4 May 2021	Initial release

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