AN13247

NXP PMIC Solution for MediaTek MT2712 Processors

Rev. 1 — 24 June 2021 Application note

Document information

Information	Content
Keywords	FS56, PF81, PF5024, Power solution, PMIC, MediaTek MT2712, Infotaiment, Functional safety
Abstract	NXP's Power Management IC (PMIC) integrates multiple power supply channels and is suitable for high-performance In-Vehicle Infotainment (IVI) systems. This application note describes NXP's PMIC solution for MediaTek MT2712 processor-based IVI systems.

Revision History

Table 1. Revision history

Revision	Date	Description
AN13247 v.1	20210624	Initial Release
Modifications	NA	

1 Introduction

This application note describes how NXP Power Management ICs (PMIC), which feature power tree configuration, power-up and power-down sequences, and digital control, can be implemented in systems that use a MediaTek MT2712 processor. This document also highlights the safety mechanisms embedded in the PMIC and includes information on interconnecting NXP functional safety PMICs with MT2712-based systems that have safety requirements.

In addition, the document also provides schematics and a BOM for a typical NXP PMIC/ MT2712 power solution.

2 System Design

The MT2712 is a MediaTek processor designed for in-vehicle infotainment (IVI) systems. The device consists of a high-performance, hexa-core system-on-chip (SoC) that features multiple ARM Cortex cores integrated in a single device. NXP's PMICs provides an ideal solution with a 1*PF81 and 1*PF5024 to power MT2712 processor systems. The PF8100 and PD5024 are highly-integrate multiple regulators well-suited to accommodate the high-performance demands of IVI processors like the MT2712.

Figure 1 shows the NXP PMIC power solution for MT2712-based IVI system. The block diagram is based on a Quality Management (QM) PMIC for systems with QM requirements. Normally, a single MCU is linked with the MT2712 for IVI applications. One function of the MCU is to control the MT2712's domain power on/off function.

The FS56 is an automotive multi-output power supply integrated circuit. It has a battery-connected pre-regulator Buck2 that generates intermediate voltages to supply power to the PF81 and F5024. The FS56 also integrates a battery connected Buck1 regulator that can be used to supply the MCU and other peripherals. The FS56 supports 12 V battery systems. The PF81 and PF5024 provide regulators for the MT2712's power rails.

The FS56, PF81, PF5024 feature a built-in one-time programmable (OTP) memory that stores key startup configurations. The PF81 and the PF5024 also have dedicated functional blocks for synchronizing multiple PMIC operations. These blocks minimize design time and reduce system complexity by implementing a single-chipset approach that eliminates the need for external controllers to support system default voltage configurations and power up synchronization.

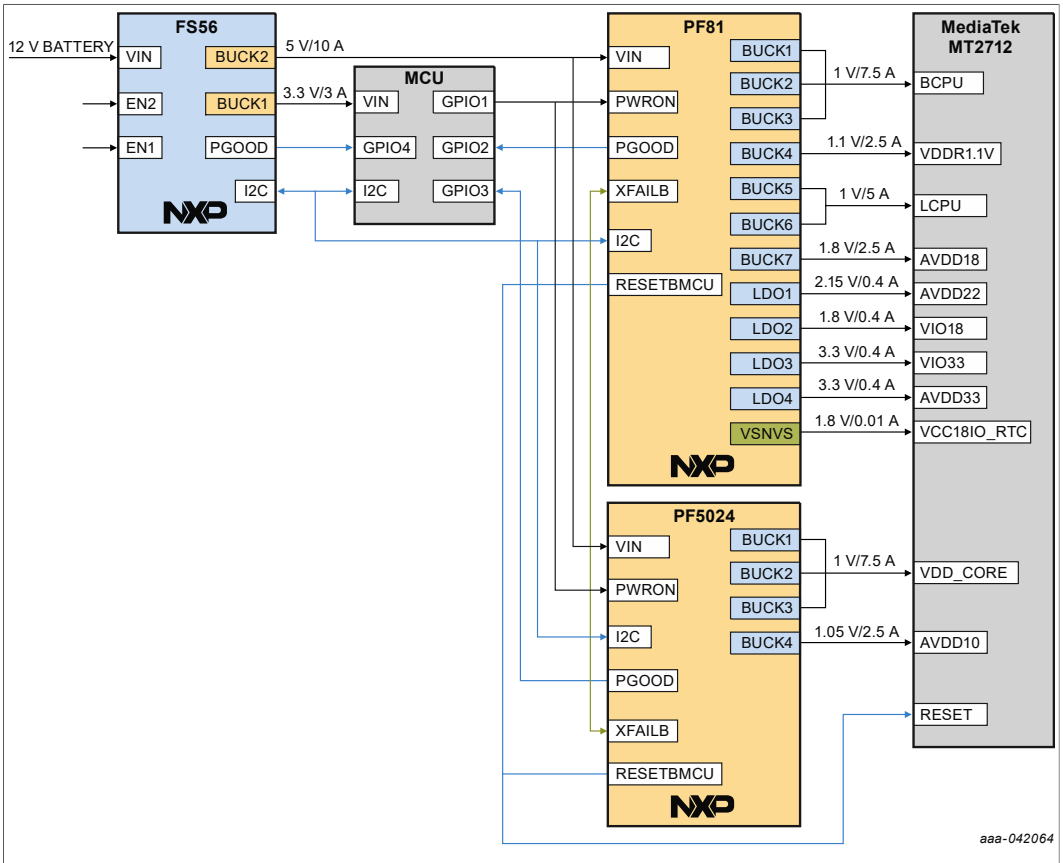

Figure 1. NXP PMIC power solution block diagram for MediaTek MT2712 based IVI system

Table 2. PMIC block functions

PMIC	Block	Functions
FS56	Vin	Power input from 12 V battery
	Buck1, Buck2	Power supply output
	EN1	Enable signal for Buck2; connects to KL15 or CAN transceiver INH signal
	EN2	Enable signal for Buck2; connect to 12 V battery if FS56 Buck2 needs always-on functionality
	Pgood	PF81 Power good indicator
	I^2C	I^2C communication with MCU
	Vin	Power input from FS56
PF81	Buck1, Buck2 ,Buck3, Buck4, Buck5, Buck6, Buck7 LDO1, LDO2, LDO3, LDO4	Power supply output
	VSNVS	Always-on power supply for MT2712 RTC
	POWERON	PF81 power-up enable input controlled by MCU
	I^2C	I^2C communication with MCU
	Pgood	PF81 Power good indicator
	XFAILB	Bidirectional pin for multi PMIC power-up\down sequence synchronization
	RESETMCU	Reset connection wtih MT2712
PF5024	Vin	Power input from FS56
	Buck1, Buck2, Buck3, Buck4	PF5024 Power supply output
	POWERON	PF5024 power-up enable input which control by MCU
	I^2C	I^2C communication with MCU
	Pgood	PF5024 Power good indicator
	XFAILB	Bidirectional pin for multi pmic power up\down sequence synchronization
	RESETMCU	Reset connection wtih MT2712

3 MT2712 Power Solution

The PF81 contains seven high-efficiency buck converters and four linear regulators with load switch options. The PF5024 contains four buck converters. Each buck converter on both the PF81 and the PF5024 are rated up to 2500 mA and linear regulator rated up to 400 mA. PF81 and PF5024 buck converters support Dynamic Voltage Scaling (DVS). For an MT2712 power solution, PF PMICs input voltage is supplied from the FS56 BUCK2 output.

Table 3. MT2712 power rails requirements and PMIC output configuration

PMIC	Power Channel	Output Voltage/V	Current Capability/mA	MT2712 Power rails	Current Requirement/mA	Power up sequence	Power down sequence
PF81	Buck1-3	1	7500	BCPU	7000	2	5
	Buck4	1.1	2500	VDDR1.1V	493	6	2
	Buck5-6	1	5000	LCPU	3670	2	5
	Buck7	1.8	2500	AVDD18	1490	4	3
	LDO1	2.15	400	AVDD22	4	3	4
	LDO2	1.8	400	VIO18	20	4	3
	LDO3	3.3	400	VIO33	75	5	2
	LDO4	3.3	400	AVDD33	12	5	2
	VSNVS	1.8	10	VCC18IO_RTC	0.03	1	—
PF5024	Buck1-3	1	7500	VDD_CORE	6750	2	5
	Buck4	1.05	2500	AVDD10	60	4	3
—	RESETBMCU	—	—	nRESET	—	7	1

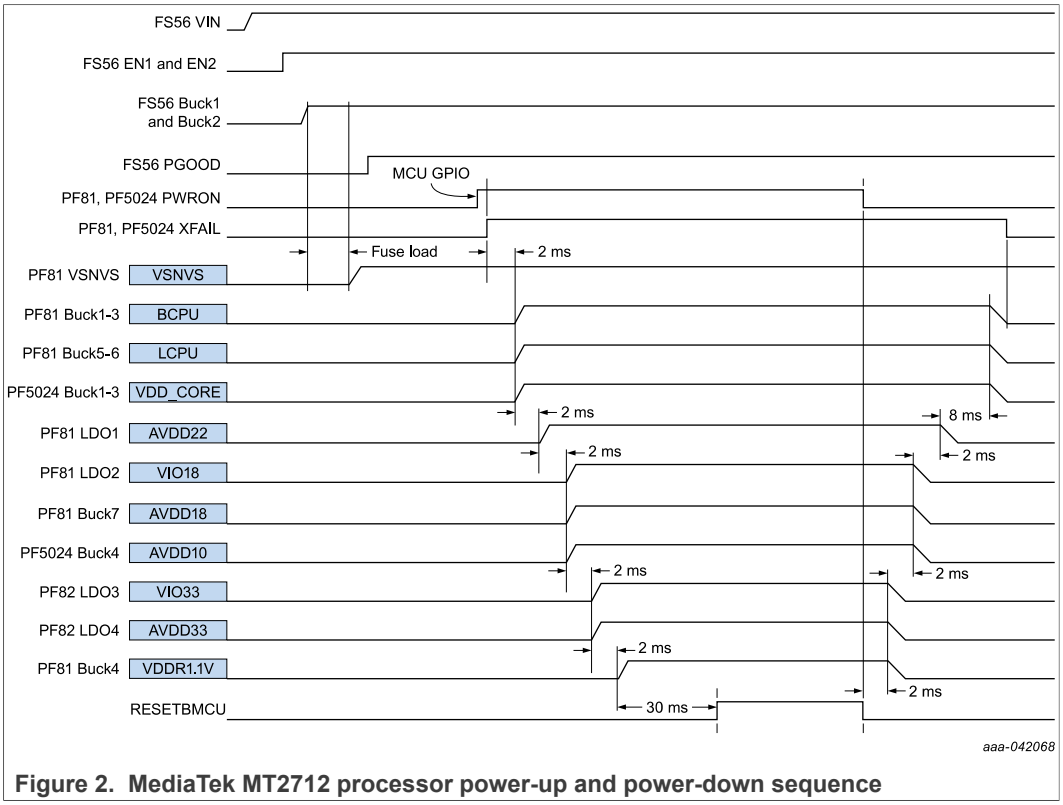

Figure 2. MediaTek MT2712 processor power-up and power-down sequence

Through the internal power-up sequencer (PWRON, XFAILB) function available on all NXP PMICs, the PF81 and the PF5024 effectively implement accurate power-up and power-down sequence synchronization for all power rails. The default sequence slots for PMICs are programmed via the OTP configuration registers. Figure 2 illustrates MT2712 processor power-up and down sequence. The specific power sequence configuration for MT2712 are programmed by OTP registers. When VIN on the PF81 or the PF5024 exceeds the UVDET threshold and the PMICs complete loading the fused configuration, VSNVS powers up. When PWRON is pulled high, the PMICs start the power-up process. PMIC regulators automatically power up according to the power-up sequence configured in the OTP. When RESETBMCU is released, the power-up sequence is complete and the MT2712 boots up.

4 Functional Safety

For safety applications with functional safety requirements, NXP provides ASIL-B and ASIL-D versions that are pin-to-pin compatible with the QM versions. The FS56, PF81, and PF5024 are ASIL-B PMIC versions with embedded safety mechanisms that comply with ISO26262. These safety mechanisms include:

- **Voltage monitoring**: NXP PMICs feature an independent voltage monitoring function for each regulator. The PMIC fault-monitoring block monitors UV, OV and ILIM faults and indicates the output state of each regulator through the PGOODx voltage regulation status pins.
- **Watchdog monitoring**: The PF81 features internal watchdog timers capable of monitoring the MT2712 processor. The FS56 also has watchdog timers capable of monitoring a safety MCU. If the PMIC internal watchdog times out, the PMIC initiates a reset.
- **I^2C CRC and write protection**: The PMICs have functional I^2C registers that are fuse-configurable. The fuse circuits have CRC error checking routines that report on and protect against PMIC register loading errors. If a register loading error is detected, a corresponding error flag is asserted. An I^2C secure-write protects secure registers from an invalid operation.
- **Analog built-in self-test(ABIST):** ABIST is designed to diagnose latent faults. It checks the voltage monitoring block (OV/UV) of each regulator to determine whether a fault has occurred. If a failure on the OV/UV monitor is detected, the PMIC asserts the corresponding ABIST flags in the I^2C register.
- **Functional safety output:** The FS56 has a functional safety output FSOB that transitions the system into a safe state when a fault cannot be handled by the safety MCU.
- **VIN OVLO function**: The PF82 and PF5024 feature VIN_OVLO circuits that monitor the PMIC's main input supply. The PMIC monitors its input voltage and initiates a power-down sequence when it detects a VIN_OVLO in the system.
- **MCU failure monitoring (FS56 only)**: The FS56 ASIL-B version features an FCCU function in charge of monitoring hardware failures from the MCU. The FCCU pins are connected to the fault output pins of the MCU. When the FCCU pin indicates that an MCU fault has occurred, the FS56 resets the MCU and\or asserts the FSOB pin.
- **External IC monitoring (FS56 only)**: The FS56 features an ERRMON function that monitors external safety IC faults in the application.
- **External voltage monitor (FS56 only)**: The FS56 ASIL-B part supports up to 4x VMON. Depending on the safety requirements, VMON can be used to monitor the PF82 to assure that the device maintains the required safety level for the system.

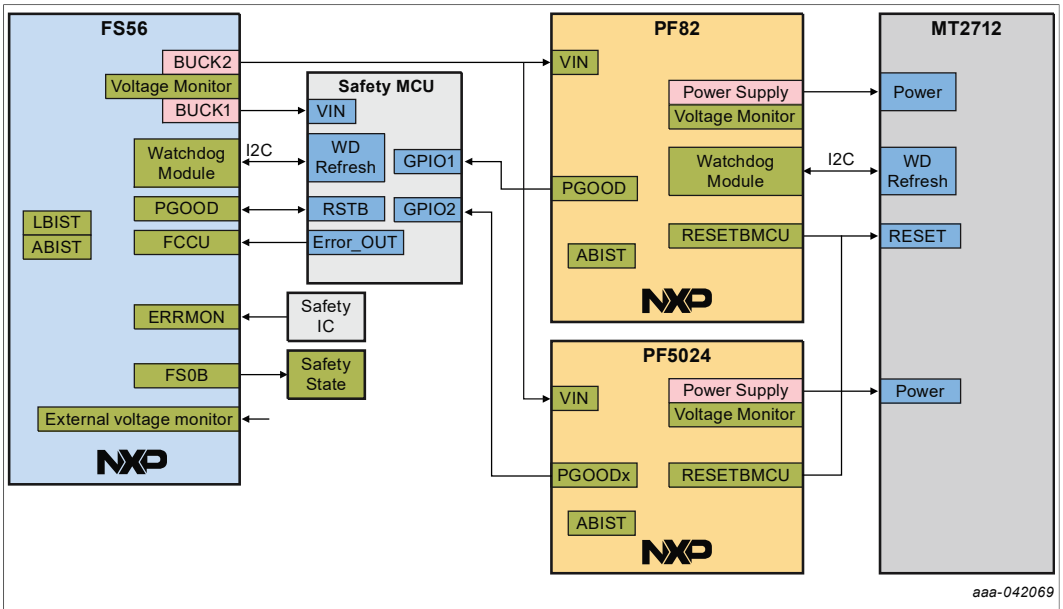

Figure 3. Functional Safety operation with MediaTek MT2712 system

5 Schematic

Figure 4 and Figure 5 show an MT2712 processor power solution schematic based on NXP PMICs.

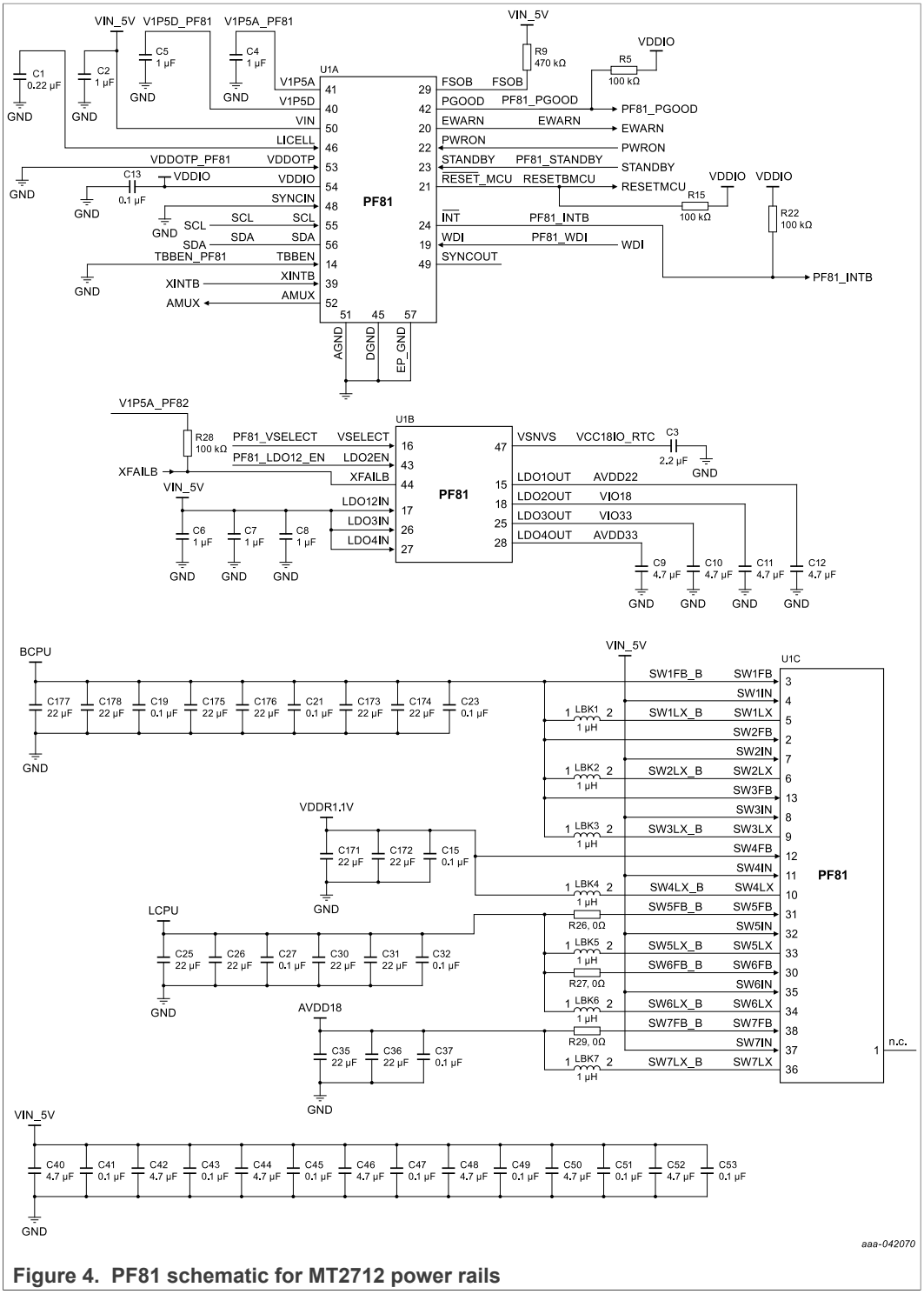

Figure 4. PF81 schematic for MT2712 power rails

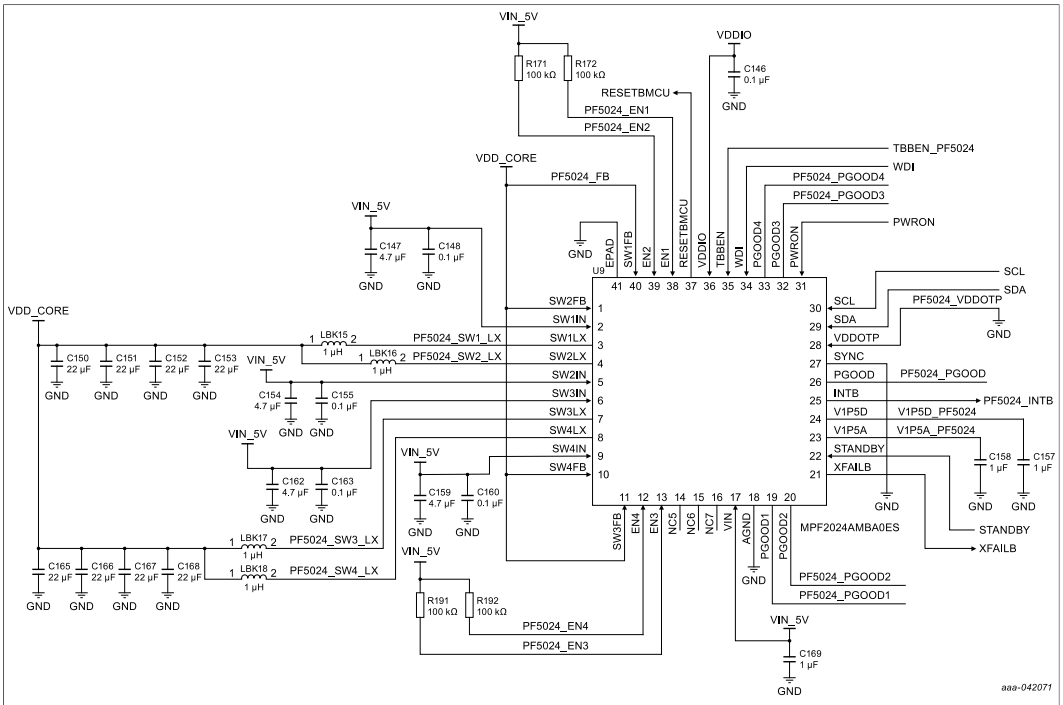

Figure 5. PF5024 schematic for MT2712 power rails

6 Bill of Material

Table 4 provides a list of the recommended components for the NXP PMIC/MT2712 power solution defined in Section 5 "Schematic". The components listed here are shown with representative part numbers; they can be substituted with equivalent parts.

Table 4. Bill of Materials

Value	Qty	Part Number	Description	Vendor	Component
	1	PF81	Power management IC	NXP	PMIC
	1	PF5024	Power management IC	NXP	PMIC
0.22 µF	1	GRT155C81E224KE01	25 V 10% X6S 0402	MURATA	Output capacitor
1.0 µF	9	GCM155C71A105KE38D	10 V 10% X7S 0402	MURATA	Input capacitor
2.2 µF	1	GRT155C71A225KE13	10 V 10% X7S 0402	MURATA	Output capacitor
4.7 µF	15	GRT188C81E475KE13	25 V 10% X6S 0603	MURATA	Output capacitor
0.1 µF	20	GCM155R71C104KA55D	16 V 10% X7R 0402	MURATA	Input and Output capacitor
22 µF	22	GRT21BC81A226ME13	10 V 20% X6S 0805	MURATA	Output capacitor
1.0 µH	14	TFM252012ALMA1R0MTAA	4.7 A 20% SMD	TDK	Output inductor

7 Reference Resource

PF5024

[1] PF5024 Data Sheet and Application Note

[2] OTP configuration tool and Flex GUI

[3] EVM board PCB and schematic

PF8100-PF8200

[4] PF8100-PF8200 Documentation (Data Sheet, Application Notes, Errata, etc.)

[5] OTP configuration tool and Flex GUI

[6] EVM board PCB and schematic

PF56

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[8] Power Management community

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