AN12710

Layout recommendation for battery cell controllers

Rev. 2 — 19 April 2023 | Application note

Document information

Information	Content
Keywords	MC33771B, MC33771C, MC33772B, cell controller, Battery Management System, BMS
Abstract	This document provides guidelines for the layout and EMC robustness of the MC33771B, MC33771C, MC33772B cell controllers used in Battery Management System applications.

Revision history

Rev	Date	Description
2	20230419	• Updated security status from "Company confidential" to "Public". • Added Keywords and Abstract • Added Revision history
1	20200218	Initial version

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

1 Introduction

This application note provides guidelines for the layout and EMC robustness of the MC33771B, MC33771C, MC33772B cell controllers (referred to MC3377x in this document) used in Battery Management System applications. The device performs ADC conversions of the differential cell voltages and current, as well as battery coulomb counting and battery temperature measurements. The information is transmitted to MCU using one of the microcontroller interfaces (Serial Peripheral Interface (SPI) or Transformer physical layer (TPL)) of the IC.

The Battery Cell Controller measures cell voltages, temperature and current with high precision in mV and uV in a noisy automotive environment.

This document is intended to provide generic and specific recommendations for the battery cell controller MC3377x and tips for hardware developers and PCB designer to meet the automotive ISO and OEM's EMC requirements.

This layout recommendations have been realized on the EVB boards. The boards have successfully passed the validation, tests include the automotive EMC BCI test based on the ISO 11452-4. Test severity level IV and the IEC61000-4-2 and ISO10605 ESD tests

The design of the EVB board is a compact design with a two-sided component placement.

The recommendations in this document are also valid for a one-sided component placement and different shapes and dimensions of a PCB and connector pin assignments.

© 2023 NXP B.V. All rights reserved.

2 PCB recommendations

2.1 Layer architecture

NXP recommends to use a four-layer PCB design, FR4 PCB with 35µ copper,

A compact design is met with a two-sided placement on top and on bottom of the PCB.

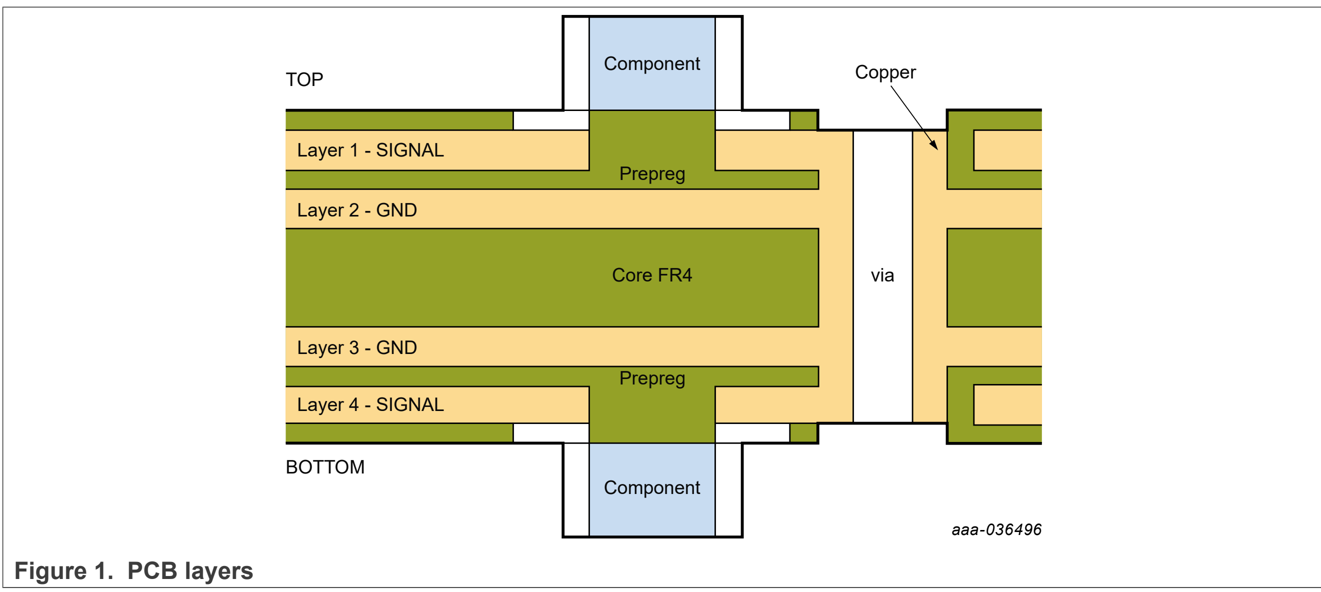


Figure 1. PCB layers

As we have placed the components on top and on bottom, we have to use Layer 1 and Layer 4 for signal routing. Layer 2 and Layer 3 are used exclusively for the ground planes. The parasitic capacitance between Layer 1 and Layer 2 and between layer 3 and Layer 4 will improve the EMC performance significantly. Requirements for the ground planes have to be met (see section Ground planes).

To improve the EMC and ESD performance, NXP recommends to fill the unused areas on the top and bottom layers with ground planes. Requirements for the top and bottom filled GND planes have to be met. See Section 3.1.

2.2 PCB zones for placement

A good design starts with a good placement. NXP recommends separating the PCB into different zones. Then, place the components into these zones related to the function in the design.

Zone 1: Battery Cell Controller MC3377x

Zone 2: Filtering components

Zone 3: ESD protection

Zone 4: Isolation (transformer or capacitor isolation)

Zone 5: Cell balancing resistor with high power dissipation

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

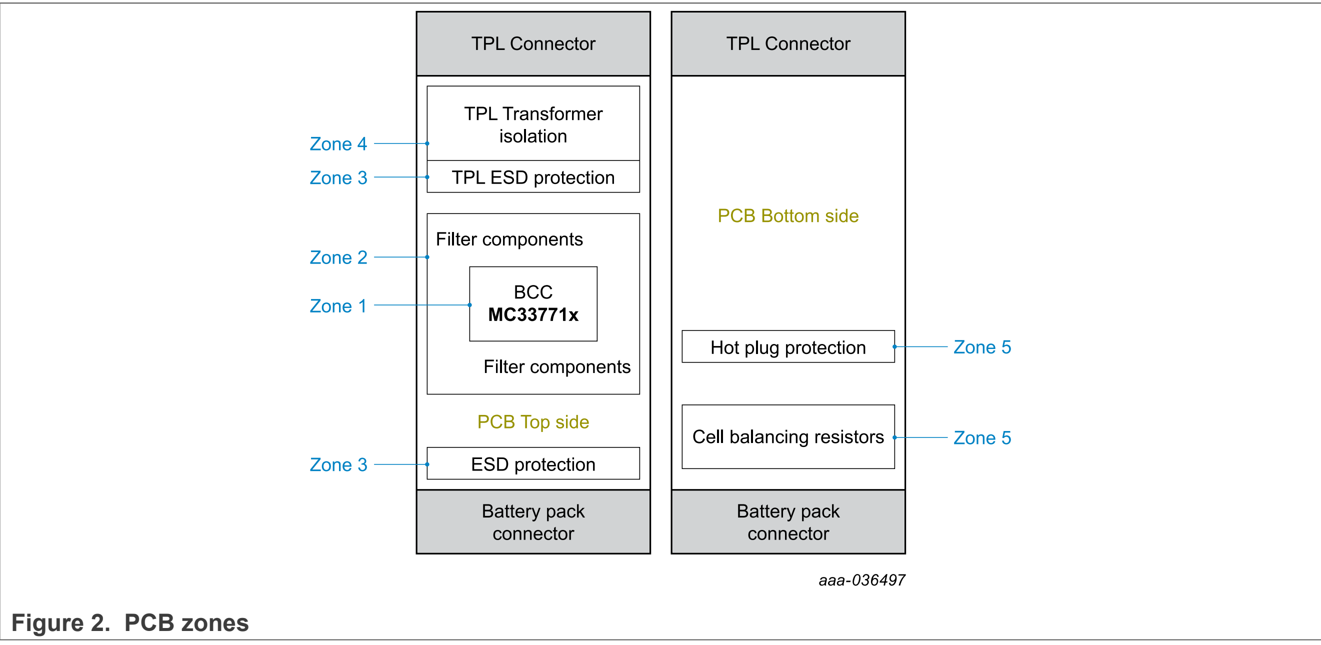


Figure 2. PCB zones

Table 1. Overview of component placement in zones

	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5
BCC MC3377x	X				
Cell LPF Filter		X			
Cell differential Filter capacitors		X			
TPL Filter capacitors		X			
NTC LPF filter		X			
Current sense filter		X			
VCOM decoupling capacitor		X			
VANA decoupling capacitor		X			
VPWR decoupling capacitor		X			
ESD capacitors (CT)			X		
ESD capacitors (GPIO/NTC)			X		
TPL TVS Diodes ESD			X		
TPL Transformer				X	
Z-Diodes (Hot plug protection)					X
Balancing resistors					X

2.2.1 Zone 1: Battery cell controller MC3377x

Do not route any signals across the BCC exposed pad or the layers below. Instead, fill the area under the BCC with a ground plane. Thermal vias significantly improve the thermal properties of the BCC. See Figure 3 and the data sheet for footprint recommendations [1].

© 2023 NXP B.V. All rights reserved.

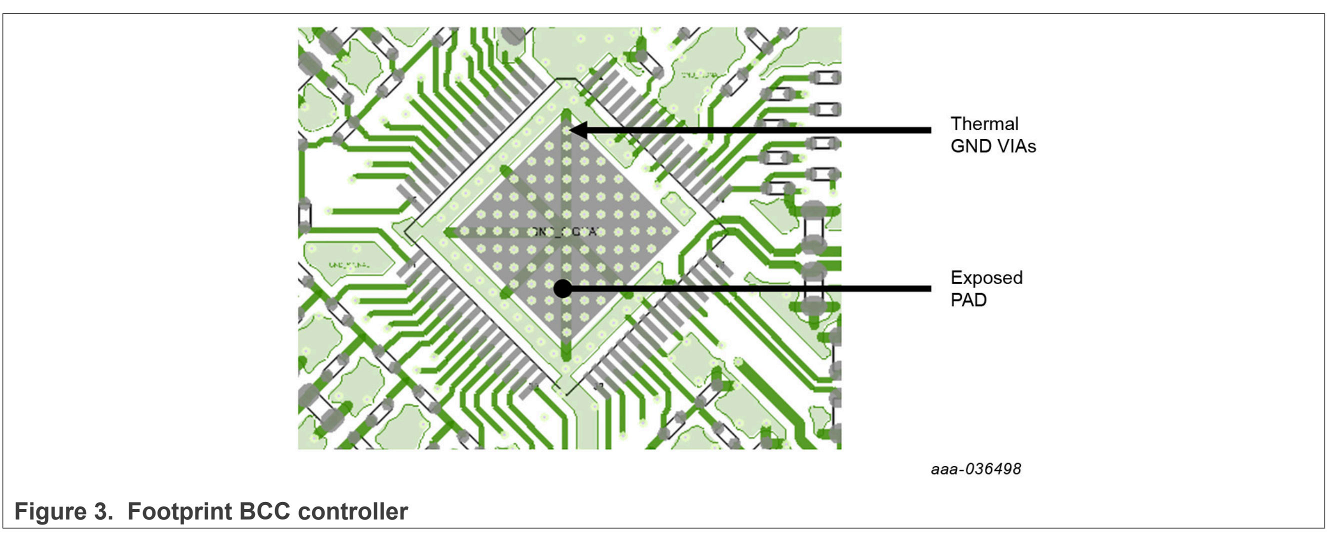


Figure 3. Footprint BCC controller

2.2.2 Zone 2: Filtering components

Clear structure is necessary. Filtered and unfiltered signals should not be mixed. Keep a distance between the filtered and unfiltered signals to avoid HF noise coupling to the filtered signals.

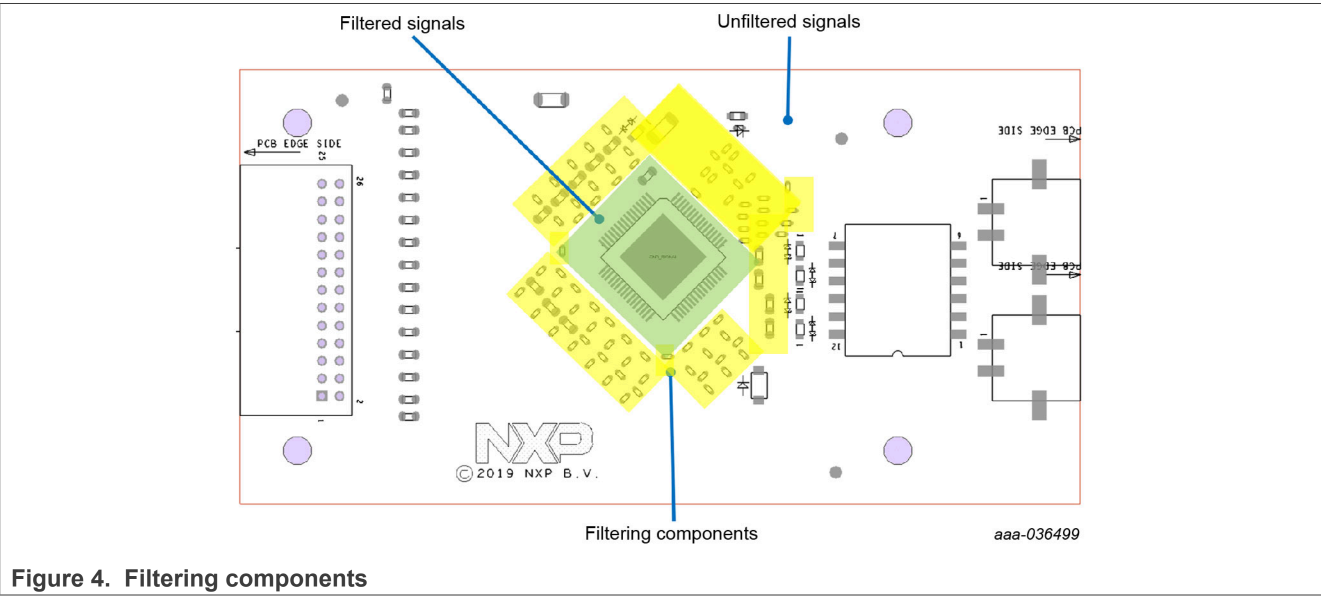


Figure 4. Filtering components

2.2.3 Zone 3: ESD protection

ESD protection components have to be placed as close as possible to the connectors. This is where the ESD pulse will typically enter into the PCB.

As the ground reference for the differential TPL signals is not available on the TPL connectors, the ESD TVS protection diodes could not be placed close to the connector and protect for ESD pulse at that position. In this case the ESD TVS diodes are placed close to the transformer (outputs/inputs) pins between the transformer and the BCC, where a ground is available to connect the TVS to ground.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

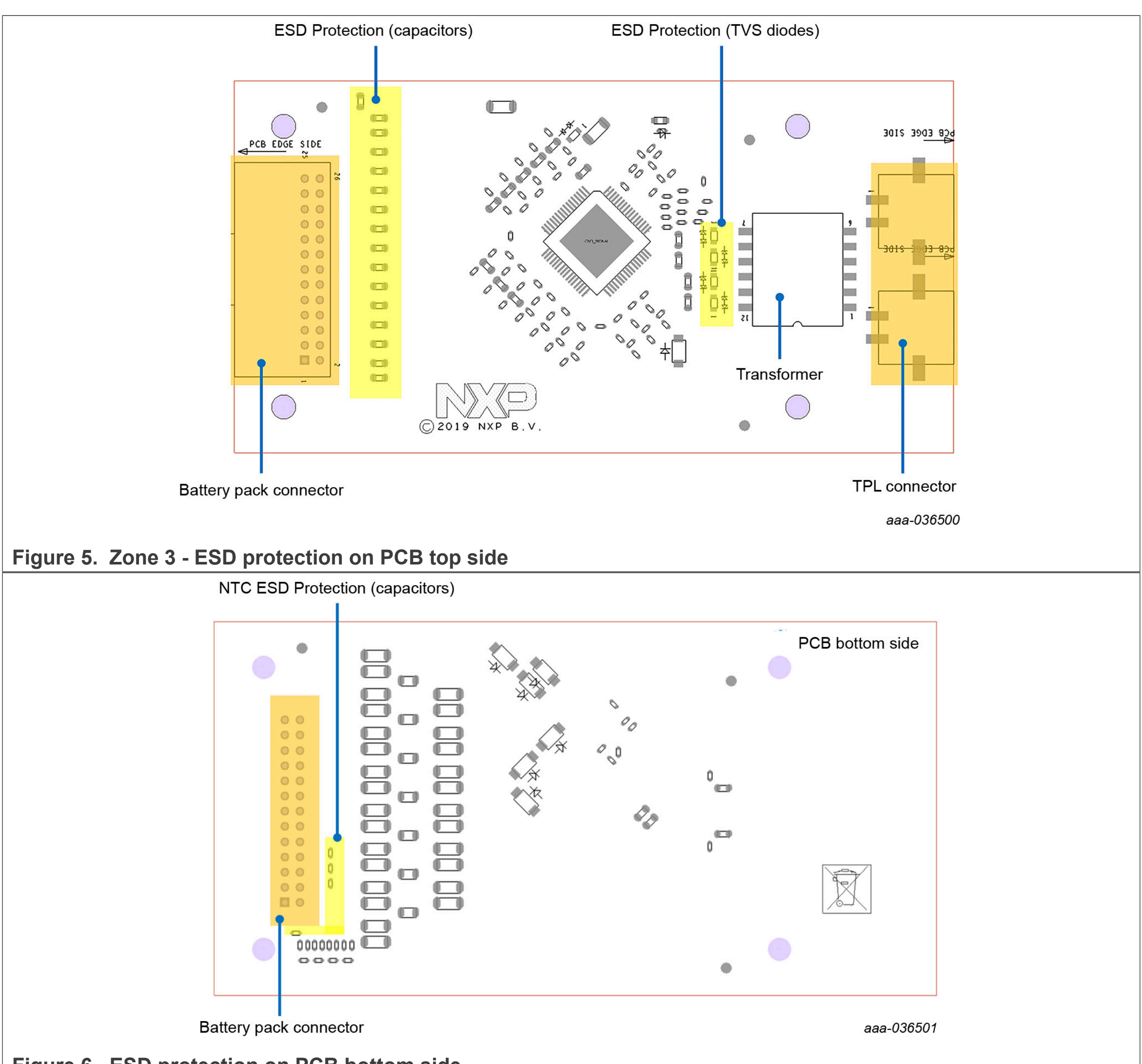


Figure 5. Zone 3 - ESD protection on PCB top side

Figure 6. ESD protection on PCB bottom side

2.2.4 Zone 4: Isolation (transformer or capacitor isolation)

Related to the system voltage, maintain the required creepage distance related to your design isolation requirements between the input and output of the transformer. The creepage distance and isolation coordination are described in IEC60664. Keep the isolated and non-isolated signals with the required distance separated in all layers and avoid HF coupling between both galvanic isolated voltage signals.

© 2023 NXP B.V. All rights reserved.

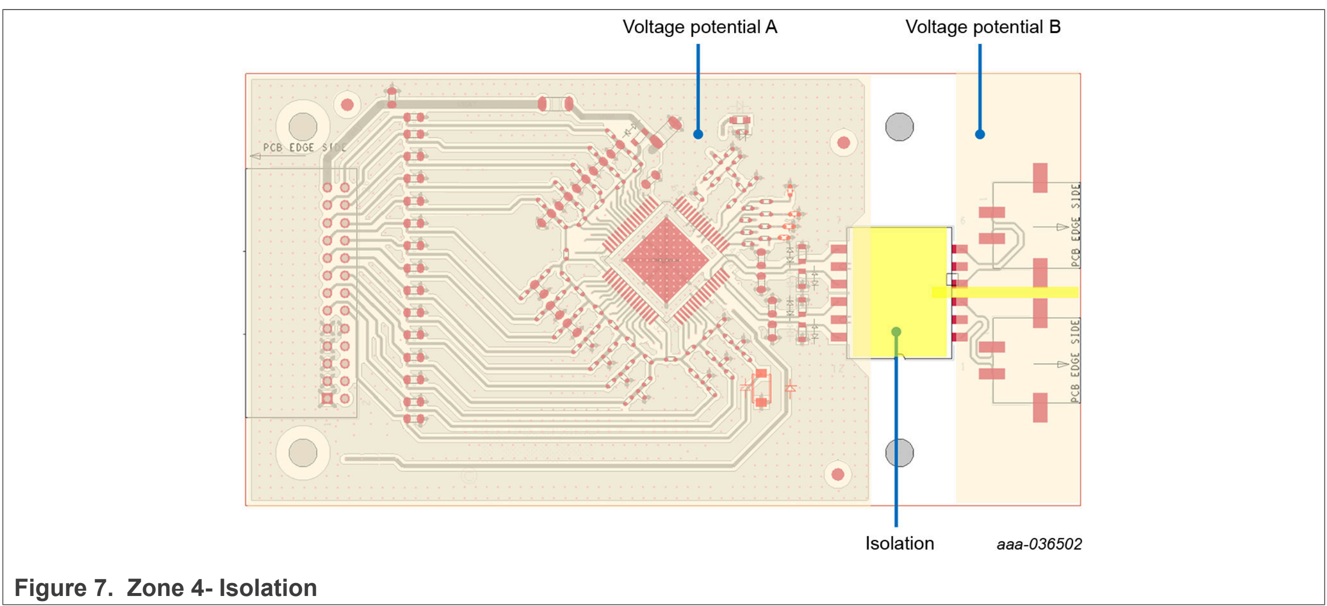


Figure 7. Zone 4- Isolation

When considering capacitor isolation in centralized solutions, it is recommended to use two capacitors in series. The capacitors have to be placed on each board close to the TPL connector. The capacitor voltage has to be selected to meet at least the system voltage. Select the right capacitor with the required creepage distance. It is possible to place an air gap to increase the creepage distance in the PCB under the capacitor or select a capacitor with a bigger package.

Note: *The bigger the package, the higher the risk for cracking.*

2.2.5 Zone 5: Components with high-power dissipation

NXP recommends placing any components with high-power dissipation into this zone. This includes balancing resistors.

If current sense is used, thermoelectrical effect can cause a voltage drift. This is especially true for the µV current sense measurement when the ends of their filtering resistors will see two different temperatures. A detailed description of this is in Section 3.12.

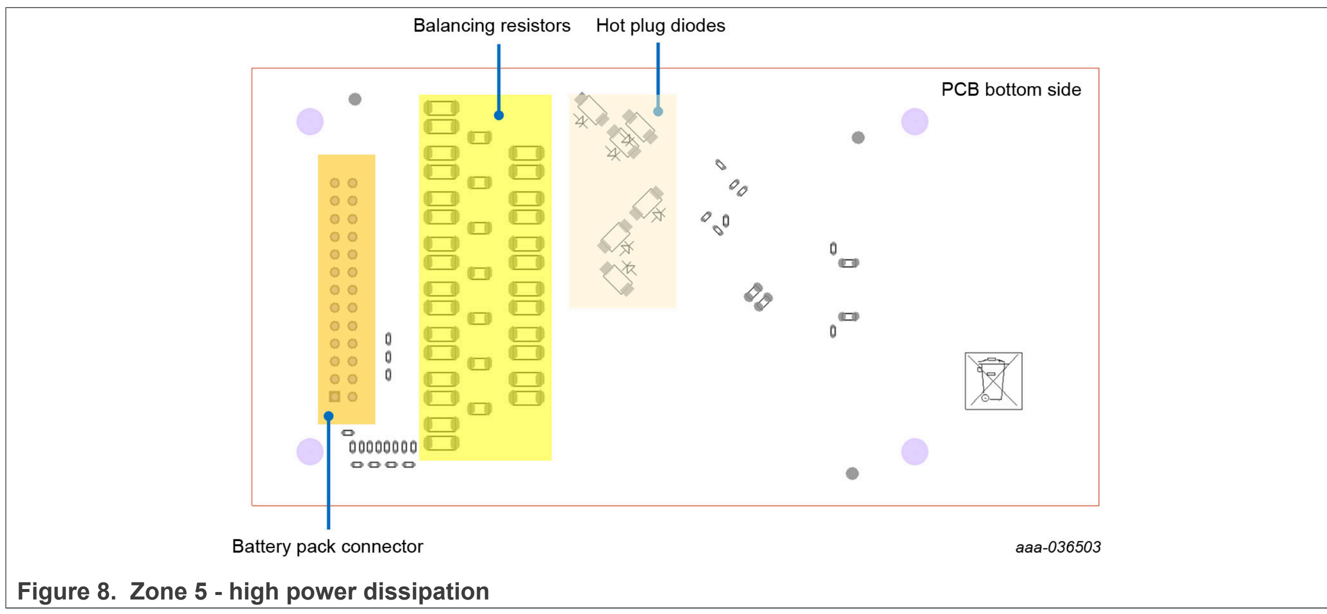


Figure 8. Zone 5 - high power dissipation

© 2023 NXP B.V. All rights reserved.

3 Circuit and layout parts

3.1 Ground planes

Ground planes have a very high impact on the EMC performances, such as RE/RI, and have to be implemented carefully. The ground plane must meet the following requirements:

- Use only one ground plane for the digital and analog circuit parts.
- Do not route any track/trace through the ground plane.
- Avoid large gaps in the ground plane. Most gaps are caused when several vias are placed too close to each other. This design prevents filling the ground around each via. To avoid this, maintain more than 0.45 mm of clearance between vias.
- Connect the ground planes together with vias as much as you can. Every 2 mm is sufficient. This will reduce the ground impedance and improves the EMC performance.

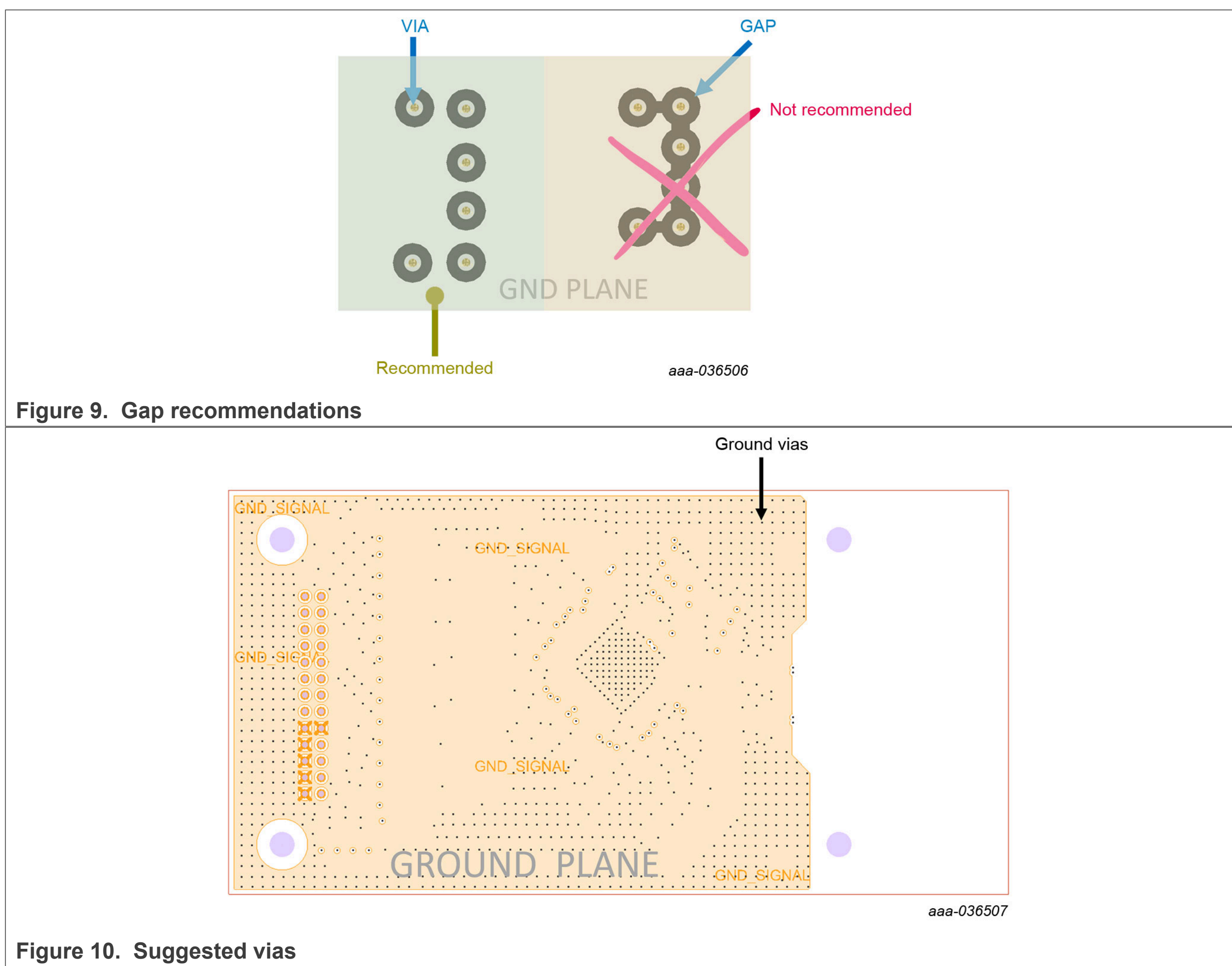


Figure 9. Gap recommendations

Figure 10. Suggested vias

3.2 Power planes

Power planes are not recommended for this kind of design and will not significantly improvement performance. Use a ground plane instead.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

VPWR and VCOM tracks can be routed with the standard tracks. Increasing the width of the tracks will reduce the voltage drop and increase the accuracy.

Note: *Decoupling capacitors have to be placed in the recommended positions (see VCOM and VPWR)*

3.3 ESD capacitors

The ESD capacitors should have the capability to absorb the ESD discharge pulse energy.

Place the ESD capacitors as close as possible to the connector pins. Route the tracks from connector pin to the ESD capacitor with a low impedance first. Then, route the tracks from the capacitor pads to the rest of the circuits on the PCB.

The capacitors have to be connected to the ground plane in the inner layer with as low impedance as possible. Using two vias instead of only one will increase the EMC and ESD performance. Connecting to a top or bottom ground plane is also possible.

Keeping the tracks as short as possible with a low impedance and low inductance between the connectors and the ESD capacitors will improve the ESD performance.

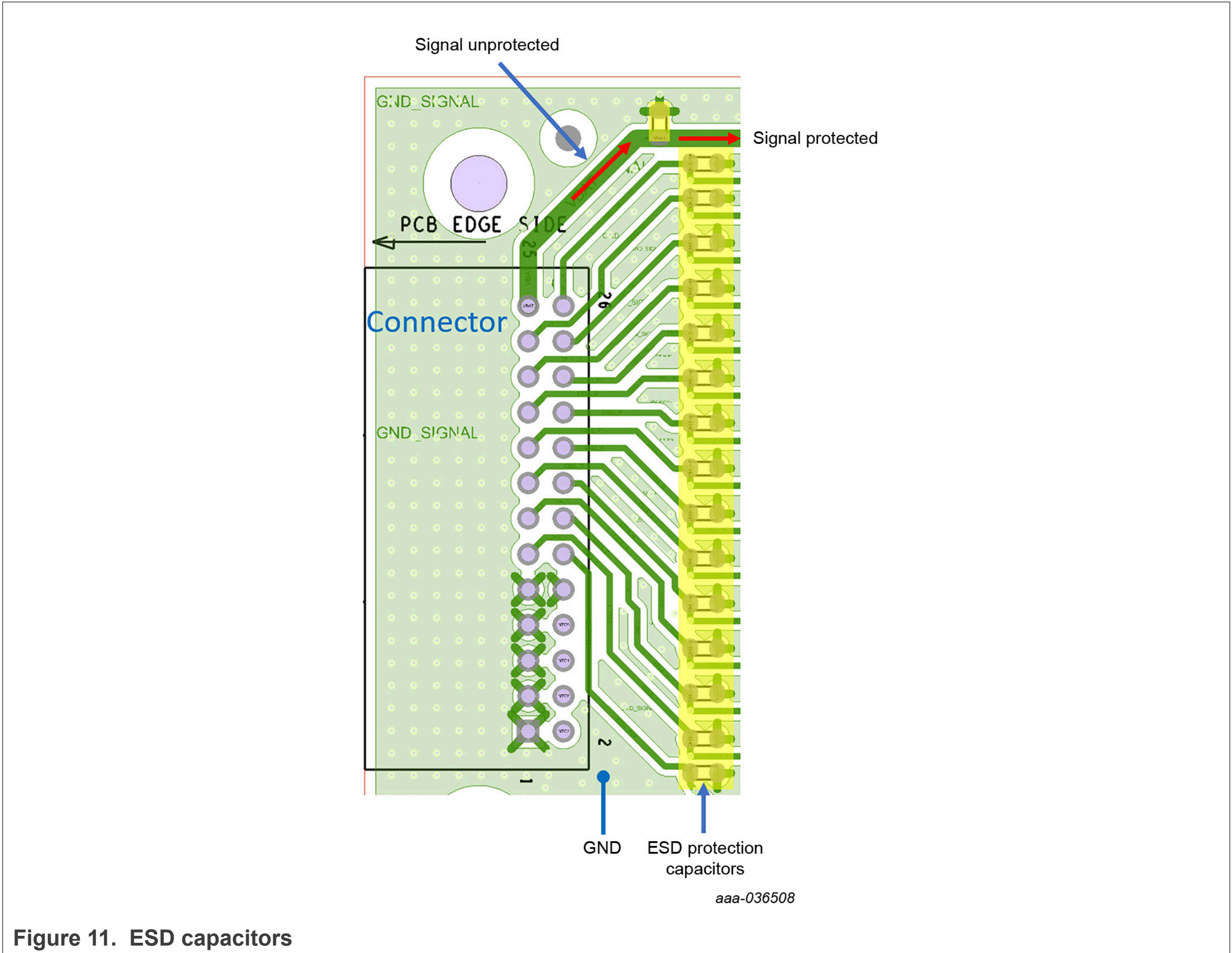


Figure 11. ESD capacitors

In automotive applications, some OEMs require the use of two capacitors, placed 90° from each other, in series on all cell terminal connections. This decreases the risk of short circuit if a crack in the capacitor occurs. In the RD33771CDSTEVB evaluation board, soft termination capacitors are used. Some OEMs recommend or require

© 2023 NXP B.V. All rights reserved.

using capacitor packages that are 0805 size or bigger. This increases the ESD performance and increases the creepage distance at sensitive positions.

3.4 Balancing resistors

The balancing resistors can be placed between the LPF Filter and the cell pack connector.

Do not place the cell balancing resistors close to the current sense LPF components, the thermoelectrical effect could cause a voltage offset of several μV of the current measurement.

Use sufficient cooling copper planes to absorb the temperature caused by the power dissipation generated on the balancing resistor. Place the cooling plane over a ground plane. PCB parasitic capacitance will increase the EMC performance.

3.5 Differential capacitors and LPF filter

Place the differential filter capacitors as close as possible to the BCC CTx pins.

The low-pass filter components have to be placed as close as possible to the BCC CT pins. After the low-pass filter, the signals should not cross unfiltered signals.

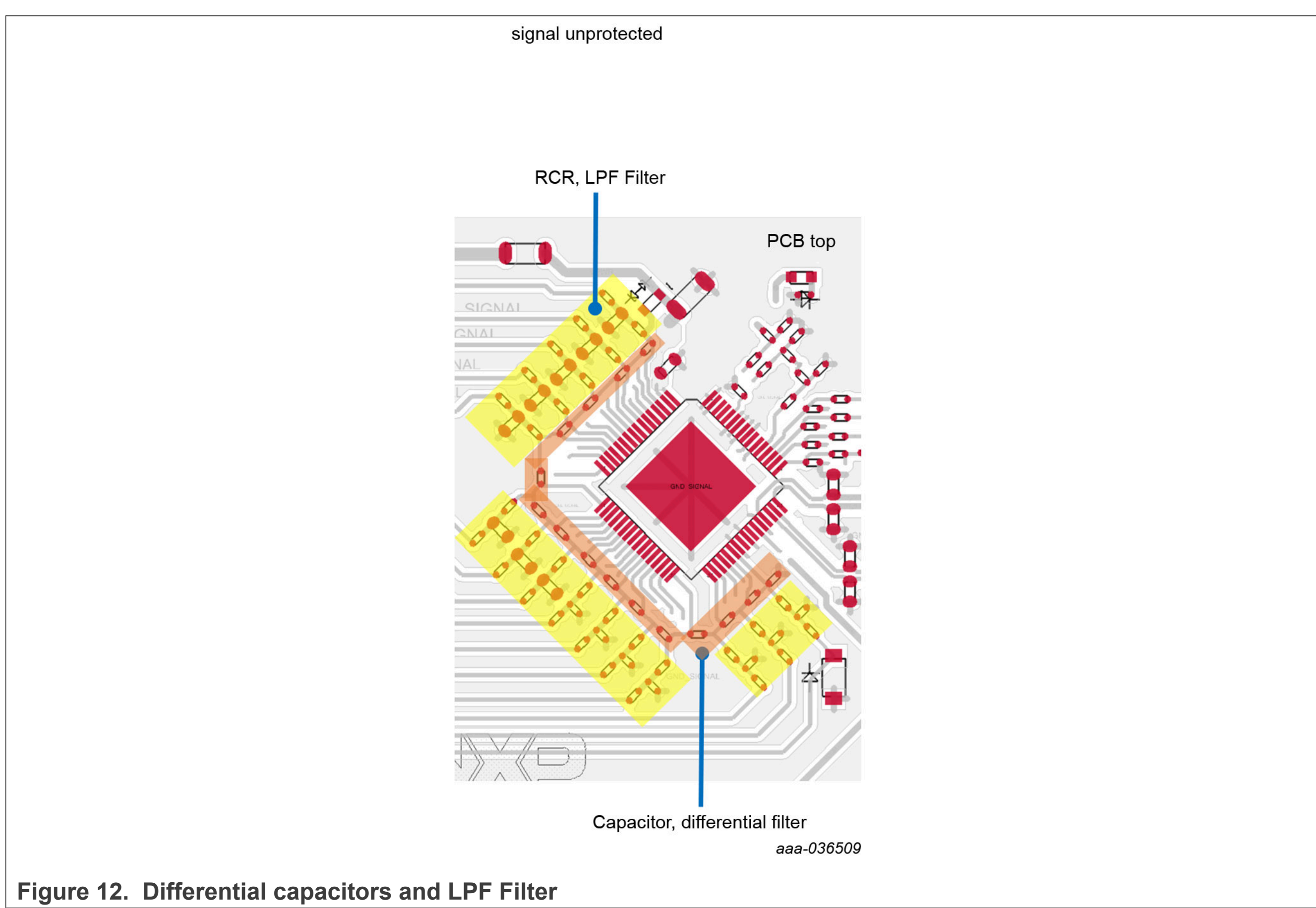


Figure 12. Differential capacitors and LPF Filter

3.6 VPWR capacitors

Place the VPWR decoupling capacitor with a short track as close as possible to the VPWR1 and VPWR2 pins of the BCC.

© 2023 NXP B.V. All rights reserved.

Keep a low impedance between the ground of the capacitor and the GNDREF pin of the BCC.

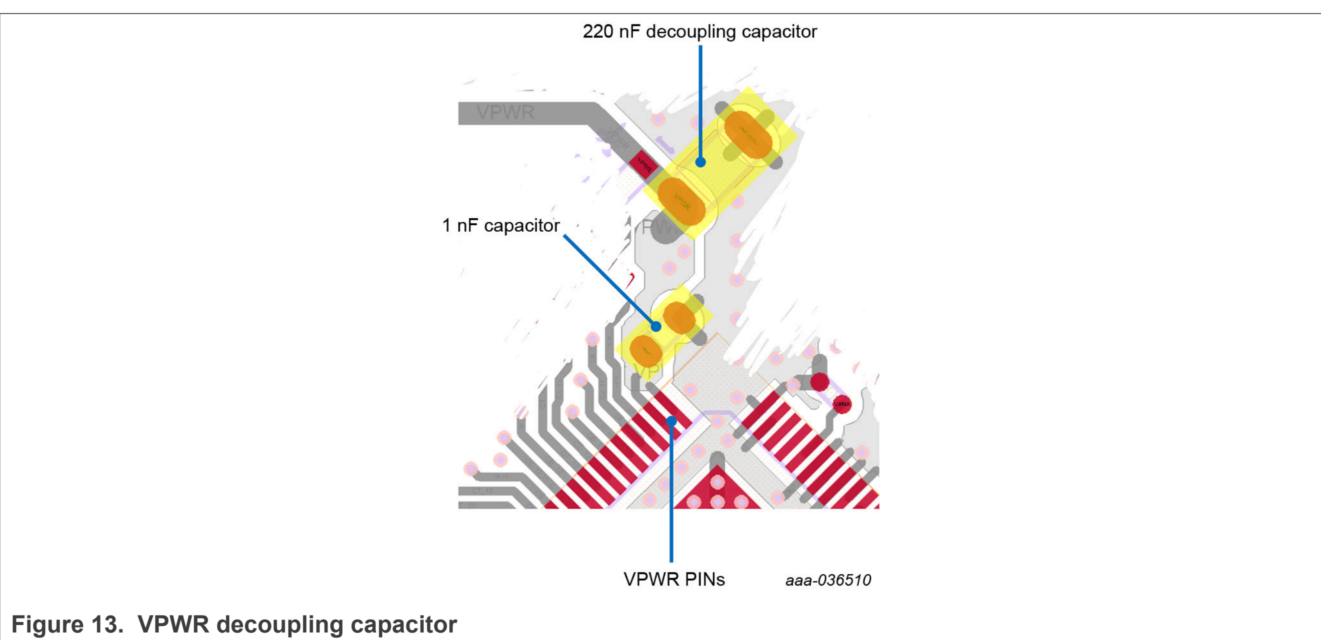


Figure 13. VPWR decoupling capacitor

3.7 VCOM

Place the VCOM decoupling capacitor as close as possible to the BCC VCOM pin.

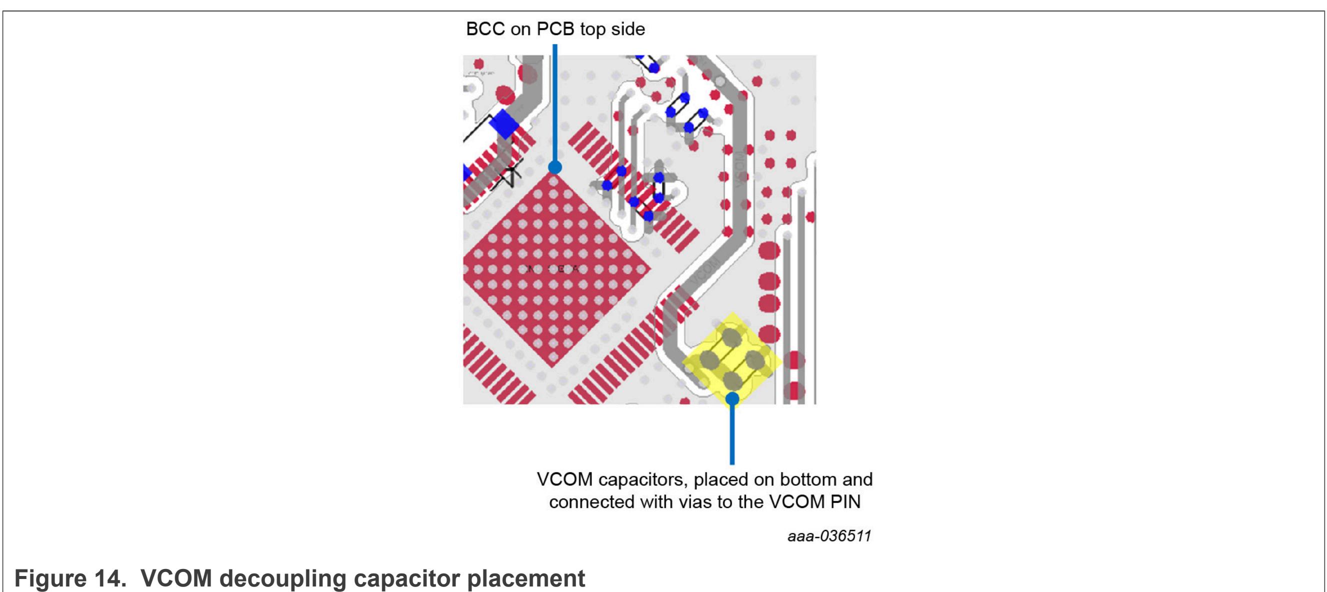


Figure 14. VCOM decoupling capacitor placement

3.8 GPIO and NTC filter

Place the low pass filter as close as possible to the BCC GPIO pins.

3.9 VANA

Place the decoupling capacitors recommended and listed in the data sheet as close as possible to the VANA pin of the battery cell controller MC3377x.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Keep a low impedance between the ground of the capacitor and the AGND pin of the BCC.

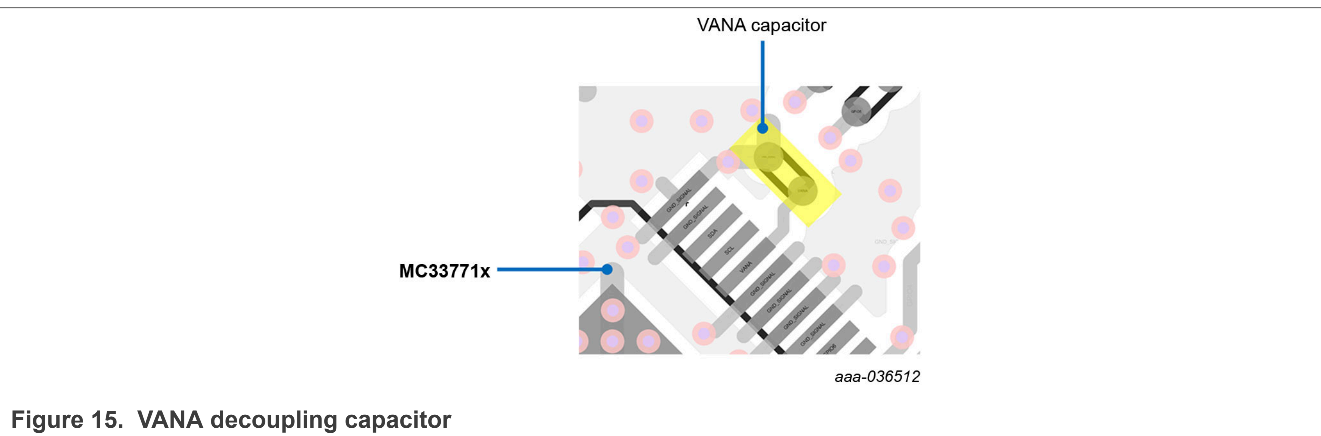


Figure 15. VANA decoupling capacitor

3.10 TPL

Place the TPL capacitors close to the TPL pins. Place the ESD protection TVS diode close to the transformer.

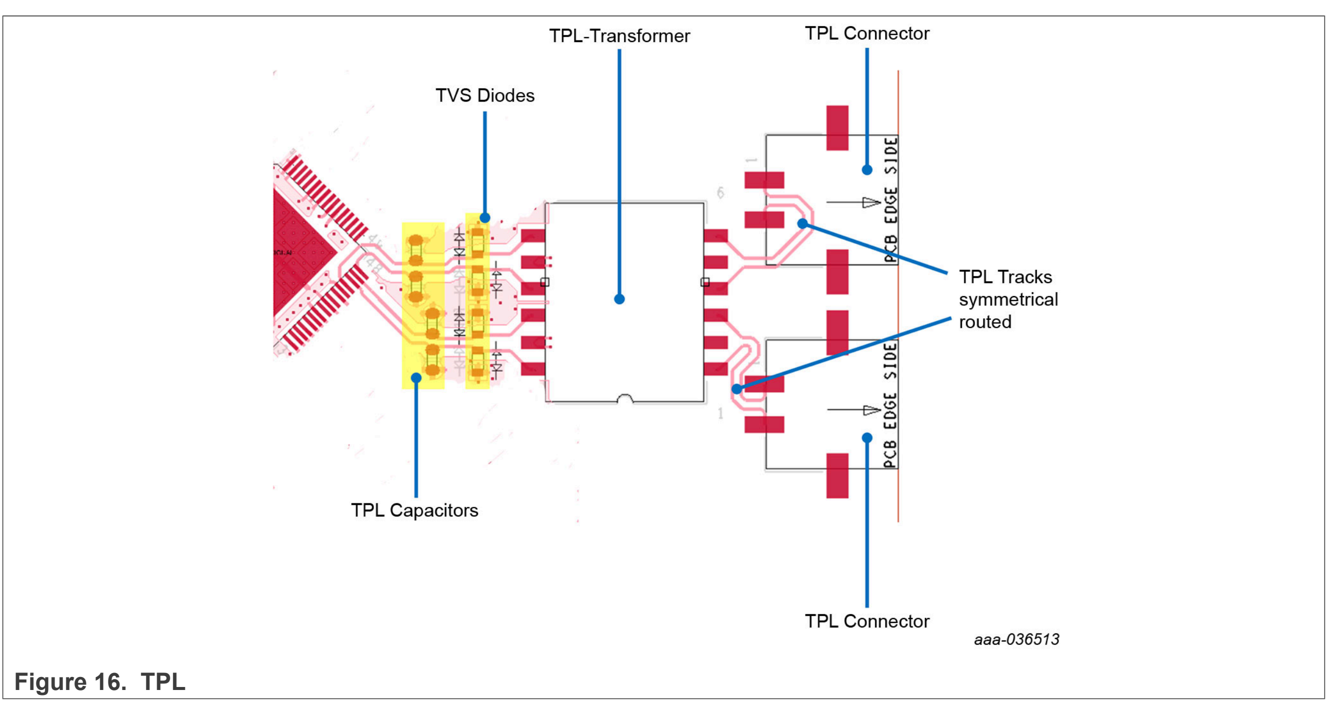


Figure 16. TPL

The 2 MHz TPL communication is a differential (high and low) two-wire signal and must be symmetrically routed on one layer to avoid decreasing of the signal quality.

Routing of the TPL tracks over a ground plane improves the EMC performance. This design reduces radiated emission.

Related to measurements, uncontrolled impedance for short tracks does not decrease the TPL performance.

It is recommended to not cross filter analog signals with the TPL tracks. Keep distance between the high-speed digital and the high-sensitive analog measurement signals, such as the current sense tracks.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

3.11 Hot plug protection

It is recommended to place the hot plug protection Zener diodes close to the CB signals on the bottom side of the PCB.

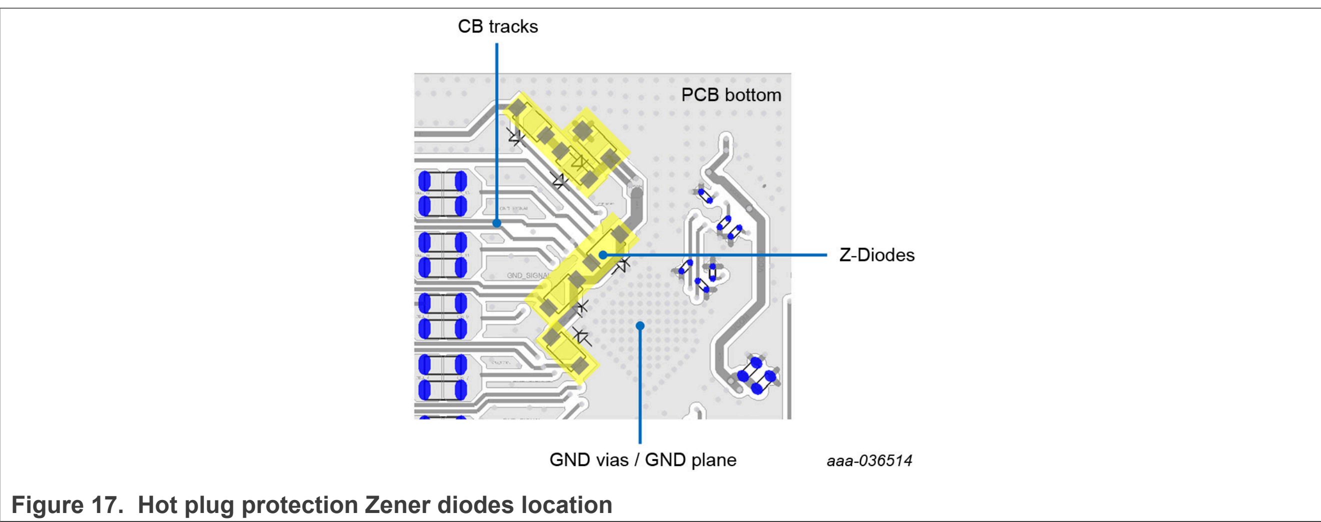


Figure 17. Hot plug protection Zener diodes location

3.12 Current sense

The current measurement is the most sensitive measurement on the board. The load current on the 100 μΩ shunt will cause a voltage drop across the 100 μΩ shunt and will be monitored from the BCC.

For example, for a load current of 1 A, 100 μV will be dropped across the shunt and will be measured with high accuracy from the battery cell controller. For a 100 mA load, 10 μV will be measured and for 10 mA, 1 μV will be measured.

To meet high accuracy in a noisy environment, NXP recommends the following:

- Place the LPF filter as close as possible to the current sense inputs of the BCC
- Route the current sense+ and current sense– tracks as symmetrical as possible.
- Route the tracks over a ground layer or shielded between two ground layers.
- Avoid a thermoelectrical effect by placing the components for the current measurement with a sufficient distance from components generating heat, such as the balancing resistors.
- Keep distance from high-noise signals, such as the unfiltered cell terminal tracks.
- If the shunt is connected through wires with the BCC, use twisted pair wires.
- Using a common mode choke or ferrite beads will reduces HF noise, depending on the EMC requirements, performance and design.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

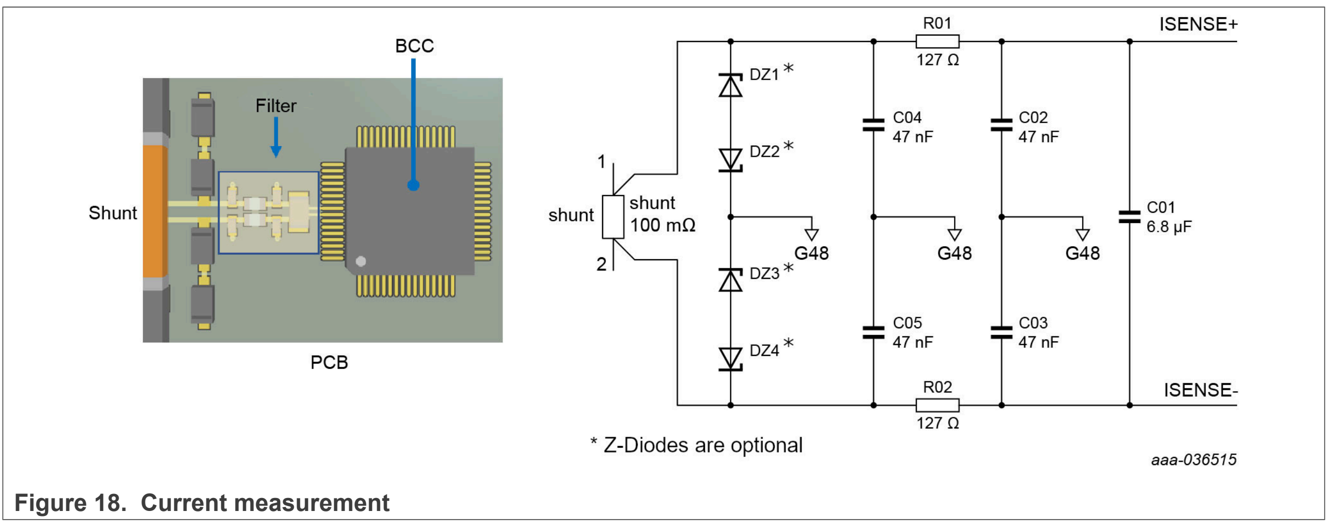


Figure 18. Current measurement

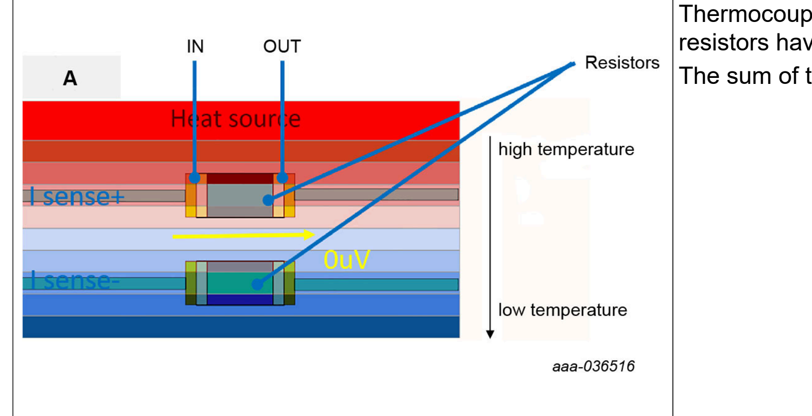
3.12.1 Thermocouple effect EMF

The conversion of heat directly into electricity at the junction of two different types of materials is called the *thermocouple effect*, also known as the *Seebeck effect*. A small amount of voltage is produced between the two materials. The change of the produced voltage with the temperature from the intermetallic junction is a function of the metallic combination of the contact of the two materials. Depending on the temperature differences, direction and contact materials, positive or negative voltages can be produced.

The thermocouple effect impacts the sensitive current measurement; several µV will cause a current drift of tens of mA.

To avoid or minimize the thermocouple effect on PCBs, the filtering resistors have to be placed in a position where both resistor ends are exposed to similar temperatures. See image A. Resistors have to be placed horizontal and in parallel to the heating source. Vertical placement and in parallel to the heat source has to be avoided as the thermocouple effect will be significantly increased. See image B. Differential voltage measurements that are used for the current measurement might not cause a voltage drift if the two resistors are placed symmetrically and produce the same thermocouple voltage.

Unsymmetrical placement (image C) of filter resistors in different temperature zones on a PCB causes a voltage drift in a differential measurement. The amount of drift is a function of the temperature difference on the resistor ends and the different resistor material connected together in the resistor. The thermocouple effect is also present in the solder point as two different materials are connected together (copper and a mixture of solder tin).

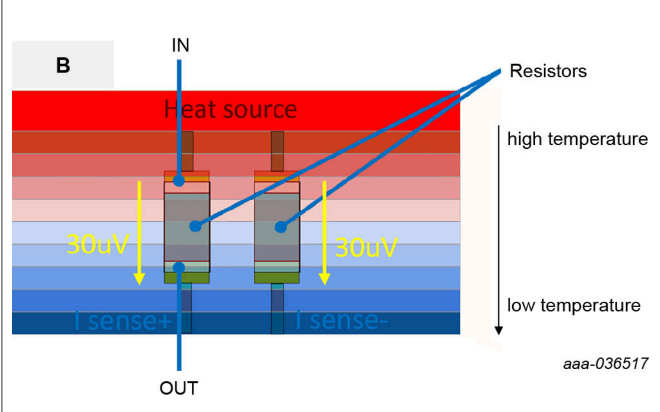
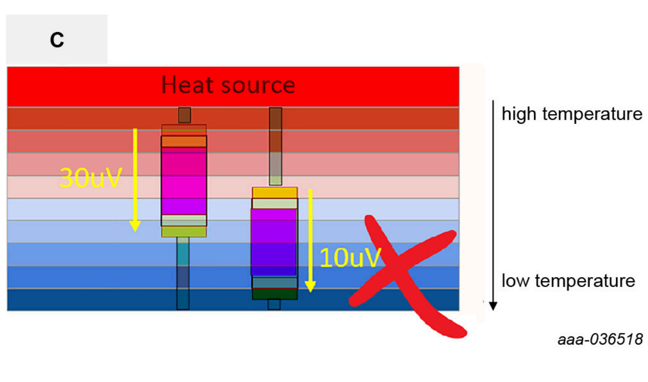


Thermocouple effect has no impact as both ends of the resistors have the same temperature.

The sum of the produced voltage is ~0 µV

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

	Thermocouple effect produces 30 µV voltage drop over the resistors. As in this example, both resistors are placed symmetrical over the different temperature zones. The produced voltage drop on both resistors is the same. The differential current measurement is 0 µV as a difference between Isense+ and Isense–.
	Thermocouple effect produces two different voltage drops on the resistors, as each resistor is placed over a different temperature zone. In this example, the current measurement measures a voltage difference of 20 µV. This will cause an offset current of 100 µR shunt of 200 mA.

© 2023 NXP B.V. All rights reserved.

4 Reference design EVB board RD33771CDSTEVB

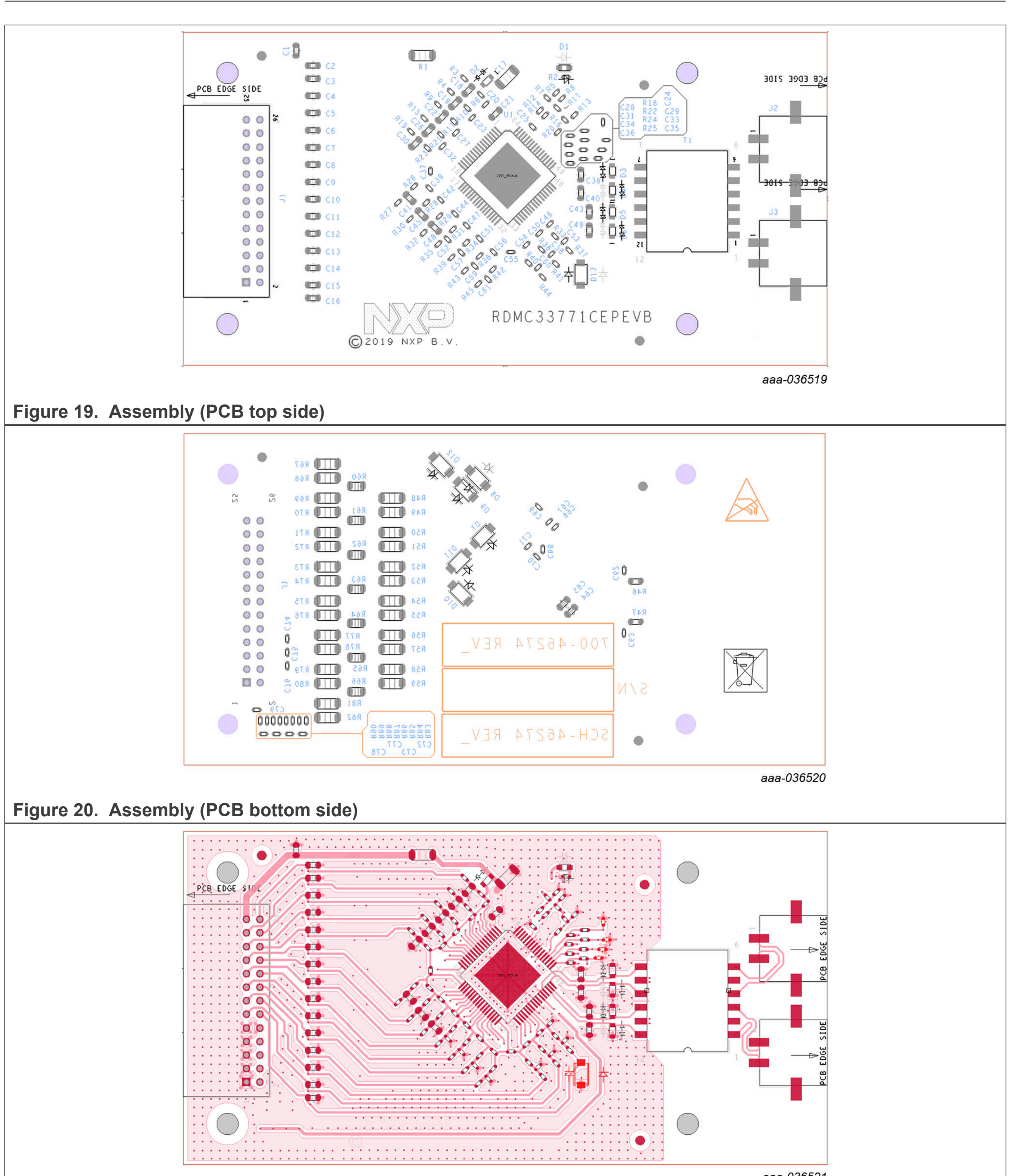


Figure 19. Assembly (PCB top side)

Figure 20. Assembly (PCB bottom side)

Figure 21. Layer 1 (PCB top side)

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

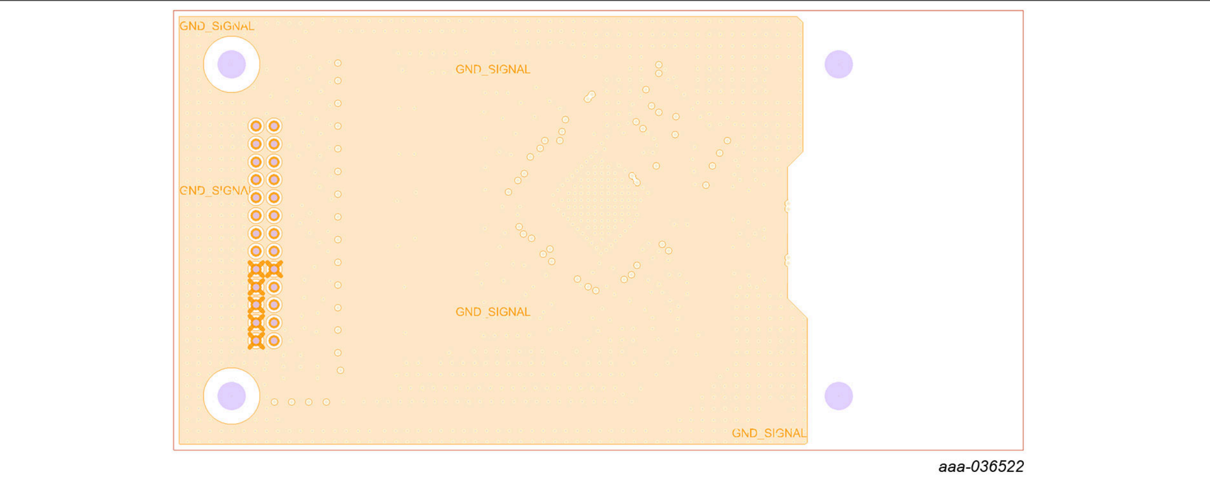


Figure 22. Layer 2 (1st inner layer)

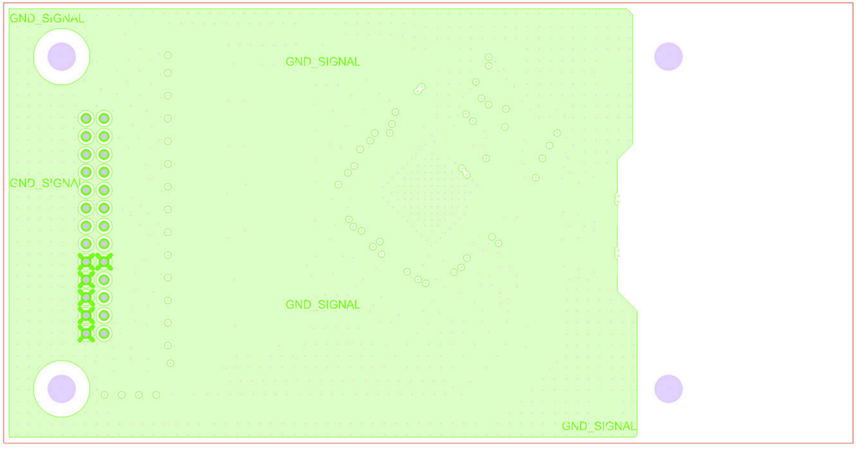


Figure 23. Layer 3 (2nd inner layer)

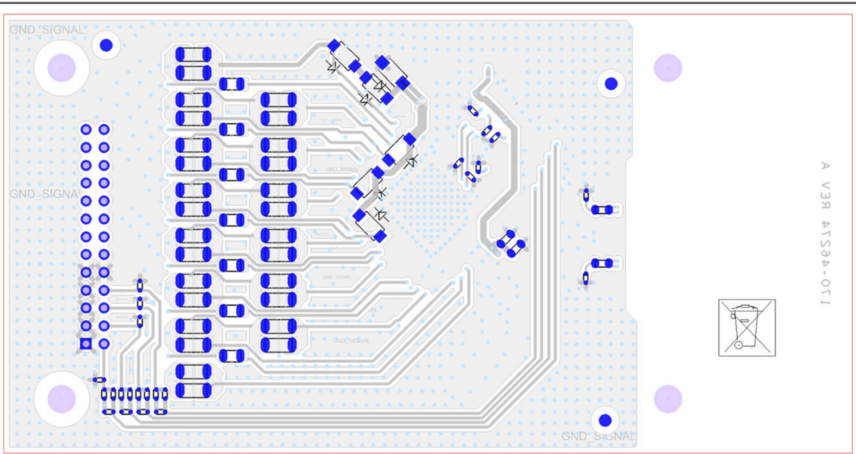


Figure 24. Layer 4 (bottom side)

© 2023 NXP B.V. All rights reserved.

5 EMC tests

These recommendations were implemented in several boards and have been successfully validated, related to the following standard automotive EMC Test specifications.

- RE (Radiated emission) test
- CP test (Conducted disturbances - Current probe method related to CISPR25
- BCI test related to the ISO 11452-4 Test level IV
- ESD test related to ISO10605 and IEC61000-4-2

This capture focuses on the most relevant general EMC requirements such as the conducted Immunity and the radiated emission. Detailed EMC test requirements and test setups are described in the CISPR25, ISO and in the OEM EMC requirements. Detailed EMC test reports are available and can be requested from NXP.

5.1 RE (Radiated Emission) test

Because the BCC includes a high-speed communication interface, an amount of radiated emission is measured, especially in the lower frequency ranges below 100 MHz. The TPL routing and filter and the decoupling components, such as the TPL capacitors and the common mode chokes etc. on the TPL lines, have a high impact on the radiated emissions.

The RE test has been successfully completed, related to the CISPR25 in the frequency range from 150 KHz up to 2.5 GHz, class 5.

This board has also passed advanced EMC tests premium OEM EMC test requirements in frequency ranges up to 6 GHz.

5.2 CP Test, (Conducted disturbances - Current probe method related to CISPR25

The conducted disturbance from the EVB board has been measured with the current probe method related to the CISPR25. The measured conducted emissions were always under the defined limits in the CISPR25.

The current probe measurement method has been used on six different positions.

- Position P1: On all CT and NTC signal wires together
- Position P2: Only on HV+ (Battery pack plus busbar/wire)
- Position P3: Only on HV– (Battery pack minus busbar/wire)
- Position P4: HV+ and HV– put together in the bulk injection probe
- Position P5: Only on TPL input wires
- Position P6: Only on the TPL output wires

The current probe has been placed at the distances described test setup in the CISPR25 standard

5.3 BCI (Bulk Current Injection) test related to ISO 11452-4

For battery management systems, the BCI test is one of the most important tests. This test simulates the EMC noise on vehicle level coupled into the board net and to the battery HV+ and HV– and to all harnesses and wires that are connected to the CMC / BMS boards. On the vehicle, DCDC converters and the motor inverter typically cause high EMC noise in the low frequency ranges. This EMC noise can disturb all sensitive measurements (voltage, current, temperature) in the BCC and interrupt the 2-wire differential TPL communication.

The board and its layout in the data sheet specified filters have been successfully tested related to the international ISO 11452-4 standard and to some premium OEMs standards and requirements. In the whole Test-Frequency range (100 KHz) 1 MHz to 400 MHz the CT and GPIO accuracy was within the pass criteria. Communication error/loss and fault are part of our failure criteria.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

The injection probe has been put in six different positions in a simulated Li-Ion battery pack. See drawing below. related to the test setup described in the ISO11452-4.

For all positions, the stand substitution method has been used and the injection probe has been placed at the three distances from connector to the DUT described in the ISO11452-4. Close loop method has been also successfully tested for a specific customer allocation and related to their test setup and acceptance criteria.

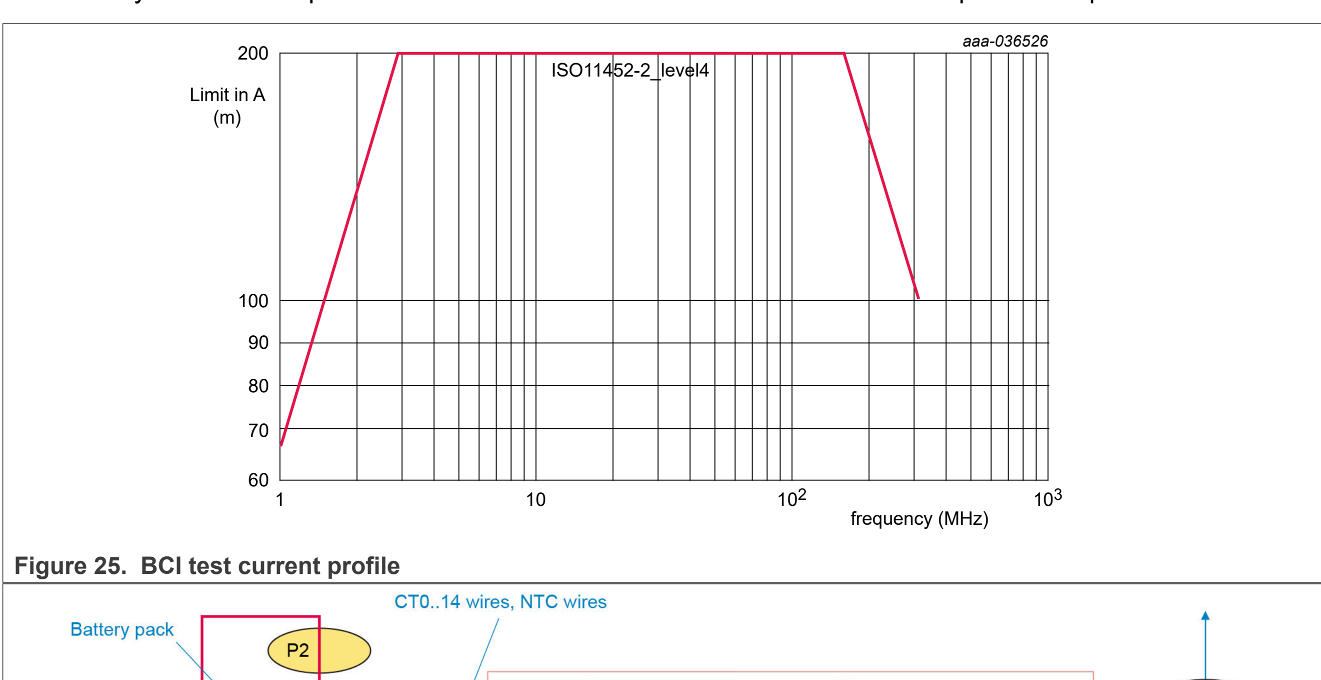


Figure 25. BCI test current profile

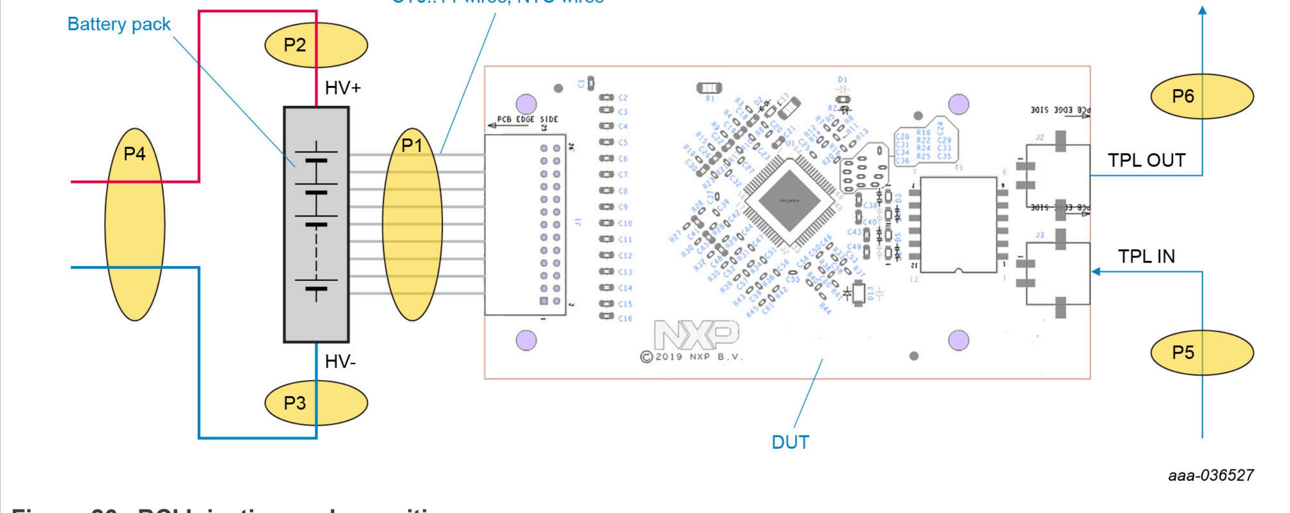


Figure 26. BCI Injection probe positions

The Injection probe has been placed on 6 different positions

Position P1: On all CT and NTC signal wires together

Position P2: Only on HV+ (Battery pack plus busbar/wire)

Position P3: Only on HV- (Battery pack minus busbar/wire)

Position P4: HV+ & HV- put together in the bulk injection probe

Position P5: Only on TPL input wires

Position P6: Only on the TPL output wires

On each position, the injection probe has been placed at the three distances that are defined in the ISO11452-4.

All information provided in this document is subject to legal disclaimers.
© 2023 NXP B.V. All rights reserved.

5.4 ESD Test related to ISO10605 and IEC61000-4-2

Electrostatic discharge pulses are simulated to each pin of the connectors. This is to test the robustness of the sensitive signals and functions of the BCC, related to IEC61000-4-2 and the ISO10605 automotive standards.

The relevant direct discharge method has been used. ESD discharge pulses up to 8 KV have been tested with a network (330R/150 pF and 2KR/330 pF-150 pF) on all pins on the connector. This tests the effectiveness on the designed and routed ESD filter in different modes.

After the ESD tests, the BCC (IC) was soldered out from the board and inspected for any ESD (EOS) damage in the ESD structure. Malfunctions and damage in the silicon ESD structure were not detected.

The following direct discharge ESD tests have been executed

- Powered System with a network of 2KR/330pF/8KV
  - Acceptance criteria are all parameters within the limits of the specification
- Unpowered System with a network of 2KR/150pF/8KV and 330R/150pF/8KV
  - Acceptance criteria are all parameters within the limits of the specification

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

6 General information

A good design starts with good placement. NXP recommends separating the PCB into different zones and placing the components into these zones related to their function.

6.1 Coating

For battery management systems where cell voltages are permanently connected to the PCB, it is recommended to coat the assembled PCB. This process avoids leakage current in a humid environment. Water condensation usually leads to migration and short-circuits between signals that are connected permanently to the cell terminal voltages.

6.2 Layout standards

It is recommended to use the generic standard on printed board design IPC2221A.

NXP recommends using the international standard IEC60664 for the isolation, creepage and clearance distances.

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

7 References

[1] **MC33771C: 14-Channel Li-ion Battery Cell Controller IC** — https://www.nxp.com/products/power-management/battery-management/battery-cell-controllers/14-channel-li-ion-battery-cell-controller-ic:MC33771C

[2] **HLQFP64 package information** — https://www.nxp.com/docs/en/package-information/SOT1510-2.pdf

[3] **HLQFP48 package information** — https://www.nxp.com/docs/en/package-information/SOT1571-1.pdf

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

8 Legal information

8.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

8.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Suitability for use in automotive applications — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

8.3 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

© 2023 NXP B.V. All rights reserved.

Tables

Tab. 1. Overview of component placement in zones 5

All information provided in this document is subject to legal disclaimers.

© 2023 NXP B.V. All rights reserved.

Figures

Fig. 1. PCB layers 4
Fig. 2. PCB zones 5
Fig. 3. Footprint BCC controller 6
Fig. 4. Filtering components 6
Fig. 5. Zone 3 - ESD protection on PCB top side 7
Fig. 6. ESD protection on PCB bottom side 7
Fig. 7. Zone 4- Isolation 8
Fig. 8. Zone 5 - high power dissipation 8
Fig. 9. Gap recommendations 9
Fig. 10. Suggested vias 9
Fig. 11. ESD capacitors 10
Fig. 12. Differential capacitors and LPF Filter 11
Fig. 13. VPWR decoupling capacitor 12
Fig. 14. VCOM decoupling capacitor placement 12
Fig. 15. VANA decoupling capacitor 13
Fig. 16. TPL 13
Fig. 17. Hot plug protection Zener diodes location 14
Fig. 18. Current measurement 15
Fig. 19. Assembly (PCB top side) 17
Fig. 20. Assembly (PCB bottom side) 17
Fig. 21. Layer 1 (PCB top side) 17
Fig. 22. Layer 2 (1st inner layer) 18
Fig. 23. Layer 3 (2nd inner layer) 18
Fig. 24. Layer 4 (bottom side) 18
Fig. 25. BCI test current profile 20
Fig. 26. BCI Injection probe positions 20

© 2023 NXP B.V. All rights reserved.

Contents

1 Introduction 3
2 PCB recommendations 4
2.1 Layer architecture 4
2.2 PCB zones for placement 4
2.2.1 Zone 1: Battery cell controller MC3377x 5
2.2.2 Zone 2: Filtering components 6
2.2.3 Zone 3: ESD protection 6
2.2.4 Zone 4: Isolation (transformer or capacitor isolation) 7
2.2.5 Zone 5: Components with high-power dissipation 8
3 Circuit and layout parts 9
3.1 Ground planes 9
3.2 Power planes 9
3.3 ESD capacitors 10
3.4 Balancing resistors 11
3.5 Differential capacitors and LPF filter 11
3.6 VPWR capacitors 11
3.7 VCOM 12
3.8 GPIO and NTC filter 12
3.9 VANA 12
3.10 TPL 13
3.11 Hot plug protection 14
3.12 Current sense 14
3.12.1 Thermocouple effect EMF 15
4 Reference design EVB board RD33771CDSTEVB 17
5 EMC tests 19
5.1 RE (Radiated Emission) test 19
5.2 CP Test, (Conducted disturbances - Current probe method related to CISPR25 19
5.3 BCI (Bulk Current Injection) test related to ISO 11452-4 19
5.4 ESD Test related to ISO10605 and IEC61000-4-2 21
6 General information 22
6.1 Coating 22
6.2 Layout standards 22
7 References 23
8 Legal information 24

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© 2023 NXP B.V. **All rights reserved.**

For more information, please visit: http://www.nxp.com

Date of release: 19 April 2023
Document identifier: AN12710