AN12444

PCIe Certification Guide for i.MX8 Series

Rev. 1 — 27 July 2021 Application Note

Contents

1 Introduction

This document provides a fast and easy way to describe the compliance test procedures, tools, and criteria for:

- PCI Express 3.0, 2.0, and 1.1/1.0a designs on i.MX 8 series products for both silicon validation, as per the PCIe® BASE specification
- PCI Express 3.0, 2.0, and 1.1/1.0a add-in cards motherboard systems, as per the PCIe CEM specification

2 Test equipment

2.1 Test board

The test is performed on the following boards:

- i.MX 8X Family (i.MX 8QuadXPlus as an example)
- i.MX 8XLite Family
- i.MX 8 Family
- i.MX 8M Family
- i.MX 8M Mini Family
- i.MX 8M Nano Family
- i.MX 8M Plus Family

2.2 Measurement equipment

The following equipment is used to measure signal quality:

- Oscilloscope: Keysight DSAV204A

NOTE

The solution from Keysight is not the only method for the PCIe compliance test, Tektronix, and Lecroy or other tool vendors also provide the corresponding test solution and tools. Customer can use the tool in hands. The document provides a complete test solution based on the system board-level TX compliance test for i.MX serials products, so the test get started from the Keysight tool for example.

This part also lists the reference for Tektronx and Lecroy PCI Express Compliance solution:

  - https://download.tek.com/software/supporting_files/ReadmeTekExpressPCIExpress_066155511.txt
  - cdn.teledynelecroy.com/files/pdf/qphy-pcie4-tx-rx-ds.pdf

- Cables and Adapters
  - Two Rosenberger SMP-SMP cables P/N: 71L-19K2-19K2-00305C, as shown in Figure 1

  - Four Agilent SMA-SMP cables P/N: N4235-61602, as shown in Figure 2
  - Four Agilent BNC connectors P/N: 54855-67604, as shown in Figure 3
  - Two Keysight InfiniiMax II Series Probe Amplifier, 12 GHz, P/N: 1169B, as shown in Figure 4
  - Two Keysight InfiniiMax Single-ended/Differential Probe Head, P/N: E2678B, as shown in Figure 5
- Test Fixture: CLB3.0 X1/X16, as shown in Figure 6
- PCIe M.2-to-Standard adapter you have prepared yourself, as shown in Figure 7

Figure 1. SMP-SMP cable

Figure 2. SMA-SMP cable

Figure 3. BNC connector

Figure 4. Keysight InfiniiMax II Series Probe Amplifier

Figure 5. Keysight InfiniiMax Single-ended/Differential Probe Head

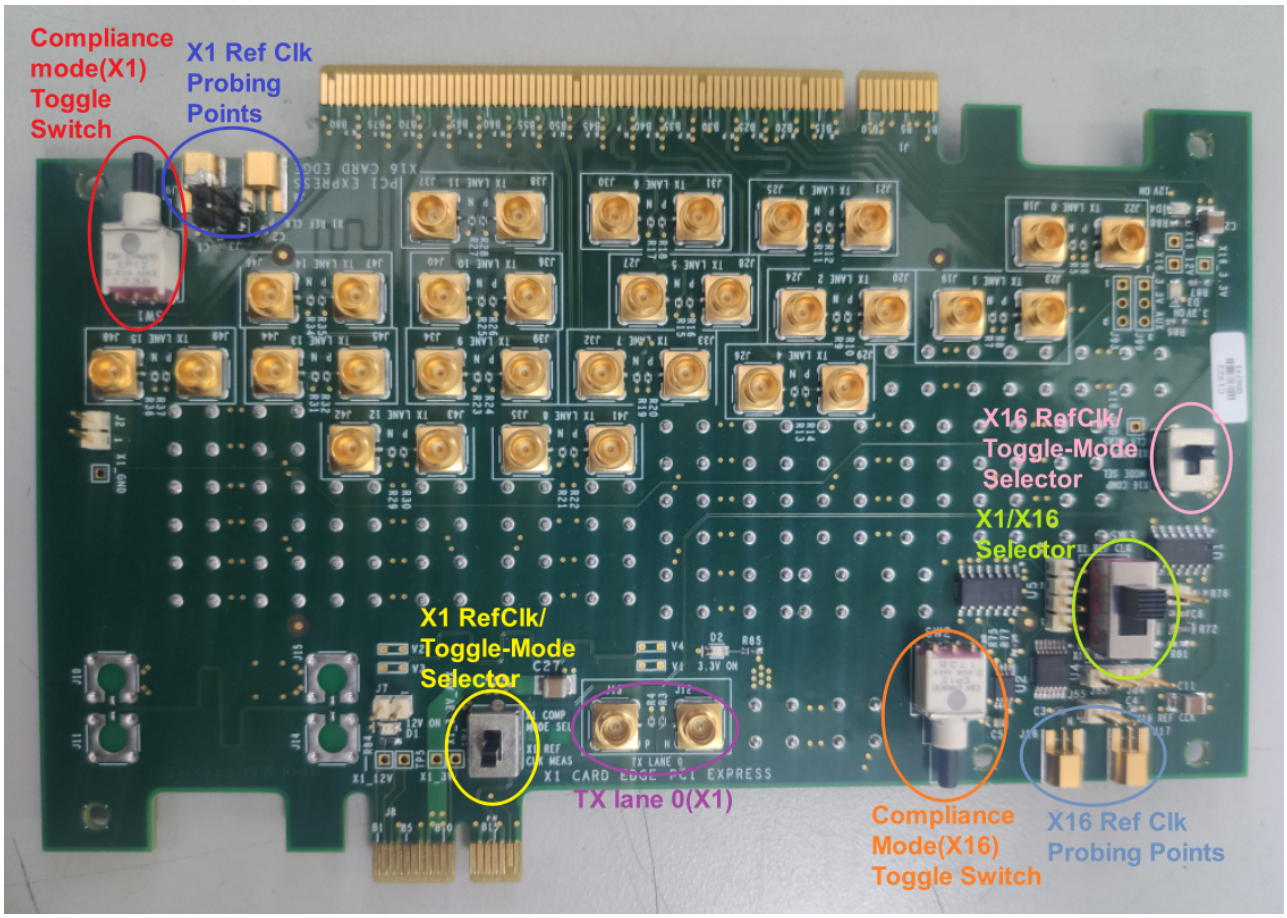

Figure 6. CLB3.0 X1X16 with several key features Highlighted

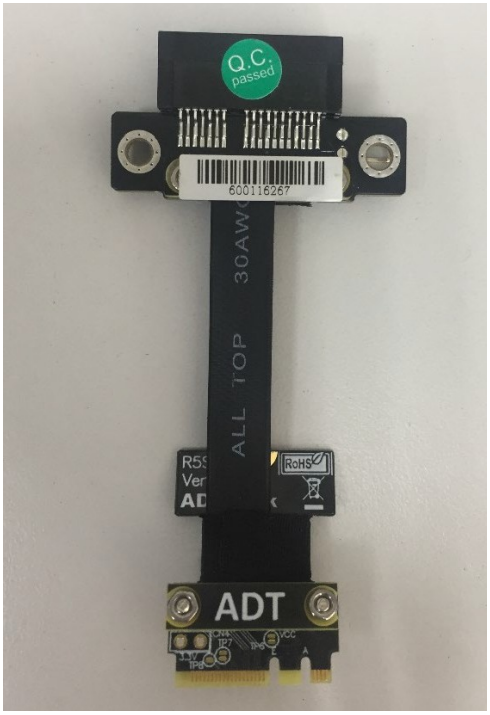

Figure 7. PCIe M.2-to-Standard adapter

2.3 Test environment

Two methods are available to the operation system:

1. Rebuilt image with the following configuration:

```
CONFIG_PCI_IMX8_COMPLIANCE_TEST=y
```

2. Add `pcie_cz_enabled=y` to `mmcargs` in U-boot. For example:

   Read the default `mmcargs` with the following command:

```
print mmcargs
```

   The default command is as below:

```
mmcargs=setenv bootargs console=ttyLP0,115200 earlycon root=/dev/mmcblk1p2 rootwait rw
```

   Enter the following command under the U-boot command:

```
setenv mmcargs "setenv bootargs console=ttyLP0,115200 earlycon root=/dev/mmcblk1p2 rootwait rw
pcie_cz_enabled=yes"
```

   Then, the command is shown as below:

```
mmcargs=setenv bootargs console=ttyLP0,115200 earlycon root=/dev/mmcblk1p2 rootwait rw
pcie_cz_enabled=yes
```

2.4 Analysis software

The used analysis software is D9040PCIC PCIExpress Test App.

NOTE

Purchase D9040PCIC Auto test APP separately and install it on the Keysight Oscilloscope.

2.5 Additional information

- Test items: only electrical tests
- Test method and equipment operation:
  - See *PCI Express Architecture PHY Test Specification, Rev. 4.0*.

    https://members.pcisig.com/wg/PCI-SIG/document/folder/830
  - See *PCI Express Card Electromechanical Specification Rev. 4.0*.

    https://members.pcisig.com/wg/PCI-SIG/document/13446
  - See *PCI Express Base Specification Rev. 5.0*.

    https://members.pcisig.com/wg/PCI-SIG/document/13005
- 100 MHz PCIe reference clock: external PLL clock (default) and internal PLL clock.

3 PCIe test procedure

For a PCIe test, perform the following steps:

1. Calibrate scopes and de-skew cables as described in **Appendix A** in *PCI Express® Card Electromechanical Specification Revision 3.0*.
2. Connect four BNC connectors to Channel 1, 2, 3 and 4 on the oscilloscope.
3. Connect four SMA-SMP cables to the BNC connectors on the oscilloscope.
   a. Connect the SMP end of the SMA-SMP cable on channel 1* to the J13 on the CLB board - the positive data line.
   b. Connect the SMP end of the SMA-SMP cable on channel 3* to the J12 on the CLB board - the negative data line.
   c. Connect the SMP end of the SMA-SMP cable on channel 2* to the J16 on the CLB board - the positive clock line (100 MHz).
   d. Connect the SMP end of the SMA-SMP cable on channel 4* to the J9 on the CLB board - the negative clock line (100 MHz).

   NOTE

   The **Connection Setup** dialog box allows the user to set up tests for multiple lanes. One or two lanes can be tested with the scope alone but all the lanes are documented. This test can be automated with the use of switches available from Keysight.
4. Insert the SD card containing the PCIe test image into the J12 slot and make sure the Boot Switches, **SW2**, are set correctly.
5. Connect the PCIe M.2-to-Standard adapter to the PCIe M.2 connector, **J5**, on the i.MX8QXP board.
6. Connect the CLB board to the PCIe M.2-to-Standard adapter.
7. Perform the settings as below on the CLB board.
   a. Switch **SW3** to **x1 REF CLK**, as shown in Figure 8.

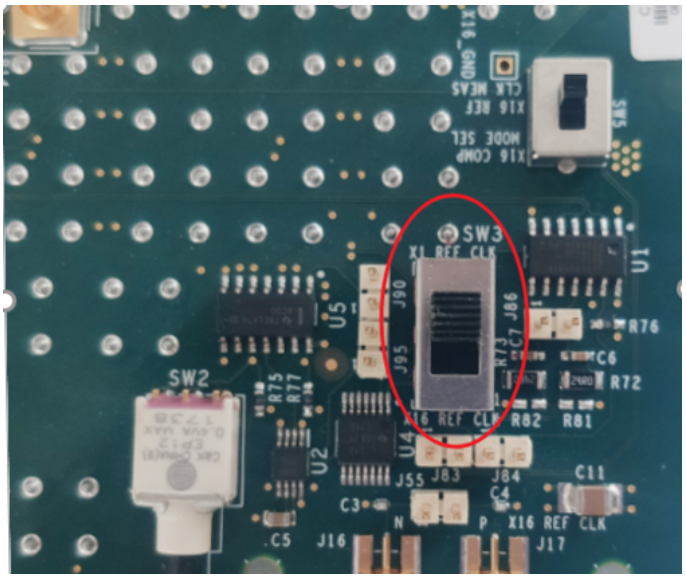

Figure 8. Switch SW3 setting

b. Switch **SW4** to **x1 REF CLK MEAS**, as shown in Figure 9.

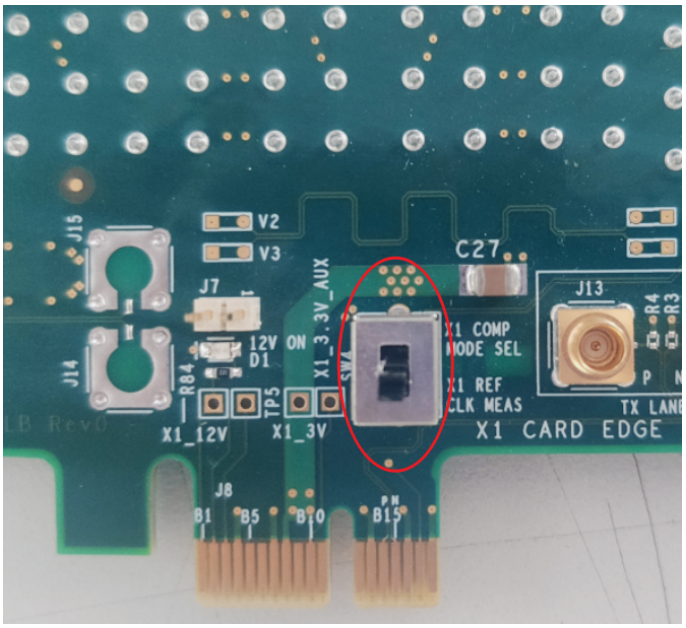

Figure 9. Switch SW4 setting

8. Figure 10 shows the complete setup.

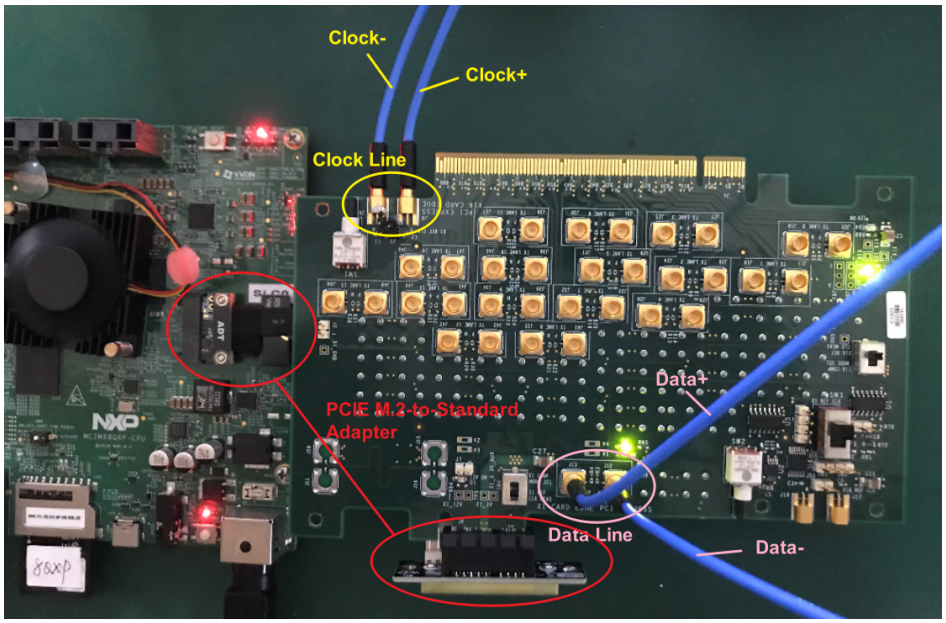

Figure 10. Complete setup

9. After all the preparations, to power on the board and run the PCIe test software on the oscilloscope, select **Analyze** → **Automated Test Apps** → **D9040PCIC PCIExpress Test App**, as shown in Figure 11.

Figure 11. Open the app

10. Perform the settings as below in the test software.
    a. In the **Device** menu, select the correct test mode.

       For example, to use PCIe1.1, select **PCIe 1.1**, as shown in Figure 12.

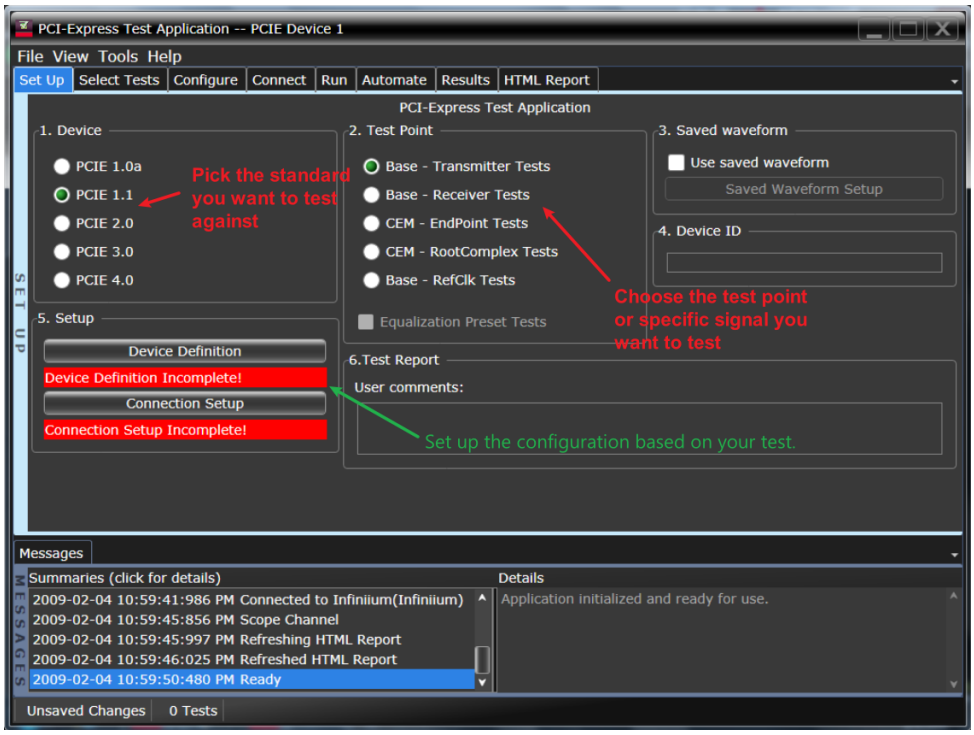

Figure 12. Setup settings in the PCIe test software - Base setup

b. In the **Test Point** menu, select **Base-RefClk Tests** or **CEM-RootComplex Tests**, as shown in Figure 13.

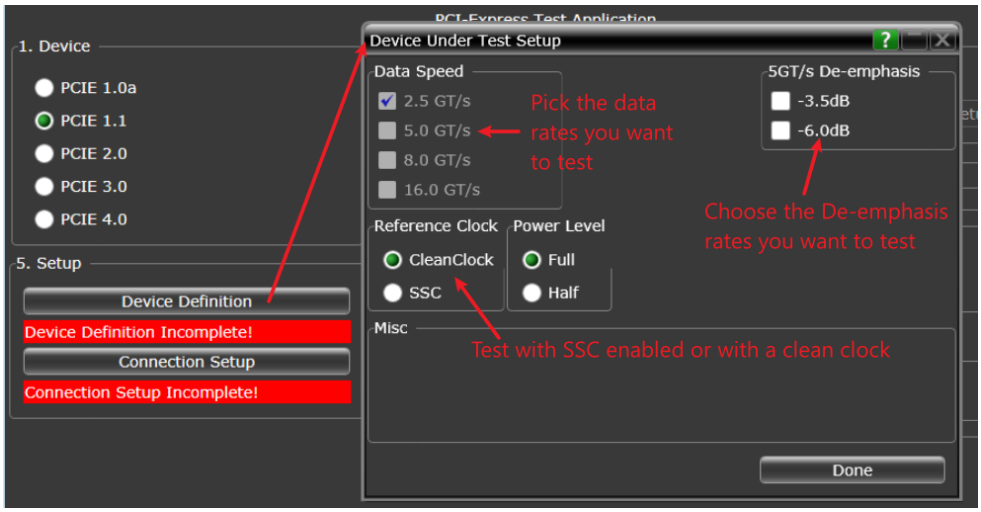

Figure 13. Setup settings in the PCIe test software - Device Under Test Setup

c. In the **Device Definition** menu, select the corresponding data rate and in the **Reference Clock** menu, select **Clean Clock**, as shown in Figure 14.

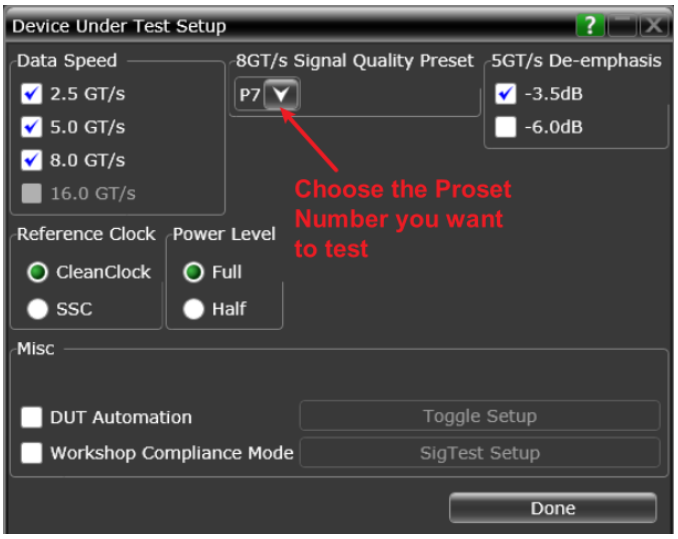

Figure 14. Setup settings in the PCIe test software - Signal Quality Preset

d. In the **Connection Setup** menu, select the proper lane, probes, and connection line based on connection for test fixture, as shown in Figure 15.

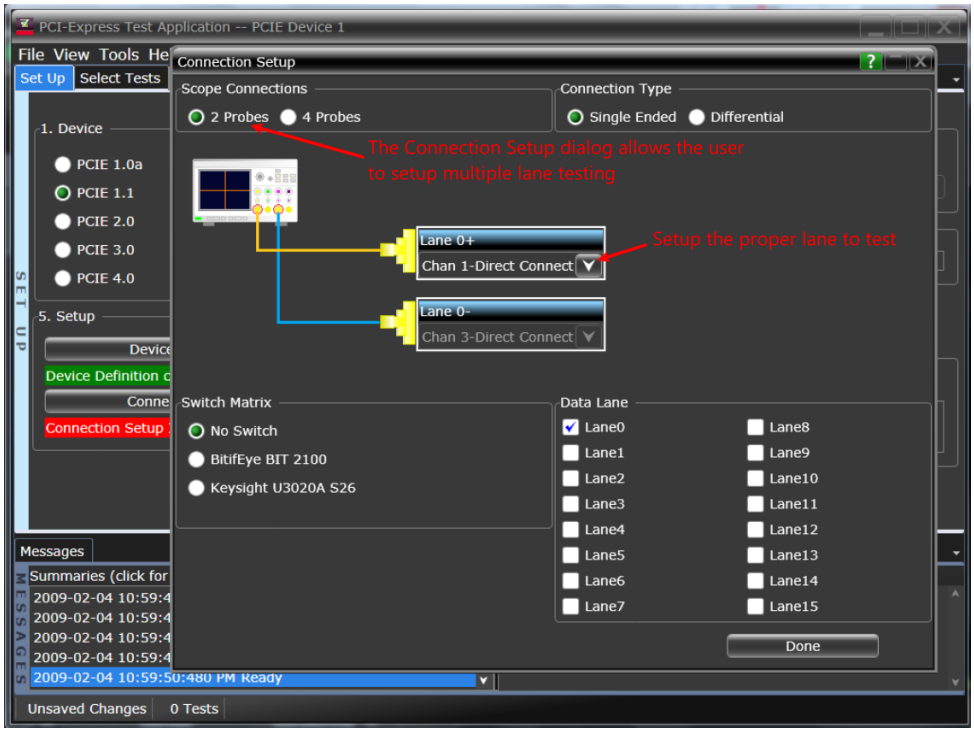

Figure 15. Setup settings in the PCIe test software - Connection Setup

e. For other options, keep the default values.

11. In the **Select Tests** menu, select the test items as required, as shown in Figure 16.

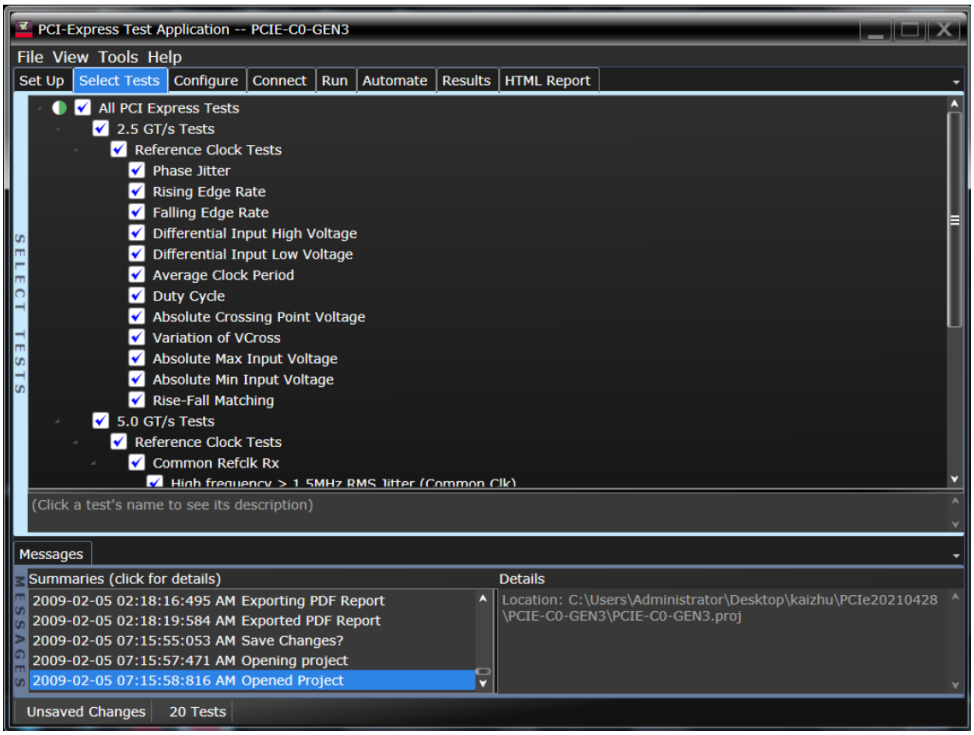

Figure 16. Select Test Menu

12. In the **Connect** menu, based on the reminder, double-check whether the test cables are connected correctly.
13. To run a PCIe 1.1 test, select **Run Tests** to start.
14. To run a PCIe 2.0 or PCIe 3.0 test, set as below:
    a. Use one SMP-SMP cable to connect **J85** to **J4** and another SMP-SMP cable to connect **J5** to **J87**, as show in Figure 17.

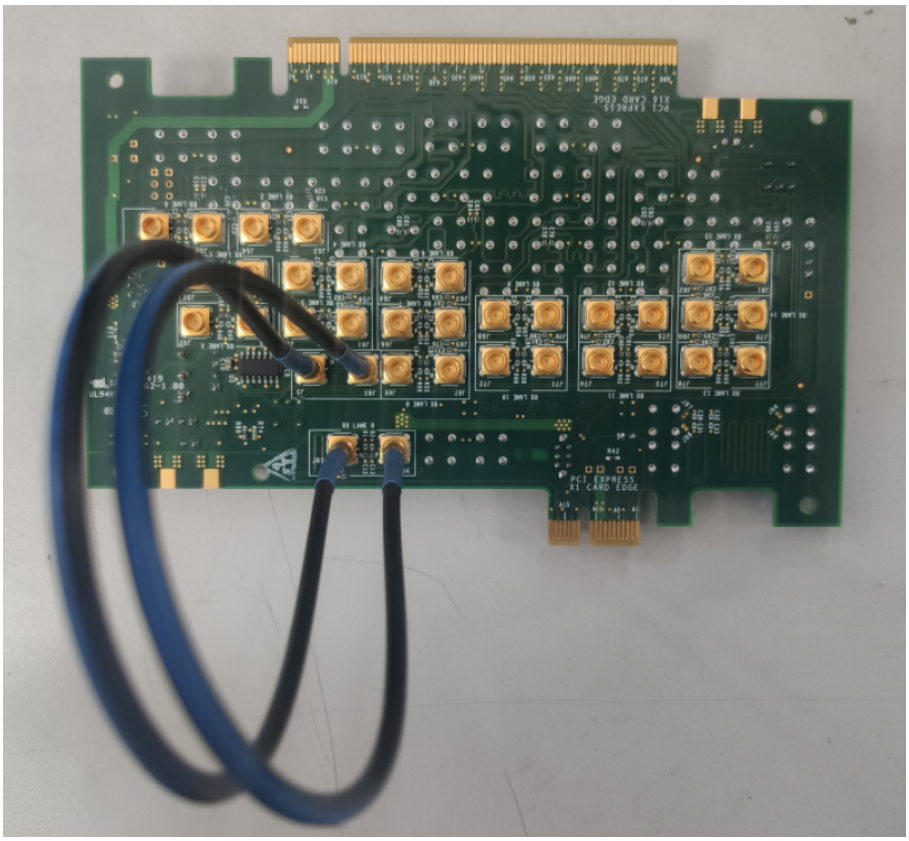

Figure 17. PCIe 2.0/3.0 test settings

b. Switch **SW4** to **x1 COMP MODE SEL**, as shown in Figure 18.

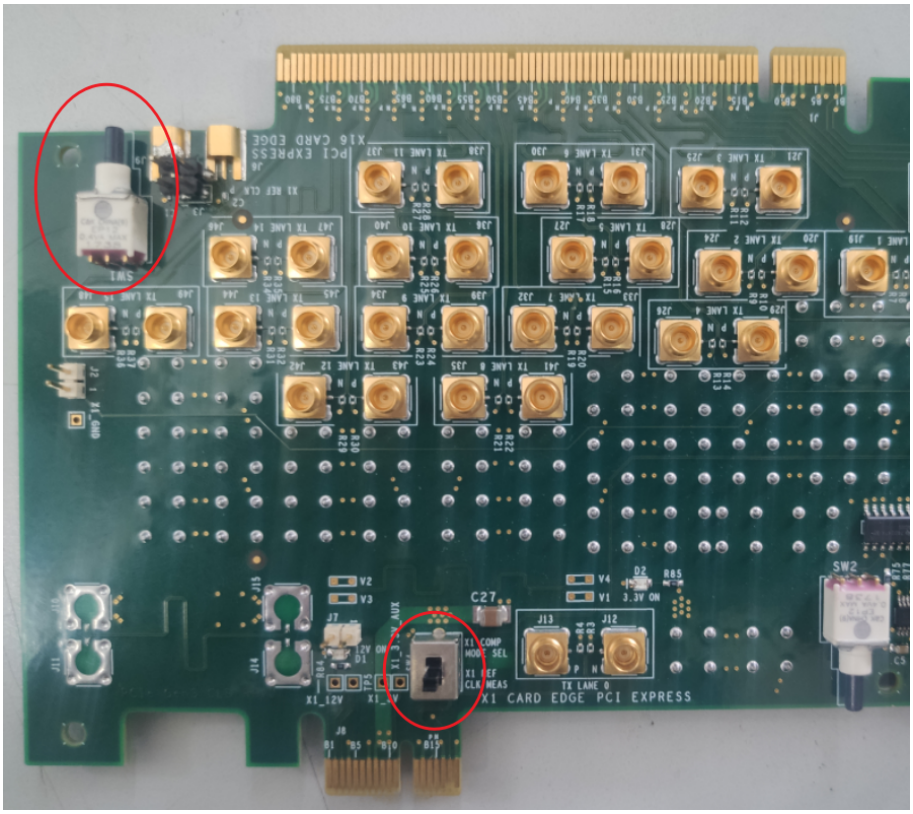

Figure 18. SW1 and SW4 settings at PCIe2.0/3.0 test

c. Press **SW1** one time to switch to **PCIe2.0 -3.5 dB**. Make sure that UI is 200 ps (5 GT/s).

Press **SW1** ten times to switch to **PCIe3.0 P7**. Make sure that UI is 125 ps (8 GT/s).

NOTE

- Power on the board before starting to set.
- The default setting is the PCIe1.1 mode. Press **SW1** once to jump to the next mode. Table 1 lists all PCIe test modes.
- PCIe3.0 P7 represents the most severe pre-aggravation, so the test is default to the worse condition.

15. After the test, switch **SW4** back to **x1 REF CLK MEAS**.

NOTE

The test item of Reference Clock: absolute crossing point voltage, 2.5 GT/s, fails with SMP-SMA direct connections.

The external clock generator, **9FGV0241**, integrates output terminations as 100 Ω and the internal termination of the oscilloscope is 100 Ω. The high-impedance leads the amplitude seen on the oscilloscope to be half of the actual output amplitude. Therefore, use different probes on Clock P and N instead of direct connection to acquire correct clock waveforms. Set the test environment as show in Figure 19.

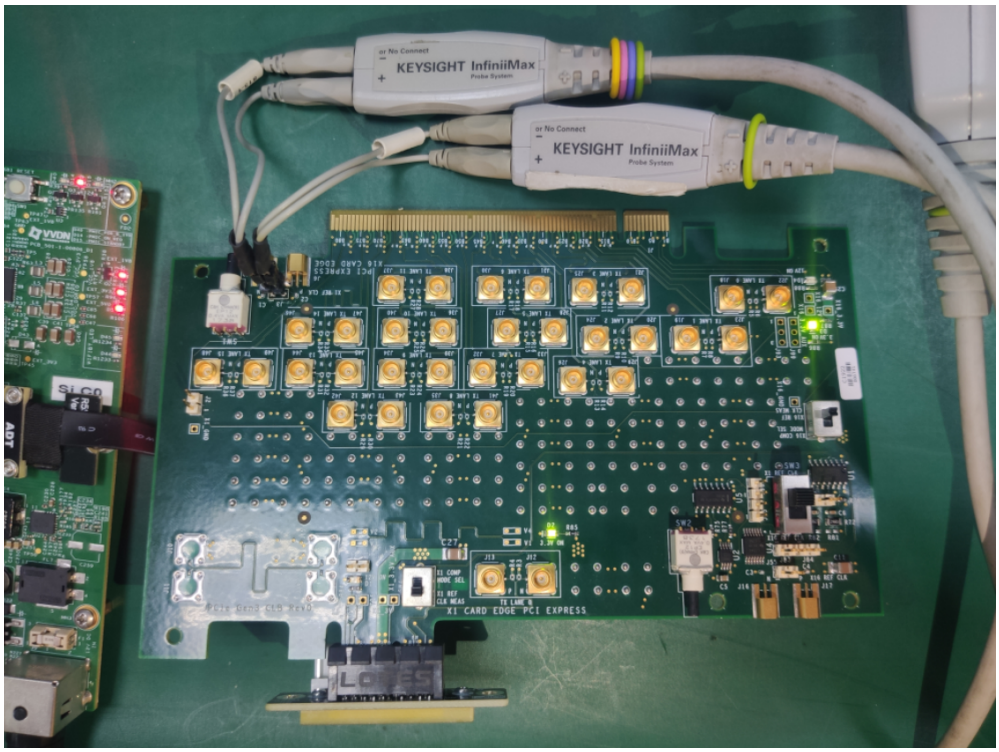

Figure 19. Crosstalk test item setup

Table 1. PCIe 1.1/2.0/3.0 test settings

PCIe	Data rate (GT/s)	Preset number	PreShoot(dB)	De-emphasis(dB)
1.1	2.5	By default	0	-3.5
2.0	5	—	0	-3.5
	5	—	0	-6
3.0	8	P0	0	-6.0±1.5
	8	P1	0	-3.5±1
	8	P2	0	-4.4±1.5
	8	P3	0	-2.5±1
	8	P4	0	0

Table continues on the next page...

Table 1. PCIe 1.1/2.0/3.0 test settings (continued)

PCIe	Data rate (GT/s)	Preset number	PreShoot(dB)	De-emphasis(dB)
	8	P5	1.9±1	0
	8	P6	2.5±1	0
	8	P7	3.5±1	-6.0±1.5
	8	P8	3.5±1	-3.5±1
	8	P9	3.5±1	0
	8	P10	0	Not Fixed[1]

1. P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. The details are described in detail in the document PCI Express® Base Specification Revision 5.0 on https://members.pcisig.com/wg/PCI-SIG/document/13446

4 PCIe test report with analysis

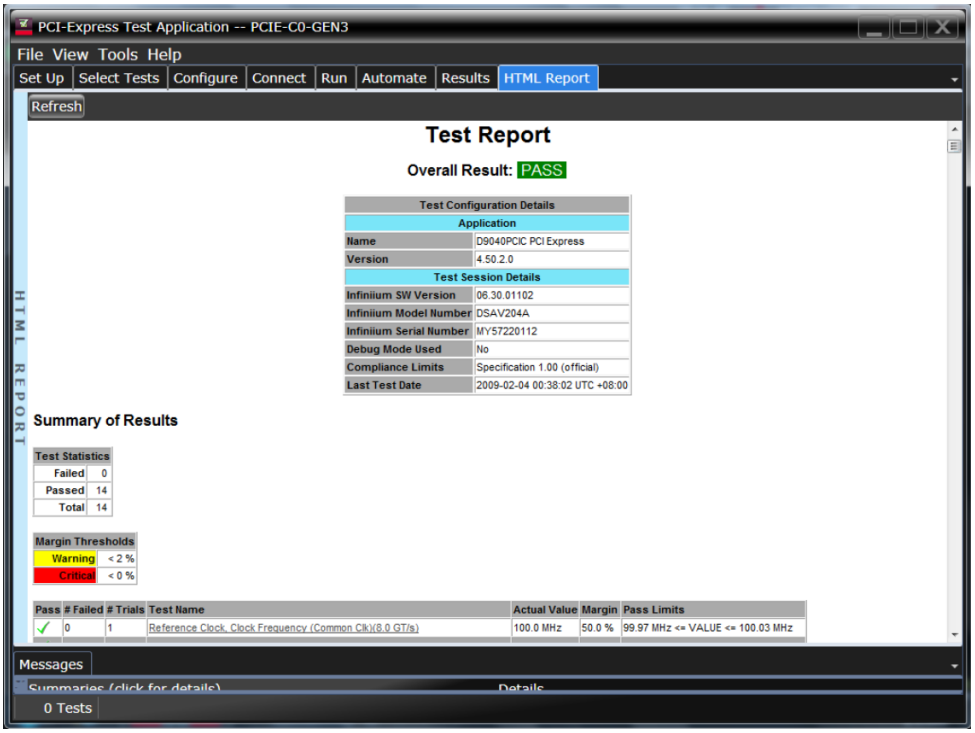

Figure 20. Test report

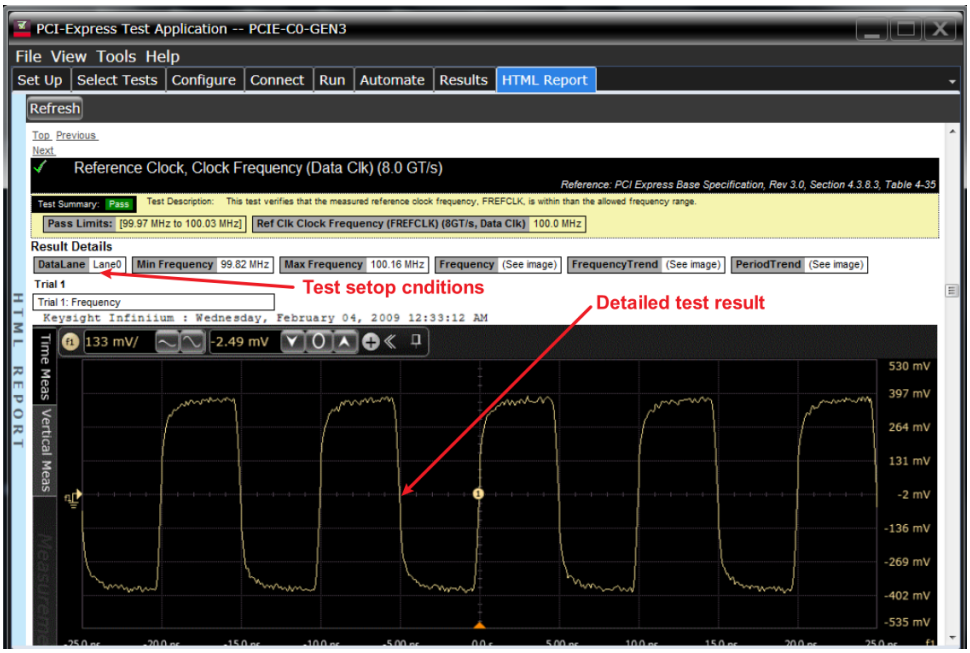

Figure 21. Test item report

The PCI Express electrical test software provides a report format. It shows where the product passes or fails and how close the result is to the limits specified for a particular test assertion. The margin test report parameter means the level where warnings are issued to electrical tests. It shows how close the product is to the official test limits defined in the particular version of the PCI Express specification under testing.

The detail report provides additional details including test setup conditions, graphical results, and test limits (where appropriate). The test report can be export as an HTML or PDF version.

4.1 PCIe 1.1 test results

Detailed settings are as shown in PCIe test procedure.

Figure 22 shows results of the PCIe 1.1 test.

Pass	# Failed	# Trials	Test Name (click to jump)	Actual Value	Margin	Pass Limits
✓	0	1	Reference Clock, Phase Jitter (2.5 GT/s)	32.88 ps	61.8 %	VALUE <= 86.00 ps
✓	0	1	Reference Clock, Rising Edge Rate (2.5 GT/s)	1.11 V/ns	15.0 %	600 mV/ns <= VALUE <= 4.00 V/ns
✓	0	1	Reference Clock, Falling Edge Rate (2.5 GT/s)	1.33 V/ns	21.5 %	600 mV/ns <= VALUE <= 4.00 V/ns
✓	0	1	Reference Clock, Differential Input High Voltage (2.5 GT/s)	396 mV	164.0 %	VALUE >= 150 mV
✓	0	1	Reference Clock, Differential Input Low Voltage (2.5 GT/s)	-402 mV	168.0 %	VALUE <= -150 mV
✓	0	1	Reference Clock, Average Clock Period (2.5 GT/s)	39 ppm	43.5 %	-300 ppm <= VALUE <= 300 ppm
✓	0	1	Reference Clock, Duty Cycle (2.5 GT/s)	49.8 %	49.0 %	40.0 % <= VALUE <= 60.0 %
✓	0	1	Reference Clock, Variation of VCross (2.5 GT/s)	41.3 mV	70.5 %	VALUE <= 140.0 mV
✓	0	1	Reference Clock, Absolute Max Input Voltage (2.5 GT/s)	403.8 mV	64.9 %	VALUE <= 1.1500 V
✓	0	1	Reference Clock, Absolute Min Input Voltage (2.5 GT/s)	-21.0 mV	93.0 %	VALUE >= -300.0 mV
✓	0	1	RootComplex Tests, Unit Interval (2.5 GT/s)	400.0170 ps	42.9 %	399.8800 ps <= VALUE <= 400.1200 ps
✓	0	1	RootComplex Tests, Template Tests (2.5 GT/s)	Pass	100.0 %	VALUE = 0.000
✓	0	1	RootComplex Tests, Median to Max Jitter (2.5 GT/s)	18.80 ps	75.6 %	VALUE <= 77.00 ps
✓	0	1	RootComplex Tests, Eye-Width (2.5 GT/s)	370.88 ps	50.8 %	VALUE >= 246.00 ps
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Transition)(2.5 GT/s)	1.0561 V	15.5 %	274.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Non Transition)(2.5 GT/s)	968.1 mV	24.5 %	253.0 mV <= VALUE <= 1.2000 V
✓	0	1	Reference Clock, Absolute Crossing Point Voltage (2.5 GT/s)	346.6 mV	32.2 %	250.0 mV <= VALUE <= 550.0 mV
✓	0	1	Reference Clock, Rise-Fall Matching (2.5 GT/s)	2.93 %	85.4 %	VALUE <= 20.00 %

Figure 22. PCIe 1.1 test results

4.2 PCIe 2.0 test results

When performing the PCIe 2.0 test, make sure you have performed Step 14.

Figure 23 shows results of the PCIe 2.0 test.

Pass	# Failed	# Trials	Test Name (click to jump)	Actual Value	Margin	Pass Limits
✓	0	1	RootComplex Tests, Unit Interval (5.0 GT/s)	200.0090 ps	42.5 %	199.9400 ps <= VALUE <= 200.0600 ps
✓	0	1	RootComplex Tests, Template Tests (5.0 GT/s)	Pass	100.0 %	VALUE = 0.000
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Transition)(5.0 GT/s)	902.0 mV	33.1 %	300.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Non Transition)(5.0 GT/s)	869.8 mV	36.7 %	300.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Eye-Width with crosstalk (5.0 GT/s)	161.14 ps	69.6 %	VALUE >= 95.00 ps
✓	0	1	RootComplex Tests, RMS Random Jitter with crosstalk (5.0 GT/s)	1.994 ps	41.5 %	VALUE <= 3.410 ps
✓	0	1	RootComplex Tests, Maximum Deterministic Jitter with crosstalk (5.0 GT/s)	10.824 ps	81.0 %	VALUE <= 57.000 ps
✓	0	1	RootComplex Tests, Total Jitter at BER-12 with crosstalk (5.0 GT/s)	38.865 ps	63.0 %	VALUE <= 105.000 ps
✓	0	1	RootComplex Tests, Eye-Width without crosstalk (5.0 GT/s)	161.37 ps	49.4 %	VALUE >= 108.00 ps
✓	0	1	RootComplex Tests, RMS Random Jitter without crosstalk (5.0 GT/s)	1.973 ps	42.1 %	VALUE <= 3.410 ps
✓	0	1	RootComplex Tests, Maximum Deterministic Jitter without crosstalk (5.0 GT/s)	10.883 ps	75.3 %	VALUE <= 44.000 ps
✓	0	1	RootComplex Tests, Total Jitter at BER-12 without crosstalk (5.0 GT/s)	38.627 ps	58.0 %	VALUE <= 92.000 ps
✓	0	1	Reference Clock, SSC Residual (Common Clk) (5.0 GT/s)	25.53 ps	66.0 %	VALUE <= 75.00 ps
✓	0	1	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Common Clk) (5.0 GT/s)	520 fs	82.7 %	VALUE <= 3.00 ps
✓	0	1	Reference Clock, SSC Deviation (Common Clk) (5.0GT/s)	-0.018 %	8.6 %	-0.53 % <= VALUE <= 0.03 %
✓	0	1	Reference Clock, Maximum SSC Slew Rate (Common Clk) (5.0GT/s)	12.7 fs/UI	98.3 %	VALUE <= 750.0 fs/UI
✓	0	1	Reference Clock, High frequency > 1.5MHz RMS Jitter (Data Clk) (5.0 GT/s)	3.72 ps	7.0 %	VALUE <= 4.00 ps
✓	0	1	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Data Clk) (5.0 GT/s)	470 fs	93.7 %	VALUE <= 7.50

Figure 23. PCIe 2.0 test report

4.3 PCIe 3.0 test results

When performing the PCIe 3.0 test, make sure you have performed Step 14.

Figure 24 shows results of the PCIe 3.0 test.

Pass	# Failed	# Trials	Test Name (click to jump)	Actual Value	Margin	Pass Limits
✓	0	1	Reference Clock, Clock Frequency (Common Clk)(8.0 GT/s)	100.0 MHz	50.0 %	99.97 MHz <= VALUE <= 100.03 MHz
✓	0	1	Reference Clock, RMS Jitter (Common Clk) (8.0 GT/s)	340 fs	66.0 %	VALUE <= 1.00 ps
✓	0	1	Reference Clock, Clock Frequency (Data Clk) (8.0 GT/s)	100.0 MHz	50.0 %	99.97 MHz <= VALUE <= 100.03 MHz
✓	0	1	Reference Clock, RMS Jitter (Data Clk) (8.0 GT/s)	510 fs	49.0 %	VALUE <= 1.00 ps
✓	0	1	RootComplex Tests, Unit Interval (8.0 GT/s)	125.0060 ps	42.5 %	124.9600 ps <= VALUE <= 125.0400 ps
✓	0	1	RootComplex Tests, Template Tests (8.0 GT/s)	Pass	100.0 %	VALUE = 0.000
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Transition)(8.0 GT/s)	477.4 mV	38.0 %	34.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Peak Differential Output Voltage (Non Transition)(8.0 GT/s)	473.4 mV	37.7 %	34.0 mV <= VALUE <= 1.2000 V
✓	0	1	RootComplex Tests, Eye-Width (8.0 GT/s)	79.84 ps	93.6 %	VALUE >= 41.25 ps

Figure 24. PCIe 3.0 test report

5 Useful links

- PCI Express Spec
- i.MX 8 Series Applications Processors
- Test software and tools

6 Revision history

Rev.	Date	Description
0	May 2019	Initial release
1	27 July 2021	• Updated Introduction to a clearer description • Updated Test board to cover more i.MX8 series • Added two measurement equipment to pass test item of Reference Clock and updated images in Measurement equipment • Added a portable method to set the operation system in Test environment • Updated the analysis software to the latest version in Analysis software • Updated the link in Additional information to the latest version • Updated the images and procedures to the latest analysis software, and added a solution to fix the issue of failure to test item of Reference Clock in PCIe test procedure • Updated to a clearer description and updated the test item of PCIE compliance test of GEN1/2/3 in PCIe test report with analysis • Updated the link in Useful links to the latest version.

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