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DisplayPort PCB layout guidelines

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Document information

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Keywords	DisplayPort, PTN33xx, CBTL061xx, PCB, layout, signal integrity, symmetry, loss, jitter
Abstract	This document provides a practical guideline for incorporating the DisplayPort ICs layout into PCB designs.

founded by Philips

Revision history

Rev	Date	Description
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1. Introduction

This document provides a practical guideline for incorporating the NXP DisplayPort (DP) ICs, DisplayPort level shifter PTN33xx family and DP/PCI Express (PCIe) multiplexer CBTL061xx family, layout into a Printed-Circuit Board (PCB) design.

DisplayPort interconnect is a point-to-point layout of serial differential signal trace pairs. The document provides guidelines for DP lane connection for the PCB traces, vias and AC coupling capacitors. The most important considerations are to minimize loss and jitter, and to maintain signal integrity.

These are general guidelines only. Board designers should carefully weigh design trade-offs and use simulation analysis to ensure a successful implementation.

2. DisplayPort interconnection PCB layout

DisplayPort is a scalable digital display interface. The interface is designed to support both internal chip-to-chip and external box-to-box digital display connections. The Main Link consists of one, two or four AC-coupled, doubly terminated differential pairs (lanes). Two link rates are supported: 2.7 Gbit/s and 1.62 Gbit/s per lane.

DisplayPort transmit signals are often implemented to share pins with DVI and HDMI signals. These multi-mode DisplayPort signals are sometimes multiplexed with PCI Express signals, which supports 2.5 Gbit/s and/or 5 Gbit/s data rate.

The high bit rate for DP/PCIe requires some specific PCB design considerations. Minimizing interconnect loss and jitter are the key requirements.

2.1 PCB stack-up and reference planes

DisplayPort requires no new PCB technology. Generally PC system boards are designed with 4-layer FR4 stack-up, with 1080 prepreg and 47 mil core, and a 0.059 inch nominal thickness.

To minimize loss and jitter, the most important considerations are to design to a target impedance and to keep tolerances small.

A signal pair should avoid discontinuities in the reference plane, such as splits and voids. When a signal changes layers, the ground stitching vias should be placed close to the signal vias. A minimum of 1 to 3 stitching vias per pair of signals is recommended. Never route a trace so that it straddles a plane split.

2.2 Traces

2.2.1 Impedance

PTN33xx and CBTL061xx I/O impedance is targeted at 50 Ω single-ended and 100 Ω differential. It is recommended that DP link PCB traces maintain 50 Ω ± 15 % single-ended and 100 Ω ± 20 % differential impedance to maintain signal integrity.

In *“Eaglelake platform design guide”*, Intel recommends 95 Ω ± 15 % differential impedance for DP and HDMI/DVI signals, and 85 Ω ± 15 % for PCIe.

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The impedance target has been lowered in the Calpella platform, which is for year 2009, including docking and add-in card. For all differential signals, DP, HDMI/DVI, and PCIe, impedance is targeted at 85 Ω ± 15 %.

There are two reasons mainly for this non-100 Ω recommendation. One is the signal loss. The higher the impedance is, the more the loss is. The trace length between the chip set and the connector may be as long as 2 inches to 4 inches, which may contribute a significant amount of loss.

The other reason is that the simulation shows the signal discontinuity is significant at the conjunction of PCB trace and high-speed connectors, especially PCIe connector, and the TDR measurement shows the dip can be as low as 70 Ω. The chip set is still designed for 100 Ω, so that there is a discontinuity from the chip set to the PCB. However, simulations have shown that the overall effect is still better to have the PCB designed at 85 Ω characteristic impedance.

2.2.2 Width and spacing

The coupling of the intra-pair differential signals and increased spacing to neighboring signals help to minimize harmful crosstalk impacts and ElectroMagnetic Interference (EMI) effects. In the microstrip case, a differential trace should be 5 mils wide, with a 7 mil wide air gap spacing between the two traces of a pair.

The spacing between pairs and to all non-DP/PCIe signals should be at least four times the dielectric height. If the non-DP/PCIe signals have significantly higher voltage levels or edge rate than the DP/PCIe signal, the space should increase to 30 mils in order to avoid coupling.

2.2.3 Length and length matching

Trace length greatly affects the loss and jitter budgets of the interconnection. The PCB trace may introduce 1 ps to 5 ps of jitter and 0.35 dB to 0.50 dB of loss per inch.

Long distance traces should be routed at an off-angle to the X-Y axis of a PCB layer, in order to distribute the effects of fiberglass bundle weaves and resin-rich areas of the dielectric.

The two traces of a pair should be symmetrically routed.

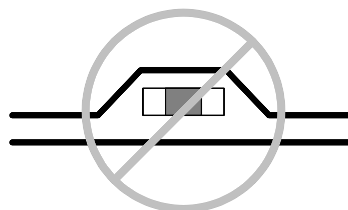

Fig 1. Non symmetrical routing should be avoided

The length difference between a differential pair should be limited to 5 mils maximum. Length matching is required per segment, and any length added (typically a ‘serpentine’ section) for the sake of matching a pair should be added near the location where the mismatch occurs.

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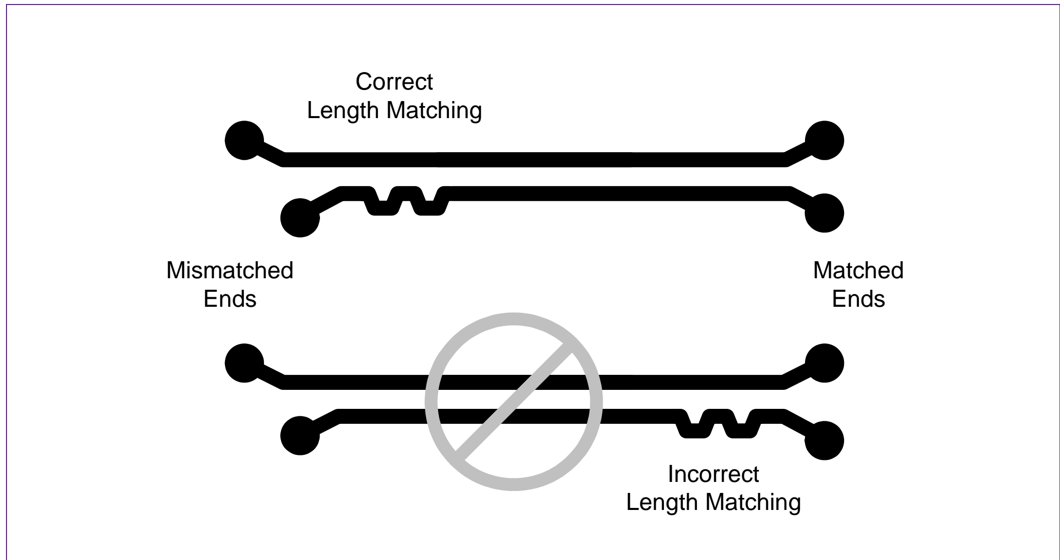

Fig 2. Length matching near location of mismatch

2.2.4 Bends

The use of bends should be kept to a minimum, since a bend can introduce common mode noise into the system, which will affect the signal integrity and EMI of the differential pair.

Bends on traces should be ≥ 135°. Tighter bends should be avoided because they impact the loss and jitter budgets.

If bends are used, the following guidelines are recommended to avoid tight bends (see Figure 3):

1. Keep all angles between traces (α) ≥ 135°.
2. Maintain an air gap (A) of ≥ 20 mils.
3. Segments such as B and C, which flank a bend, should have a length ≥ 1.5 times the width of the trace.

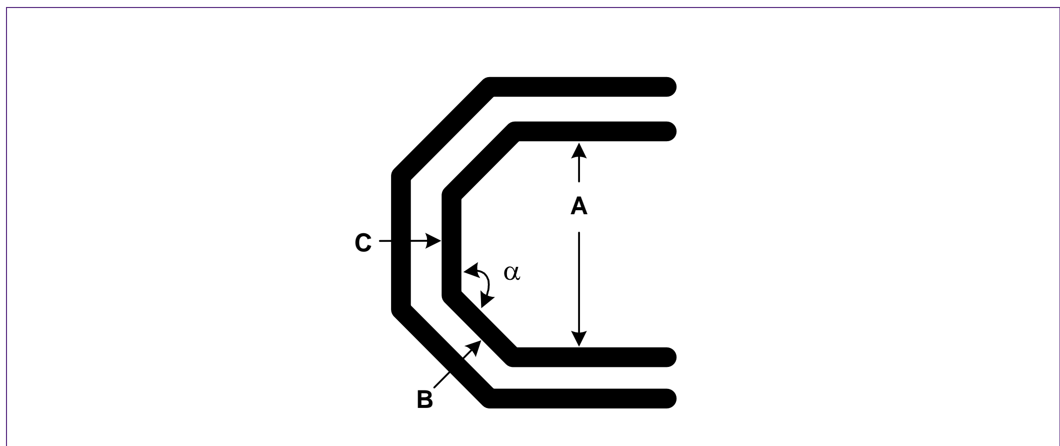

Fig 3. Trace bending guidelines

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The number of left and right bends should be as close to equal as possible, to minimize the length mismatch.

When a serpentine section is used to match one length to another, as shown in Figure 4, the length of each jog must be at least three times the trace width. The maximum distance between traces in a serpentine section should be less than two times the distance between traces in a non-serpentine section.

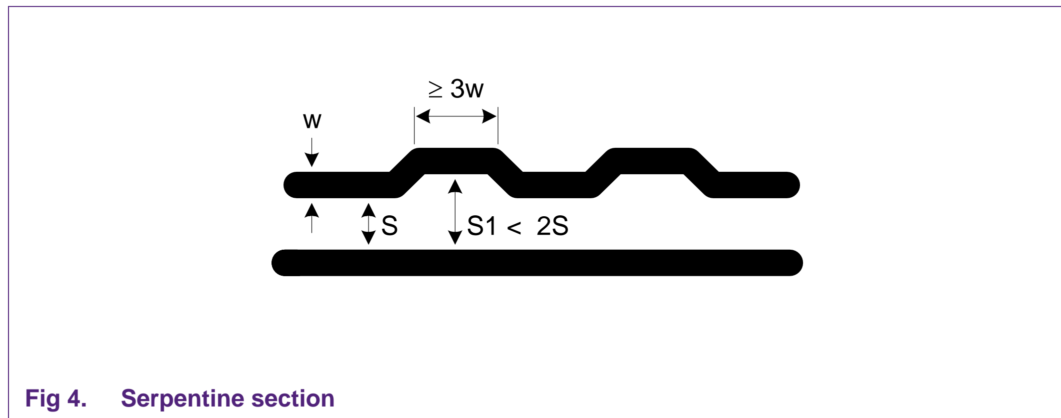

Fig 4. Serpentine section

An uncoupled section of trace routing into a pin or a ball should be ≥ 45 mils when using multiple bends, as shown in Figure 5.

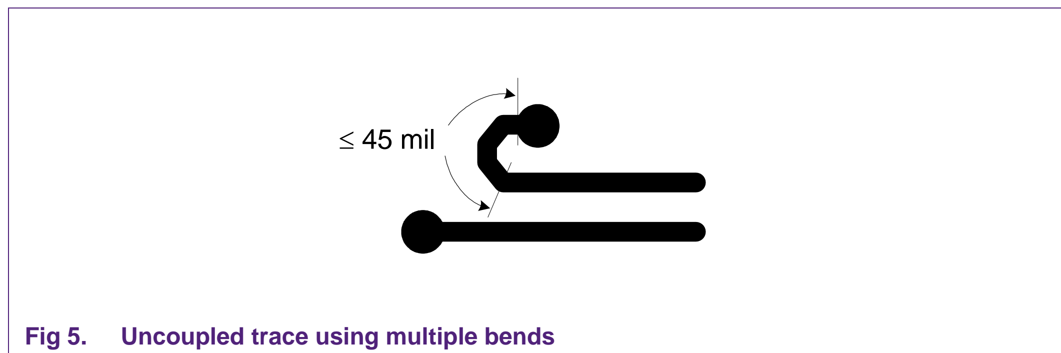

Fig 5. Uncoupled trace using multiple bends

2.3 Test points, vias and pads

Signal vias affect the overall loss and jitter budgets. Each via pair may contribute 0.25 dB of loss in some corner cases. Vias may limit the achievable maximum routing length.

Vias should have a pad size of 25 mils or less, and a finished hole size of 14 mils or less. Two vias must be placed as a symmetric pair in the same location.

Test points (which can be vias, pads or components) and probe pads should be placed symmetrically in series. Stubs should not be introduced on differential pairs. Refer to Figure 6 for illustrations of correct and incorrect placements.

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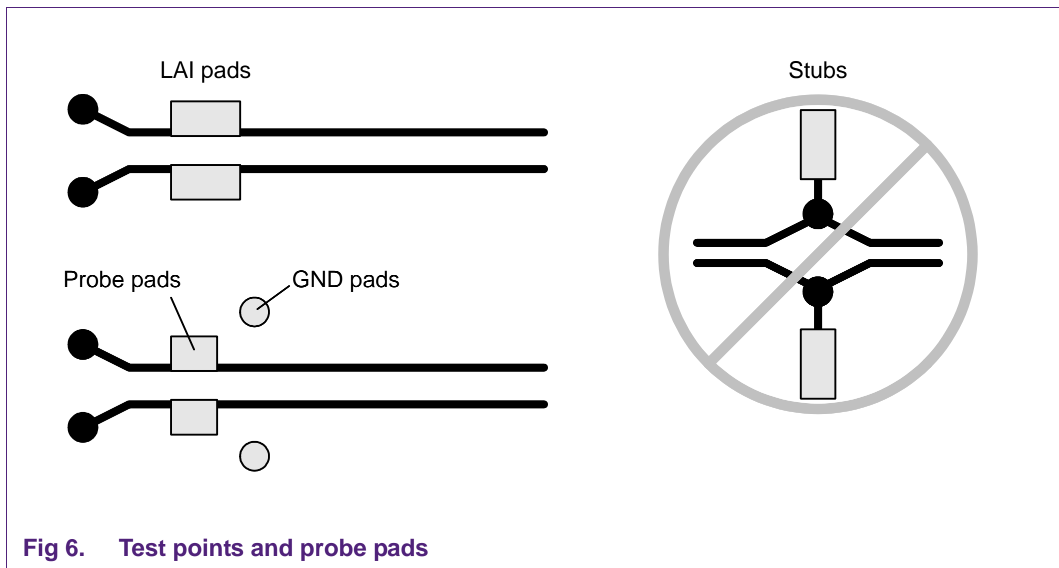

Fig 6. Test points and probe pads

2.4 AC coupling capacitors

DP and PCI Express require AC coupling between transmitter and receiver. The AC coupling capacitors for both differential pair signals must be the same value, same package size, and have symmetric placement. If possible, TX traces should route on the top layer.

The capacitor value must be in the range of 75 nF to 200 nF (100 nF is best). The 0402 package size is preferred, and 0603 is acceptable. C-pack is not allowed.

The breakout into and out of capacitors should be symmetrical for both signal lines in a differential pair. The trace separation for routing to pads must be minimized in order to optimize tight coupling between the signal pairs.

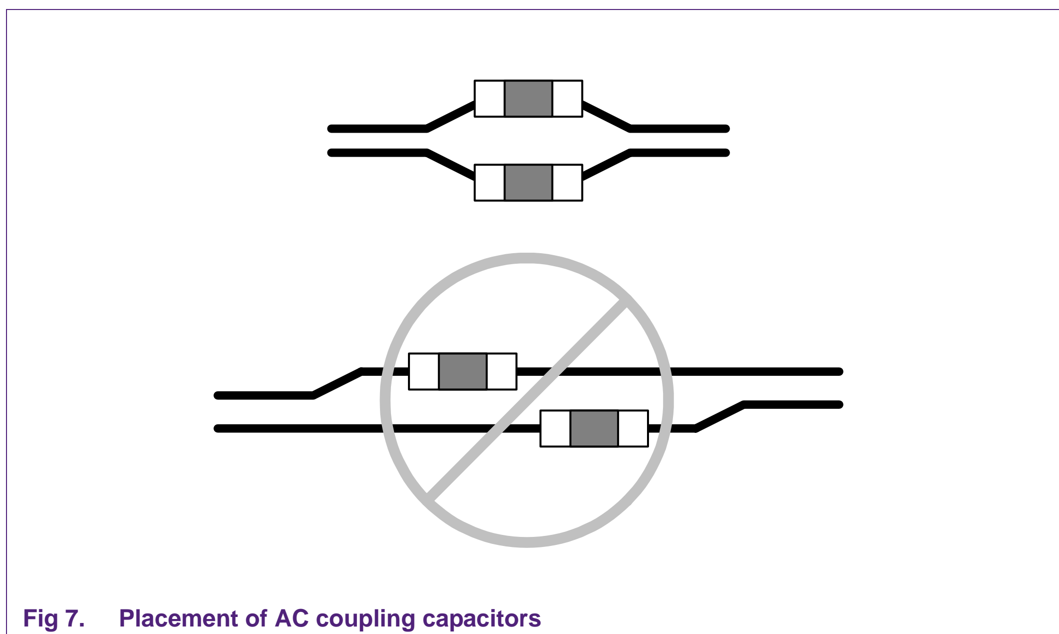

Fig 7. Placement of AC coupling capacitors

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2.5 HWQFN/HVQFN exposed center pad solder lands

Both DisplayPort level shifter PTN33xx family and DP/PCI Express (PCIe) multiplexer CBTL061xx family use HWQFN and HVQFN packages.

The HVQFN/HWQFN package exposed center pad must be soldered to a corresponding solder land on the board for enhanced thermal, as well as electrical ground, performance.

During reflow soldering, solder paste melts and gas or trapped air is released, causing splattering or solder balling. Solder balling and splatter can be minimized if the solder paste is printed as a number of individual dots, instead of one large deposit, and if the solder paste is kept at a sufficient distance from the edge of the solder land.

The solder paste pattern area should cover 35 % of the solder land area. When printing solder paste on the exposed die pad solder land, the solder paste dot area should cover no more than 20 % of this solder land area. Furthermore, the paste should be printed away from the solder land edges. This is illustrated in Figure 8; the solder paste pattern area lies within the boundary indicated by the red line and it is divided by the entire solder land area.

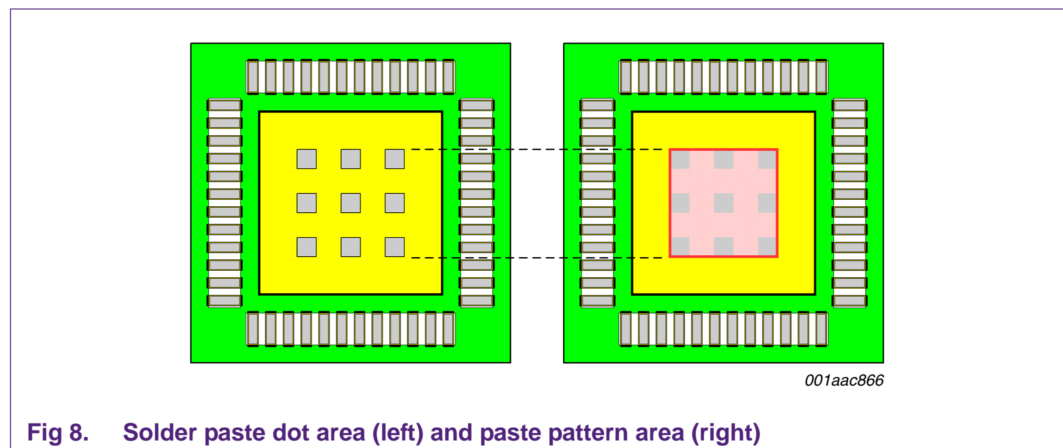

Fig 8. Solder paste dot area (left) and paste pattern area (right)

3. Summary

The DP/PCIe signals on the board work at 1.6/2.7 Gbit/s or 2.5/5 Gbit/s speed. The high data rate requires some specific implementations in the PCB layout design. The following is the summary of guideline:

- The differential pair must be routed symmetrically. Keep all differential signal traces the same length. The difference in trace length should be less than 5 mils.
- Maintains 50 Ω ± 15 % single-ended and 100 Ω ± 20 % differential impedance.
- Do not route high speed signals over any plane split; use only one ground plane underneath the differential signals.
- Avoid any discontinuity for signal integrity. Differential pairs should be routed on the same layer. The number of vias on the differential traces should be minimized. Test points should be placed in series and symmetrically. Stubs should not be introduced on the differential pairs.
- Use caution with the exposed center pad solder land for HWQFN/HVQFN package.

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4. Abbreviations

Table 1. Abbreviations

Acronym	Description
DP	DisplayPort
DVI	Digital Visual Interface
EMI	ElectroMagnetic Interference
HDMI	High Definition Media Interface
HVQFN	plastic thermal enhanced very thin quad flat package
HWQFN	plastic thermal enhanced very very thin quad flat package
I/O	Input/Output
IC	Integrated Circuit
PC	Personal Computer
PCB	Printed-Circuit Board
PCIe	PCI Express
TDR	Time-Domain Reflectometry

5. References

[1] **Eaglelake platform design guide —** Rev. 1.1.1, September 2007; Intel Corp.

[2] **Calpella platform design guide —** Rev. 0.8, August 2008; Intel Corp.

[3] **DisplayPort Standard —** Version 1.1; VESA

[4] **AN10373, “PCI Express PHY PCB Layout Guideline” —** Rev. 01; 30 April 2005; NXP Semiconductors

[5] **Board design guidelines for PCI Express architecture —** 2004; PCI-SIG

[6] **AN10366, “HVQFN application information” —** Rev. 02; 12 January 2006; NXP Semiconductors

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