AN10724

TDA8026ET - 5 slots smart card interface

Rev. 1.1 — 6 June 2016 Application note

Document information

Info	Content
Keywords	TDA8026, 5 slots, Smart Card Interface, Banking, EMV, Point-Of-Sale, ISO 7816-3
Abstract	This application note describes the smart card interface integrated circuit TDA8026ET. This document helps to design the TDA8026 in an application. The general characteristics are presented and different application examples are described.

Revision history

Rev	Date	Description
1.1	20160606	Description of upgrade from C2 to C3
1.0	20110927	Initial release

Contact information

For more information, please visit: http://www.nxp.com

1. Introduction

The TDA8026 is a multiplexed smart card interface device forming the electrical interface between a microcontroller and 5 smart cards. This device supports asynchronous cards (micro controller-based IC cards) as well as synchronous cards (mainly memory cards).

The electrical characteristics of the TDA8026 are in accordance with EMV 4.3 requirements and also comply with ISO7816-3 for class A, B and C cards.

The TDA8026 is designed to be used in payment applications such as Point-Of-Sale terminals (POS), public phones, vending machines…

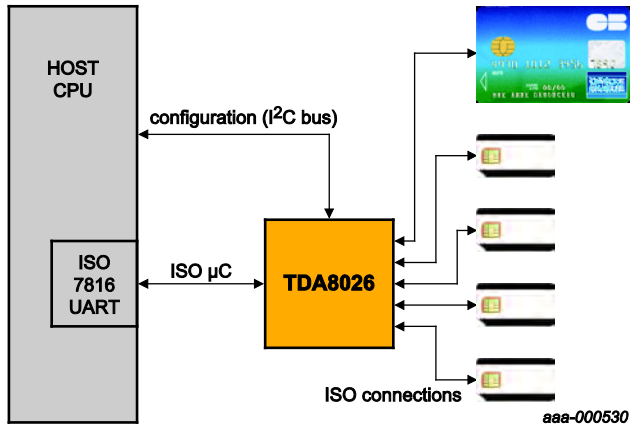


Fig 1. TDA8026 Application overview

2. Power Supply

In the TDA8026, two different power supply pins are used:

$V_{DD(INTF)}$ for the interface and the digital part

VDD for the DC/DC converter (used for the generation of the smart card voltage) and the other parts

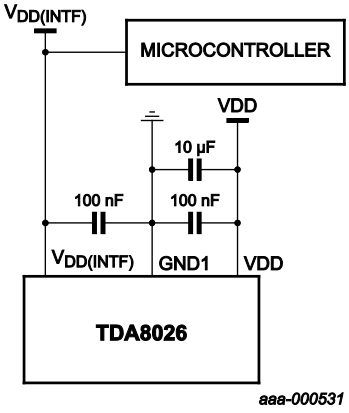


Fig 2. Power supply connections

2.1 General power supply (VDD)

VDD is the main power supply. It is mainly used to generate the smart card voltage (through the DC/DC converter)

2.1.1 Voltage range

VDD must be in the range from 2.7V to 5.5V.

2.1.2 Decoupling

In order to filter the possible noise on VDD, a capacitor of several µF (see DC/DC converter chapter) and a capacitor of 100nF must be placed between VDD and GND. The 100nF allows to filter the high frequency noise. It shall be connected close to the VDD pin.

The bigger capacitor is used to filter low frequency spikes.

2.2 Interface power supply ($V_{DD(INTF)}$)

$V_{DD(INTF)}$ is dedicated to the interface supply. All signals which are interfaced with the host are referenced to this voltage supply. $V_{DD(INTF)}$ must be the same supply pin than the microcontroller in order to have the same voltage levels.

2.2.1 Voltage range

$V_{DD(INTF)}$ must be in the range from 1.6V to 3.6V.

2.2.2 Decoupling

It is assumed that $V_{DD(INTF)}$ is more stable than VDD. Therefore a unique 100nF capacitor is generally needed to decouple $V_{DD(INTF)}$. This capacitor must be placed close to the $V_{DD(INTF)}$ pin.

2.3 Ground pins

GND1 is the ground pin used for the power supply and GNDP is the DC/DC converter ground pin. They must be connected to the main ground with straight and low resistive connections.

The other ground pins from GND2 to GND10 must also be connected to the ground. This connection is mandatory for thermal dissipation.

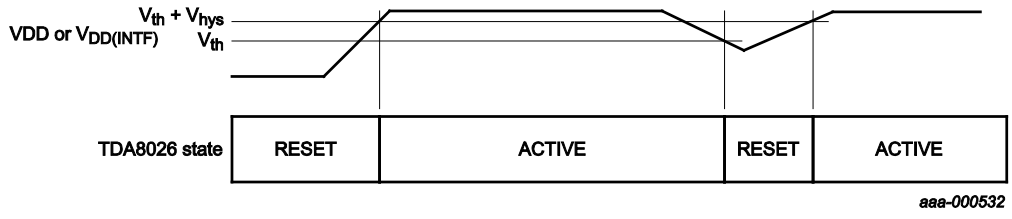
The other ground pins are the ground pins for the smart card connectors (GNDS, GNDC1 and GNDC2). They must be connected to the main ground as well.

2.4 Supervisor

Both VDD and $V_{DD(INTF)}$ power supplies are monitored.

2.4.1 VDD supervision

VDD supervision uses an internal threshold voltage. When VDD is less than this threshold, the chip is in reset state.



(1) $V_{DD(INTF)}$ is assumed to be above its own threshold

Fig 3. VDD supervision

2.4.2 $V_{DD(INTF)}$ supervision

$V_{DD(INTF)}$ can be supervised through the PORADJ pin.

The supervision principle is given in the next two pictures:

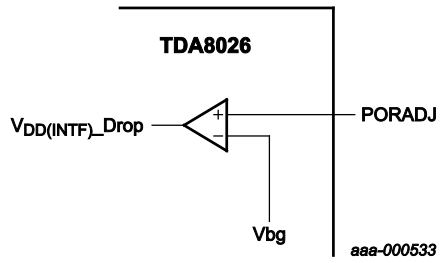


Fig 4. $V_{DD(INTF)}$ supervision – PORADJ level detector

The TDA8026 compares the pin voltage level on pin PORADJ to an internal voltage reference called Vbg.

When PORADJ falls below Vbg, the TDA8026 is reset:

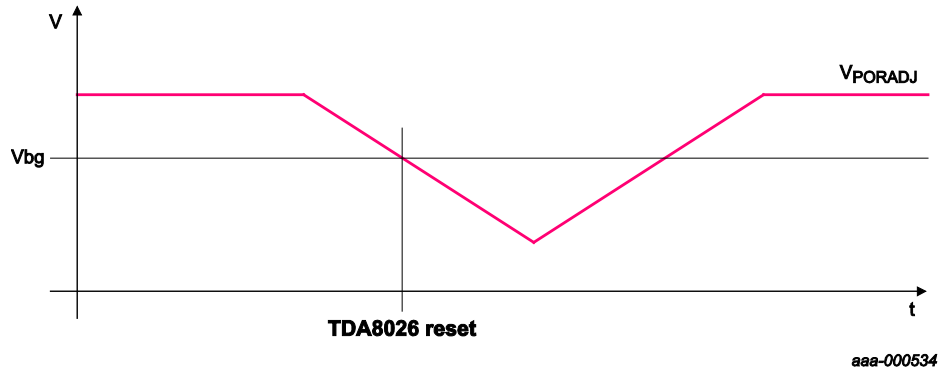


Fig 5. $V_{DD(INTF)}$ supervision – Reset when PORADJ falls

To detect a drop on $V_{DD(INTF)}$, a voltage level referred to $V_{DD(INTF)}$ must be connected to PORADJ. This voltage level can be obtained with a resistor bridge:

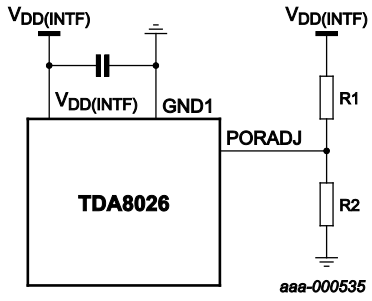


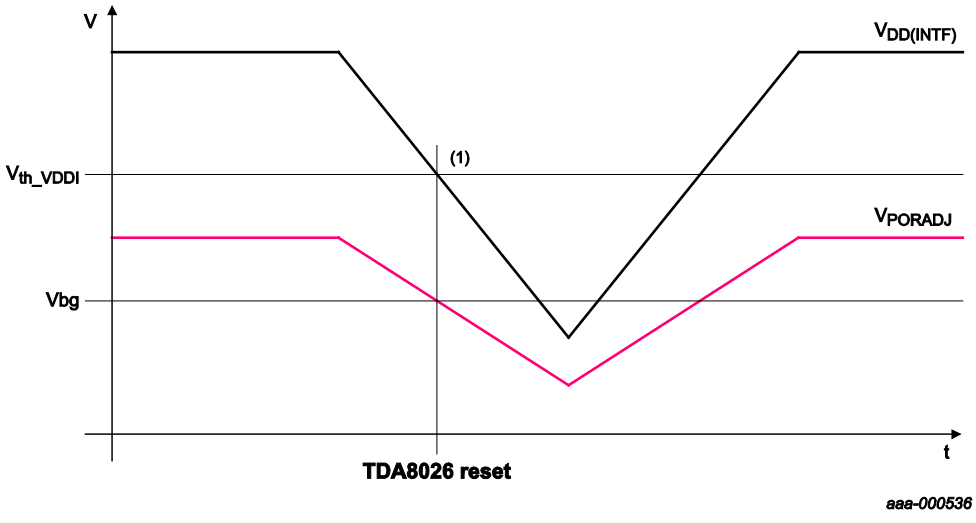
Fig 6. $V_{DD(INTF)}$ supervision – Resistor bridge

In this case PORADJ = $V_{DD(INTF)}$.R2/(R1+R2) and $V_{DD(INTF)}$ is monitored indirectly: the TDA8026 enters the reset mode when $V_{DD(INTF)}$.R2/(R1 + R2) falls below Vbg.

This corresponds to a “virtual” threshold on $V_{DD(INTF)}$ which value is obtained when

Vbg = $V_{DD(INTF)}$.R2/(R1+R2) ➔ $V_{DD(INTF)}$ = Vbg.(1+R1/R2)

This virtual threshold is called V_{th_VDDI}. This is called virtual as $V_{DD(INTF)}$ is never compared to V_{th_VDDI}. Only PORADJ is compared to Vbg. The following drawing shows this behavior:



(1) When $V_{DD(INTF)}$ falls below V_{th_VDDI}, V_{PORADJ} falls below Vbg then the drop-off is detected

Fig 7. $V_{DD(INTF)}$ supervision – Virtual $V_{DD(INTF)}$ threshold V_{th_VDDI}

The resistor bridge is needed only in the case a specific threshold on $V_{DD(INTF)}$ must be chosen for the application, but in the general case, $V_{DD(INTF)}$ can be input directly on PORADJ.

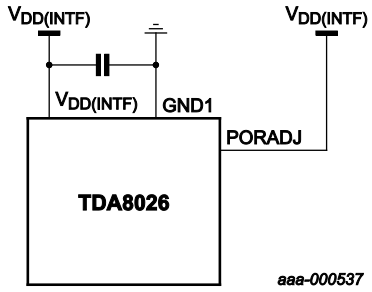


Fig 8. $V_{DD(INTF)}$ supervision – No resistor bridge

This is a particular case of the previous description with R1 = 0Ω and R2 = ∞.

Here V_{th_VDDI} = Vbg.(1+R1/R2) = Vbg.

2.5 Shutdown mode

The shutdown mode is a reset mode where the power supply is still on and one function is still enabled: the presence detection of the slot 1.

This mode is a low consumption mode (25 µA typ.)

To enter this mode, the SDWNN pin can be pulled-low at any time. See the “Functional shutdown mode” chapter for more details.

3. DC/DC converter

3.1 Description

The DC/DC converter allows to generate a voltage higher than the input power supply. This is used for instance to generate a stable 5V to supply the smart card.

3.2 Using the DC/DC converter

To use the DC/DC converter, the DCDC_OFF pin must be connected to the ground.

All the following components are mandatory to have the DC/DC converter work properly:

1 µF ceramic capacitor between VREG and GNDP

A 10 µH inductor between VDD and LX

A schottky diode between LX and VUP

A 10 µF ceramic capacitor between VUP and GNDP

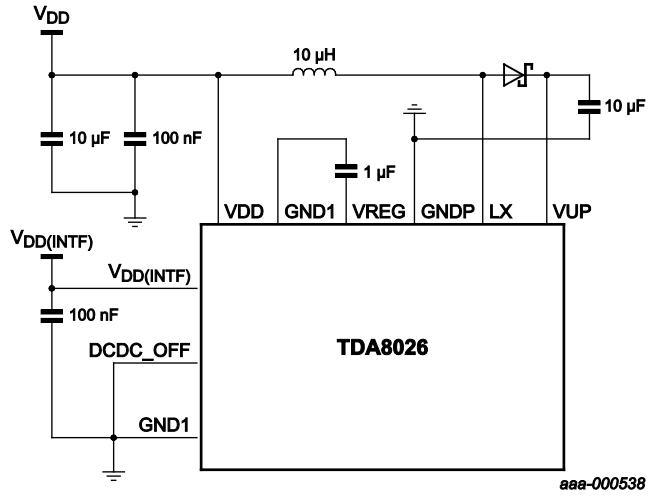


Fig 9. DC/DC Converter connections schematic

The **PRLL5817** schottky diode from NXP is recommended for this design.

3.3 Inductor choice

The recommended inductor for the DC/DC converter is a 10µH inductor from coilcraft:

Coilcraft MSS6132-103ML

If another inductor is used, the saturation current in accordance with its inductance value must be respected.

The following graphic helps to choose the inductor parameters:

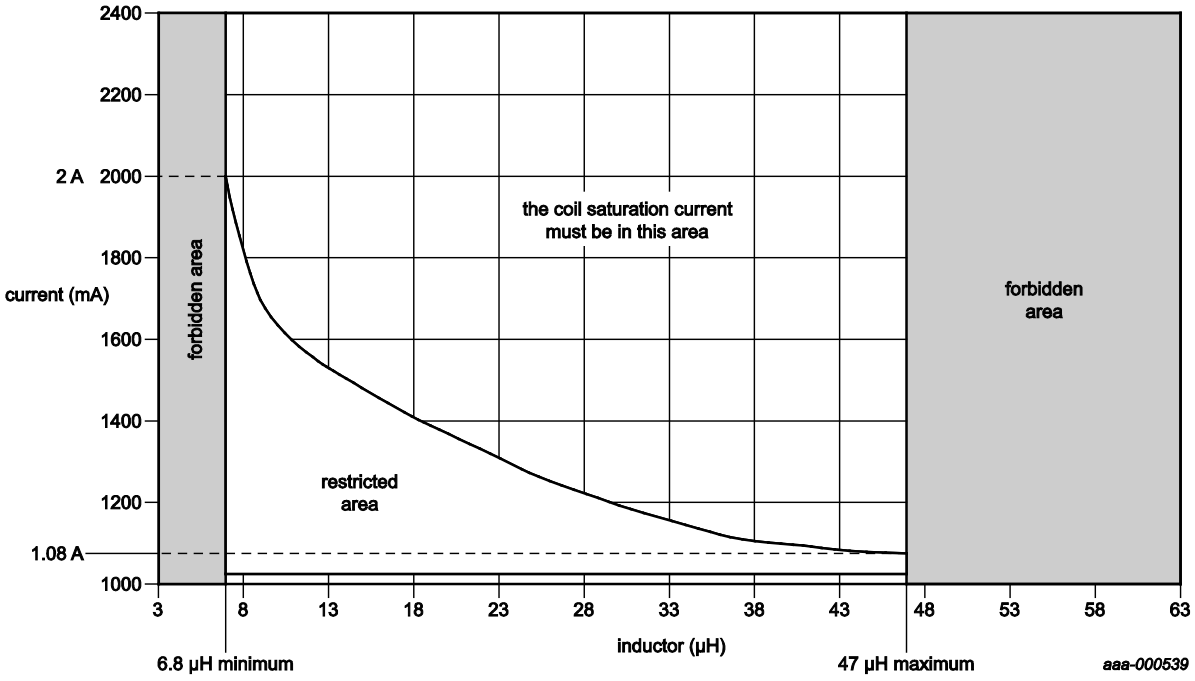


Fig 10. Inductor choice

The chosen inductor must respect this requirement: the saturation current which induces 30% inductance drop must be above the limit value.

3.4 Layout

The DC/DC converter components layout must be implemented respecting the following guidelines:

- The inductor must be placed close to the Lx pin
- The 10µF capacitor on VDD has to be routed close to the inductor and to the GNDP pin
- The 100nF on VDD must be placed close to the VDD pin
- The schottky diode must be placed close to the inductor
- The 10µF capacitor on Vup has to be placed close to Vup and GNDP.

For a layout example, refer to the evaluation board layout given in the UM10319 User Manual.

3.5 By-passing the DC/DC converter

The DC/DC converter can be bypassed if the power supply (VDD) is stable above 5.25V.

To configure the TDA8026, connect the DCDC_OFF pin to $V_{DD(INTF)}$ and connect the DC/DC converter pins as follows:

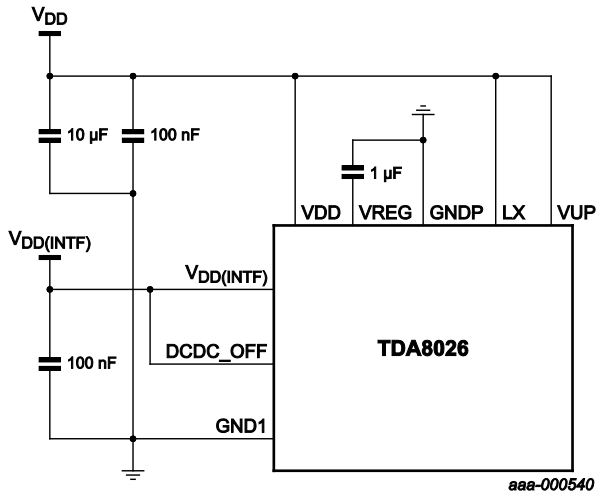
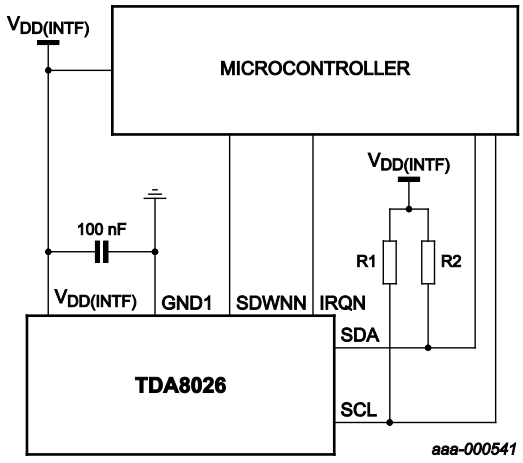


Fig 11. DC/DC converter bypassed – connections schematic

4. Host interface

4.1 Connection to the host

The following pins must be connected to the host for the TDA8026 to be driven properly.



(1) IOUC1, IOUC2, CLKIN1, CLKIN2 are connected to the host but not useful for the configuration.

Fig 12. Host connections schematic

4.2 I²C bus

The TDA8026 is accessed via its I²C bus. SDA is the bi-directional data line and SCL is the clock line.

The I²C bus can work with a frequency up to 400 kHz.

On each line of the I²C bus, a pull-up resistor to $V_{DD(INTF)}$ is needed. The value of this resistor depends on the speed of the bus.

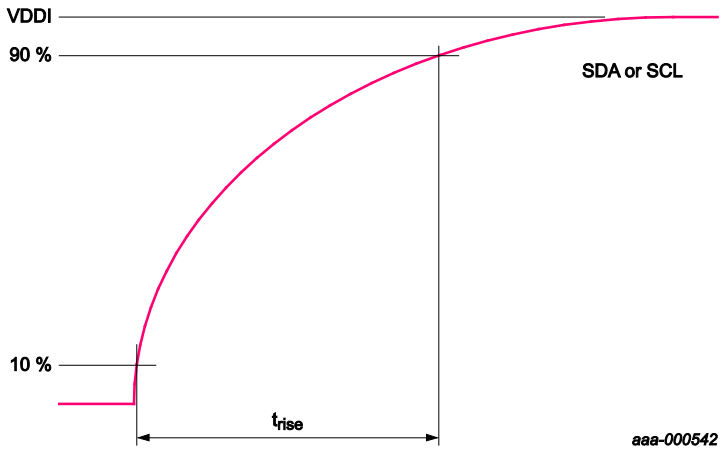


Fig 13. I²C bus rising time

The I²C standard requires a t_{rise} time lower than 300 ns for 400 kHz and 1000 ns for 100 kHz.

To achieve this time, a 1,5kΩ may be used as pull-up for 400 kHz. It allows to keep t_{rise} under 300 ns whatever the supply voltage is.

For a 100 kHz I²C bus, the resistor used may be 1kΩ per volt. For example, for $V_{DD(INTF)}$=3.3V, a pull-up resistor of 3.3kΩ is a good value.

4.2.1 Read / Write

In the following, the direction of the read or write operation is seen from the master point of view. E.g. a write operation represents a byte written in one of the TDA8026 registers. A read operation represents a byte read from a TDA8026 register.

The read and the write operations are described hereafter. For both operations, the principle is the same:

Start

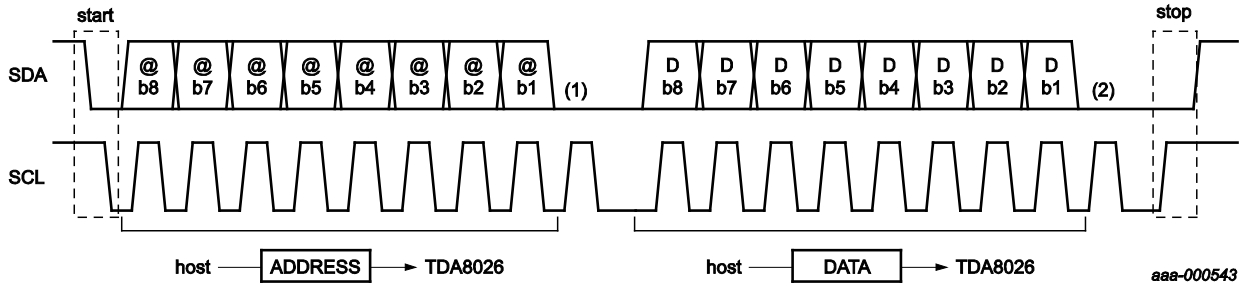
8 address bits

Address acknowledge (by the TDA8026)

8 data bits

Data acknowledge by the receiver. (This ACK is optional)

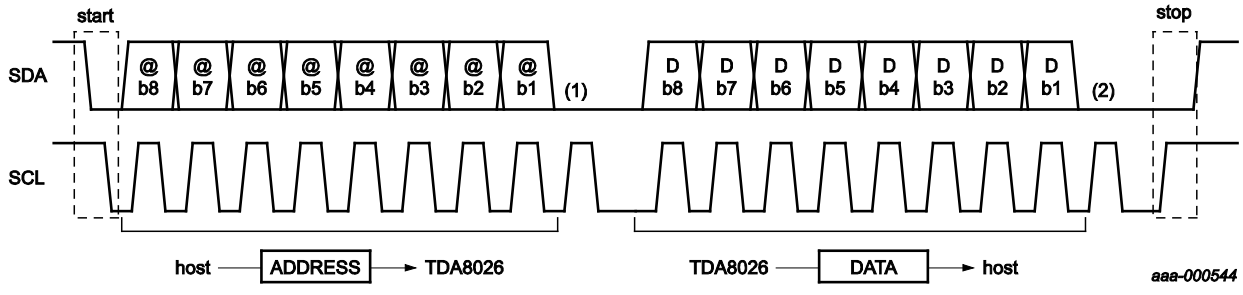
Stop



(1) Line is pulled low by the TDA8026 during the 9th clock pulse of the address byte: address acknowledge

(2) Line is pulled low by the TDA8026 during the 9th clock pulse of the written byte: data acknowledge

Fig 14. I²C Write operation



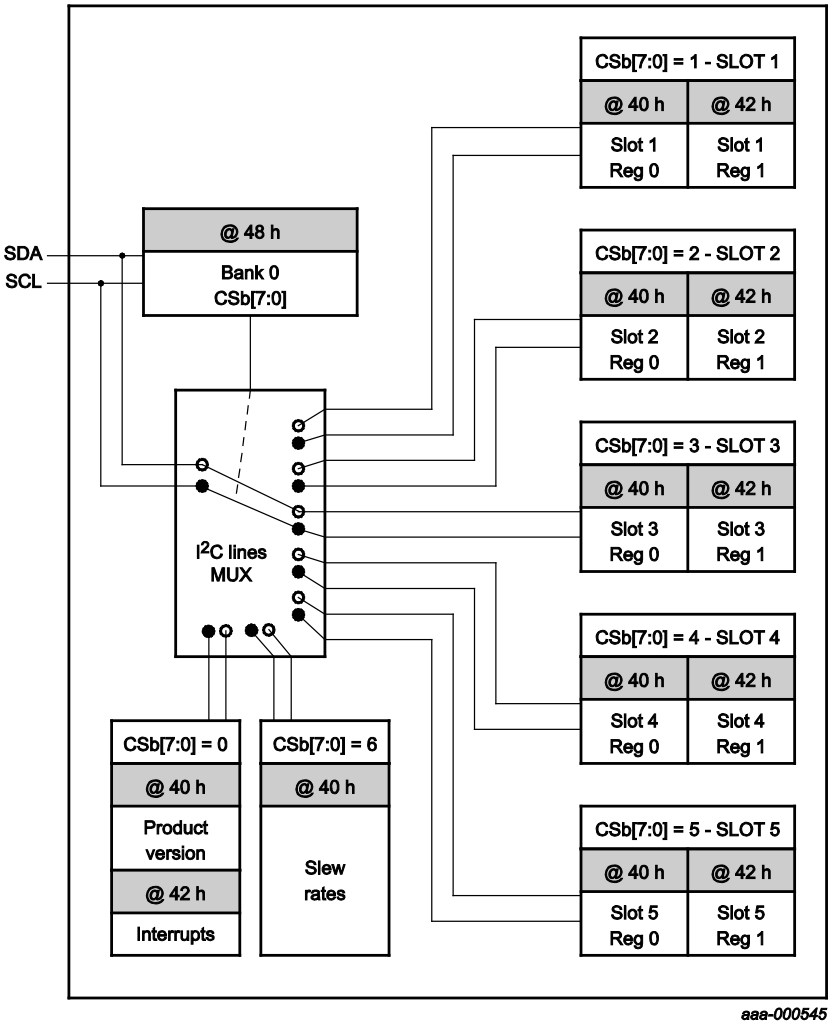
(1) Line is pulled low by the TDA8026 during the 9th clock pulse of the address byte: address acknowledge

(2) Line can eventually be pulled low by the host during the 9th clock pulse of the read byte as data acknowledge but this has no impact for the TDA

Fig 15. I²C read operation

4.2.2 Registers overview

The following drawing gives a symbolic view of the internal organization of the registers. The Bank0 registers is always accessed directly and selects the slot which will be accessed by the second addresses.



(1) The addresses are given for A0 = GND

Fig 16. I²C registers symbolic organization

The organization of the slot registers (When CSb[7:0] = 1 to 5) is described in Fig 17.

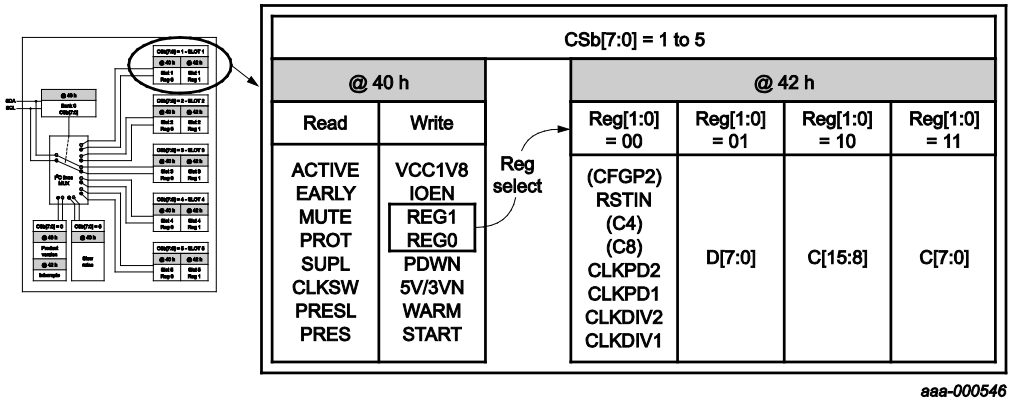


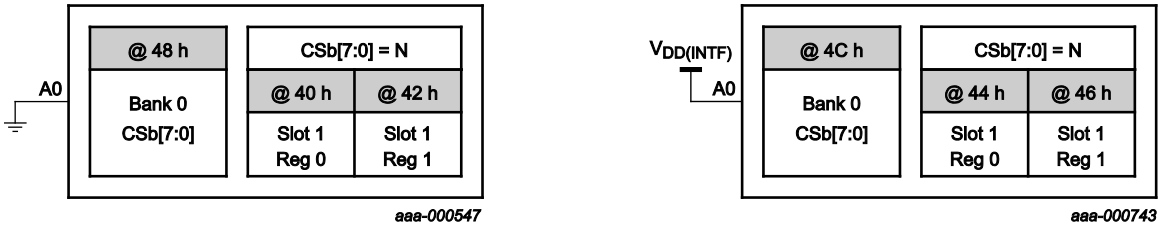
Fig 17. Slots specific registers

When there is a communication at address 42h, the accessed register is defined by the REG[1:0] value stored at address 40h.

For each slot, the register at address 40h cannot be read back. Then the microcontroller must know at any time the value stored in this register.

4.2.3 Addresses

The available addresses to access the TDA8026 depend on the A0 pin.



a. A0 = GND

b. A0 = $V_{DD(INTF)}$

Fig 18. I²C addresses regarding A0

4.2.4 Access examples

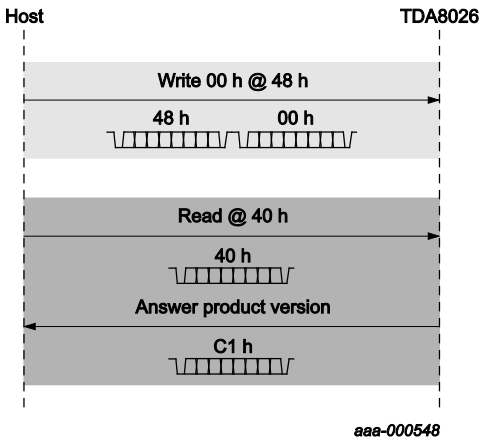
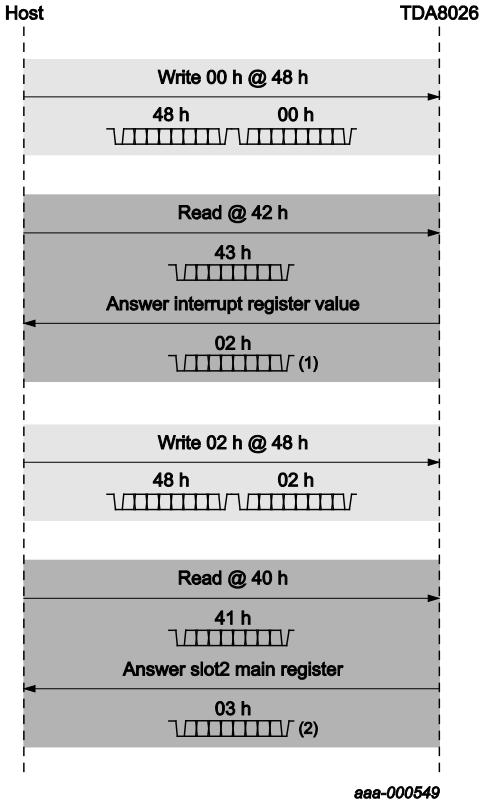


Fig 19. Access examples – Read product version

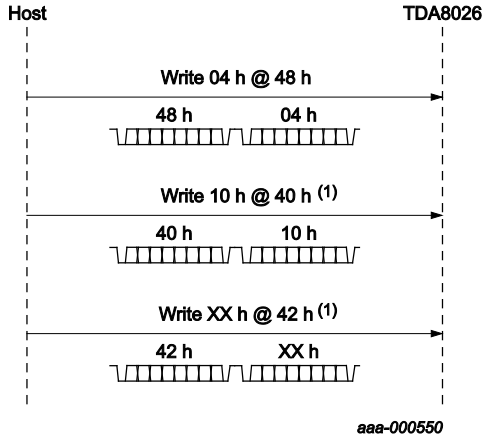
The next drawing gives an example of interrupt management when a card has been inserted in the smart card connector of the slot2



(1) The interrupt register inform about which slot number has an interrupt. Here, 02h means slot 2

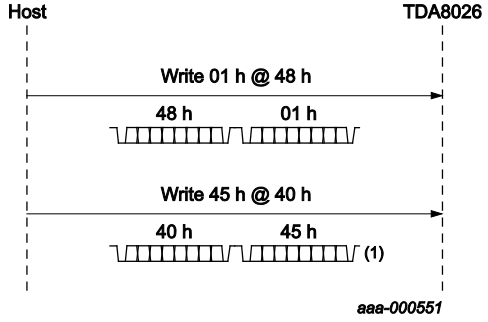
(2) PRESL is 1 because the bit PRES has changed and is now 1. It means that a card has been inserted

Fig 20. Access examples – Read an interrupt



(1) This access write the REG[1:0] value to select the register at @42h

Fig 21. Access examples – Change D[7:0] counter value for slot 4



(1) 45h: Enable I/O; Set 5V card and start activation

Fig 22. Access examples –Activate slot 1

4.3 Interrupt management

4.3.1 Slots 1 to 5

When the TDA8026 wants to warn the host that a specific event happened, it uses its IRQN line. This pin is an output of the TDA8026. When IRQN is pulled low by the TDA8026, the host shall read the cause of the interrupt.

The events that can cause an interrupt are:

EARLY: a smart card has answered too early after the reset rose, during activation

MUTE: a smart card has not answered after activation

PROT: an overload on a card slot or an overheating has been detected. An overload will cause a deactivation on the slot where it has been detected. An overheating will deactivate all the active smart cards.

SUPL: a supervisor has detected a drop-out on VDD or $V_{DD(INTF)}$. This will cause a deactivation of all slots.

PRESL: the corresponding presence pin has changed (PRES1 or PRES2). If the move is due to a card extraction while the card was active, an emergency deactivation occurs.

All these events except the last one can come from any card slot (Except PRESL for the slots 3 to 5). The next drawing describes the interrupt process when a card is inserted in slot 1.

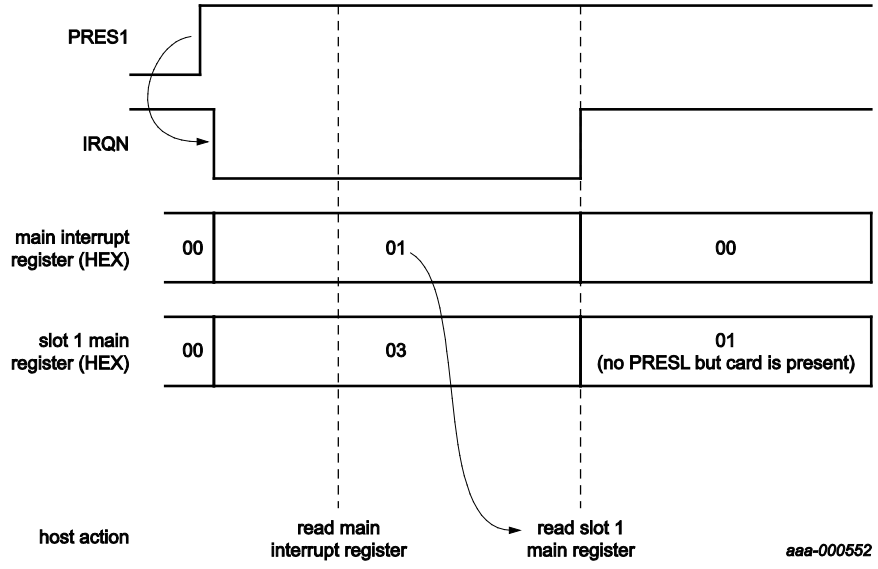


Fig 23. Interrupt process (example described: card insertion in slot 1)

4.3.2 Auxiliary interrupt

If the INTAUXN input is connected to an external device, a falling edge on this pin will cause an interrupt. It will be seen in the main interrupt register (bit 5) and will not be cleared until the interrupt has been cleared in the external device.

When this pin is used, it must be pulled-up with a 100k resistor to avoid any error when exiting the shutdown mode. When it is not used, it must be connected directly to $V_{DD(INTF)}$.

4.4 Functional shutdown mode

The shutdown mode can be entered at any time by releasing the SDWNN pin.

When in shutdown mode, the TDA8026 only monitors PRES1 and warns the host through the IRQN line as soon as there is an interrupt.

4.4.1 Exiting shutdown mode after an event

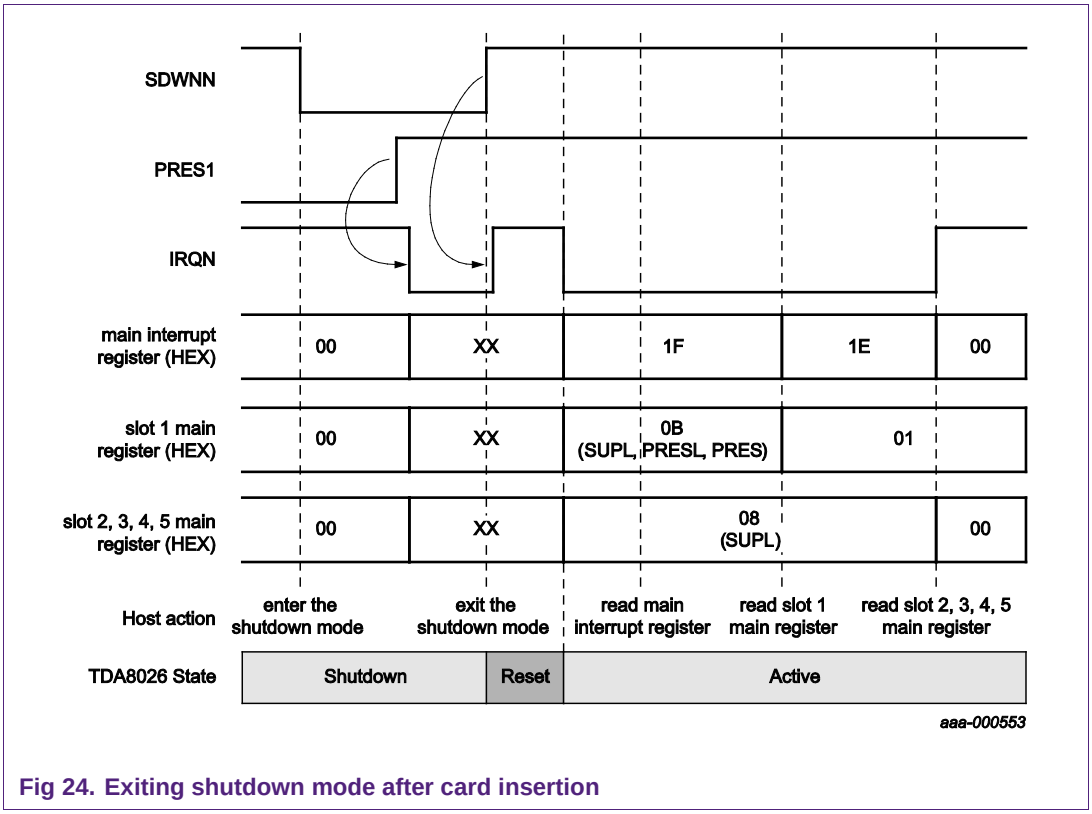


Fig 24. Exiting shutdown mode after card insertion

When SDWNN is set, the TDA8026 goes out of the shutdown mode. At this time all the registers are reset and have their default values.

The following events happen when exiting from the shutdown mode:

The TDA8026 resets all its registers to their default values

Each card slot's SUPL bit is set

The IRQN line is low

General Interrupts register is set to 1Fh (or 3Fh if INTAUXN is used and low, see chapter "Auxiliary Smart Card Reader")

4.4.2 Exiting shutdown mode with no event

It is possible to exit the shutdown mode, even without receiving a presence event.

This can be the case when the smart card is inserted but no access to the card is required. While waiting for an event on the host side, the TDA8026 can be set in shutdown mode to reduce the current consumption.

The TDA8026 can exit the shutdown mode at any time, just by setting high the SDWNN pin.

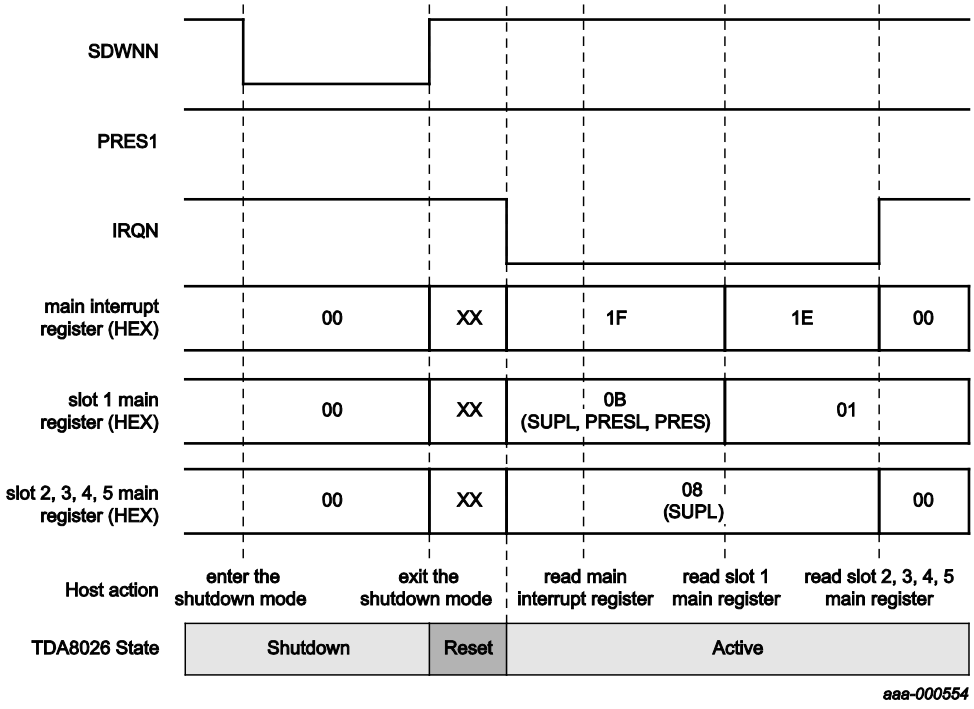


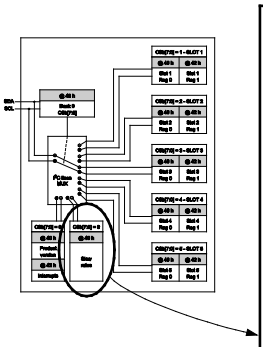
Fig 25. Exiting shutdown mode – General case

Exiting the shutdown mode, the sequence of event is exactly the same as before, as the state of the TDA8026 is the same after the reset sequence.

4.5 Slew rates

The falling and rising time of the CLK line as well as the falling time of the I/O line can be customized in order to achieve some high speeds or reduce the cross talk due to a too strong edge.

This can be done by the Slew Rate register: Register 6 of bank 1:



CSb[7:0] = 6		
@ 40 h Read/Write		
Bit	Description	Default value
7	CLK Slew Rate — Slot 2 - 5	01
6		
5	I/O Slew Rate — Slot 2 - 5	00
4		
3	CLK Slew Rate — Slot 1	01
2		
1	I/O Slew Rate — Slot 1	00
0		

aaa-000555

Fig 26. Slew rate register - description

The default value of the Slew Rate register is 44h.

The slew rate value of the CLK and I/O line of the slots 2 to 5 are identical as they share the same bits.

The slot 1 slew rate values can be customized independently.

The slew rate corresponds to the rising or the falling time of the edge between 10% and 90% of the value as described on the next pictures:

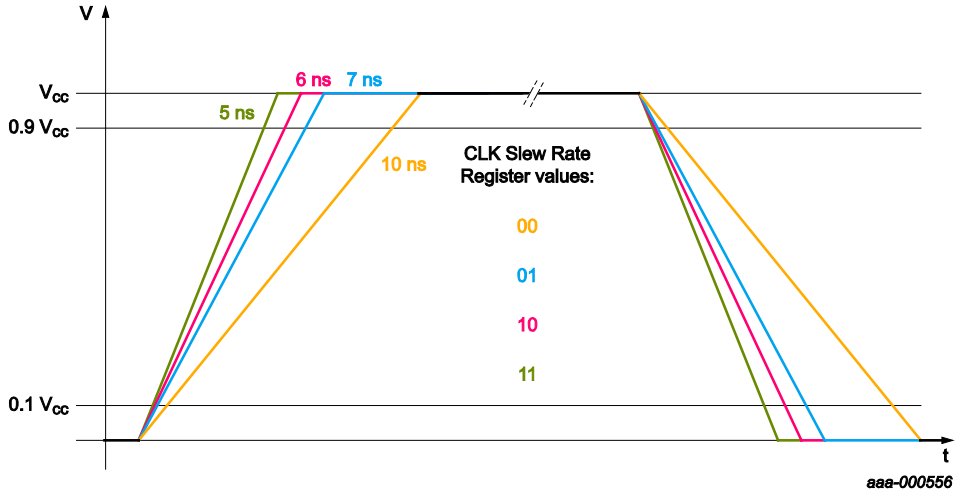


Fig 27. CLK Slew rate

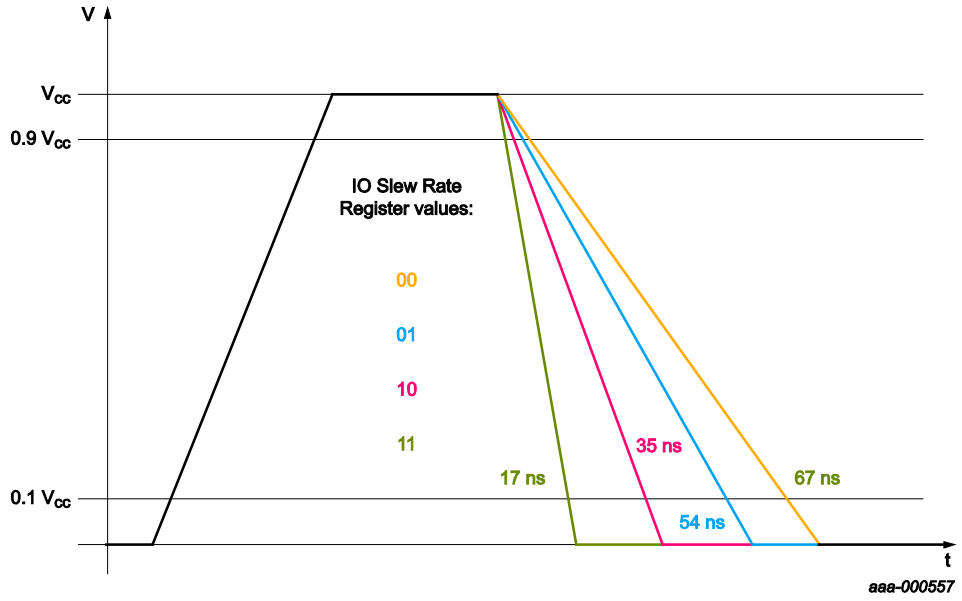


Fig 28. I/O Slew rate

5. Card connector

5.1 Presence

5.1.1 Polarity

5.1.1.1 PRES1

The slot 1 presence pin input polarity can be chosen thanks to the SPRES pin. When SPRES is tied to GND, the PRES1 input is active high. When SPRES is connected to $V_{DD(INTF)}$, the PRES1 pin is active low.

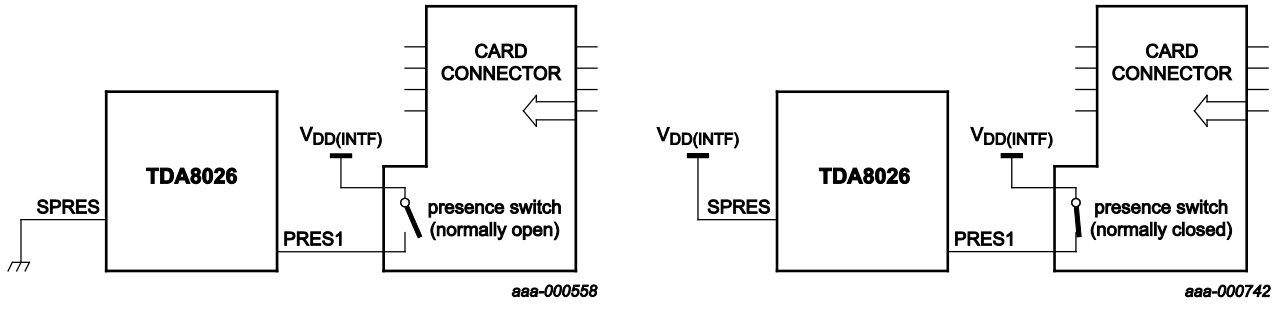
The PRES1 pin has an internal pull-down current source. Therefore, when the pin is unconnected, a low signal is seen.

When the pin is active high (SPRES = GND), if PRES1 is open, the card is assumed to be absent. When the pin is active low (SPRES = $V_{DD(INTF)}$), if PRES1 is open, the card is seen present.

This behavior allows to use two card connectors type: normally open or normally closed.

A normally open card connector must be used with SPRES = GND, PRES1 active high. A normally closed must be used with PRES1 active low and SPRES = $V_{DD(INTF)}$.

The way to use these two configurations is summarized in Fig 29.



a. Normally open presence switch

b. Normally closed presence switch

Fig 29. Slot1 - PRES card connection

5.1.1.2 PRES2

For the slot 2, the presence behavior is managed by SPRES and by an internal bit: CFGP2. The CFGP2 bit is used to invert the SPRES polarity **for PRES2 only**.

When CFGP2 = 0, PRES2 has the same behavior as PRES1 (depending on SPRES)

When CFGP2 = 1, PRES2 behavior is inverted compared to PRES1.

Table 1 summarizes the 4 possibilities, depending on the type of smart card connector presence switch used for slot 1 and slot 2.

Table 1. Presence behavior configuration

Slot 1 Card connector type	Slot 2 Card connector type	SPRES	CFGP2	PRES1	PRES2
Normally open	Normally open	GND	0	Active high	Active high
Normally closed	Normally open	$V_{DD(INTF)}$	1	Active low	Active high
Normally open	Normally closed	GND	1	Active high	Active low
Normally closed	Normally closed	$V_{DD(INTF)}$	0	Active low	Active low

5.1.1.3 Slots 3/4/5

For the slots 3, 4 and 5, there is not the same presence detection. These slots are assumed to be used for Secure Access Modules, with smart card always present or always absent.

If the card connector has a presence switch, it can be connected to an input called STAP3/4/5 respectively (STAP means STAtus Presence). This input does not behave as PRES1 or PRES2. Its value is only copied in the corresponding slot register PRES bit.

Due to this behavior, there will never be any interrupt when the card is inserted or extracted. It implies that **the SAM card must never be removed during a card session.** The extraction would not be detected and the card can be damaged.

The STAP input is always active high.

5.1.2 Debouncing

With some smart card connectors, when a card is inserted, the following signal can be seen on the PRES signal:

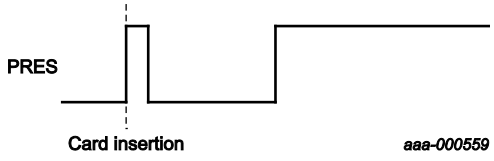


Fig 30. Bouncing on PRES pin

This could cause three interrupts sent to the host by the TDA8026. Some microcontrollers do not support this behavior.

That's why a debouncing feature has been integrated in the TDA8026. It allows to wait several ms after the last rising edge on PRES to assume that the card has been inserted.

As described in Fig 31, a counter is started when a rising edge is detected on the PRES pin, and reset when PRES becomes low. If the counter reaches its given timeout, the card is assumed to be present.

The length of the deboucning counter depends on the internal frequency. Its typical value is around 15 ms.

There is no debouncing for card extraction. The deactivation must start at the first falling edge on the PRES pin.

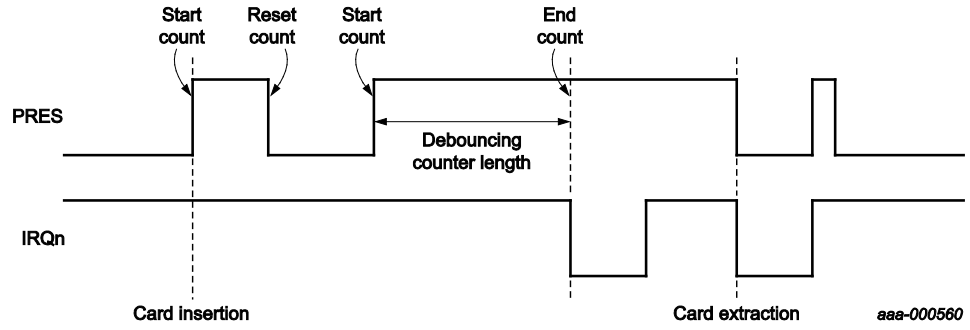


Fig 31. PRES debouncing principle

5.2 VCC capacitors

To connect the smart card connector to the TDA, only two capacitors are mandatory as external components. The schematic reference is given in Fig 32 for slot 1. The principle is the same for the other slots.

The C1 capacitor must be placed near the TDA8026 and C2 must be connected close to the card connector.

The advised values for C1 and C2 are respectively 100nF for C1 and 100nF or 220nF for C2.

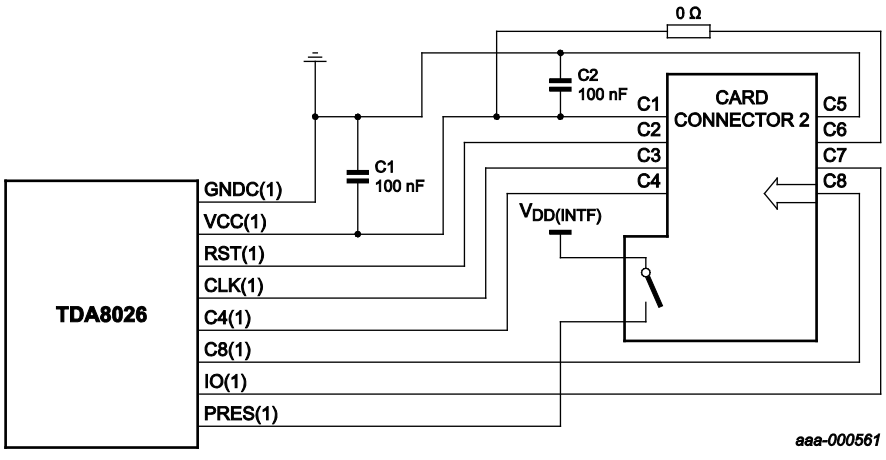


Fig 32. Slot 1 card connector schematic reference

5.3 Schematics

For the slot 1, the pins C4 and C8 of the card connector (connected to pins C41 and C81 of the TDA8026) are optional. They can be left unconnected unless some specific operation using these pins is required.

It is not advised to leave pin VPP (C6) unconnected. It can be connected directly to VCC or GND in accordance with latest ISO 7816 standards. Connecting it to VCC allows it to be compliant with older cards which might not support VPP connected to the Ground.

For more flexibility, the design should include a 0 ohm serial resistor between VPP and VCC. Then the application can be easily adapted.

Fig 33 shows the reference schematic to use with slot 2 and slot 3/4/5 (represented by slot 4)

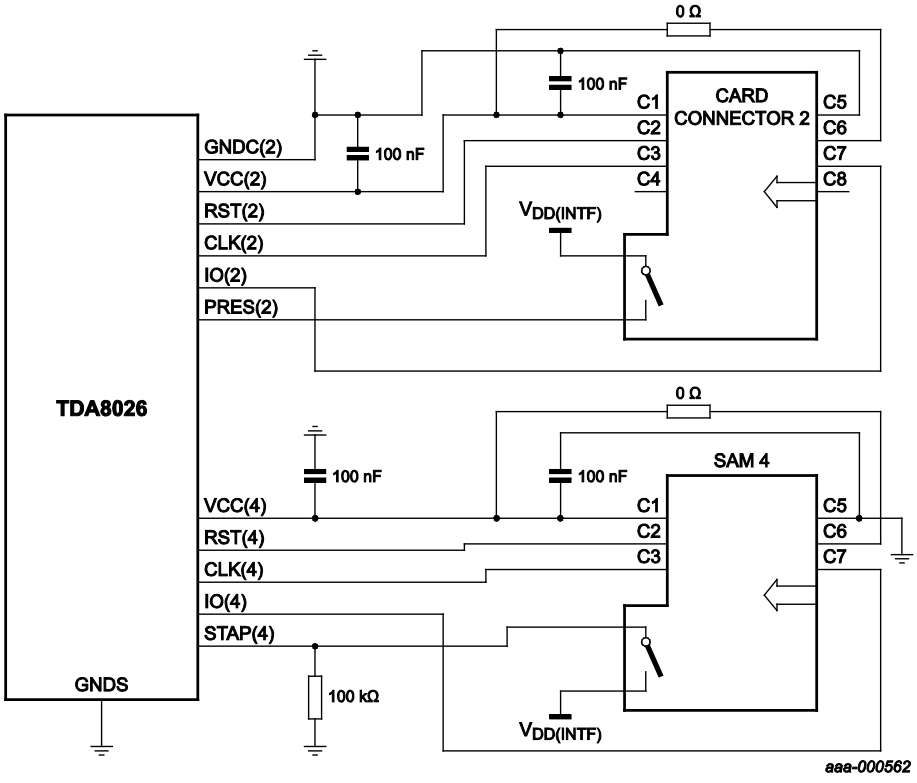


Fig 33. Slot 2, Slot 3/4/5 card connector schematic reference

6. Card operation

6.1 I/OUC – CLKIN

6.1.1 Multiplexed signals

The TDA8026 has two pairs of signals I/OUC and CLKIN:

I/OUC1 and CLKIN1 are dedicated to the slot 1

I/OUC2 and CLKIN2 are dedicated to the other slots: 2, 3, 4 and 5

The CLKIN signal is an input for the TDA8026. Then the same frequency on CLKIN2 can be used for all slots at the same time.

The I/OUC line is bidirectional. Therefore only one I/O slot can be accessed at the same time. That's the role of the I/OEN bit.

Fig 34 symbolizes the multiplexing of CLKIN2 and I/OUC2, controlled by the I/OEN bits.

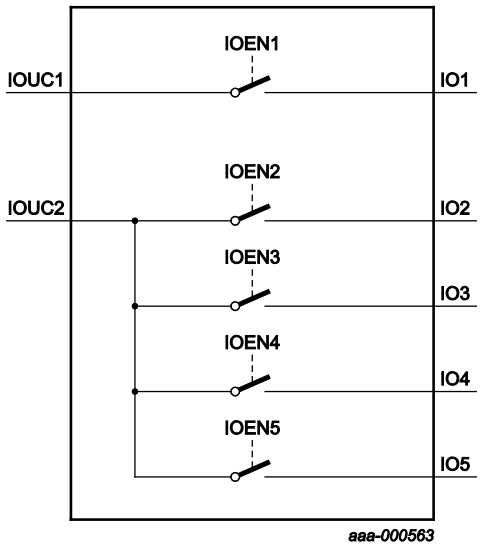
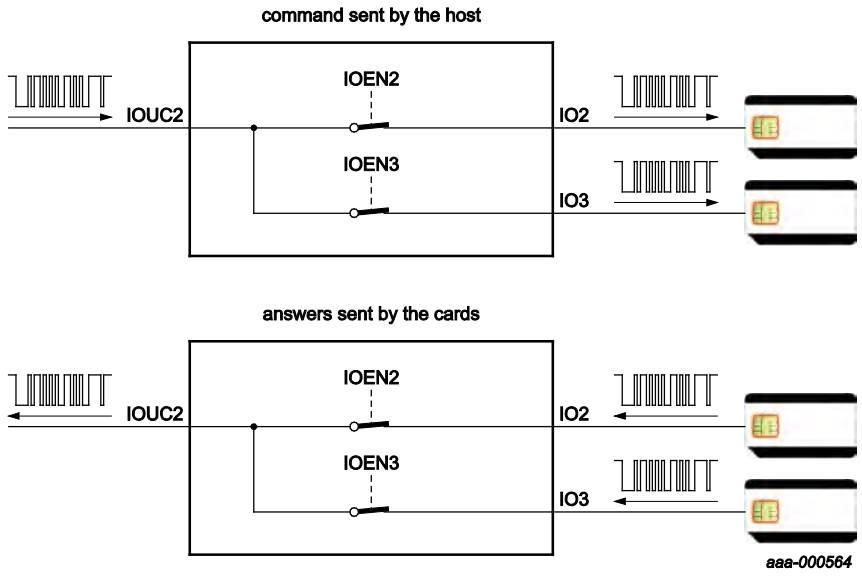


Fig 34. I/OUC distribution

When more than one slot is activated at the same time, the host must always take care to activate only one I/O line at the same time. If not, a conflict will occur when two cards will receive the same command and try to answer on the same line, as shown in Fig 35.

When such a conflict occurs, the data sent by the TDA8026 to the host does not represent any of the answer from the card.



(1) To avoid this conflict, no more than one I/OEN bit must be set at any time

Fig 35. I/OUC2 conflict example

6.1.2 Merge slot signals

The two pairs of signals I/OUC and CLKIN allow to access slot 1 at the same time as another slot, whereas it is not possible to access for example slot 3 and slot 4 at the same time, as they share the same I/OUC signal.

But to perform this double access (slot 1 + another slot), it is mandatory to have a host which is able to drive two ISO 7816 lines.

As this does not represent the majority of the cases, it is possible to connect I/OUC1 with I/OUC2, and CLKIN1 with CLKIN2. In this case, the TDA8026 behaves as if there was only one I/OUC line and one CLKIN line for 5 slots.

In this case, the host must be careful to share correctly the I/O line as described in chapter 6.1.1 Multiplexed signals.

6.2 Card configuration

The 5 slots can be accessed through their specific registers as described in Fig 17.

Prior to access a slot register, the slot must be selected by writing its number in the TDA8026 main register (@48h)

Then the selected slot can be accessed and configured with its own parameters: voltage level and clock frequency (as a division of CLKIN).

For the voltage level, two bits allow to choose between 5V, 3V or 1.8V. These bits are in the main register of each slot (@40h in write mode): if bit 7 called VCC1V8 is set, then the card voltage will be 1.8V. Otherwise, the bit 2 (5V/3VN) choose the card voltage. 5V if 5V/3VN is set, 3V if not set.

As this register is also used to activate the card, the voltage level can be selected when the card is activated. See the activation chapter (6.3) for more details.

The clock division can be selected at the slot's second address (@42h with reg[1:0]=00).

6.3 Activation

For each slot, one bit setting is enough to activate the smart card. Setting the bit START (bit 0) in the slot's main register (@40h) have the TDA8026 activates the card with the normalized sequence, and checks for the ATR reception timings.

When activating a card, the I/OEN bit must be set in order to receive the ATR, and the voltage level must be selected. The following table gives the value to write in the main register to activate a card.

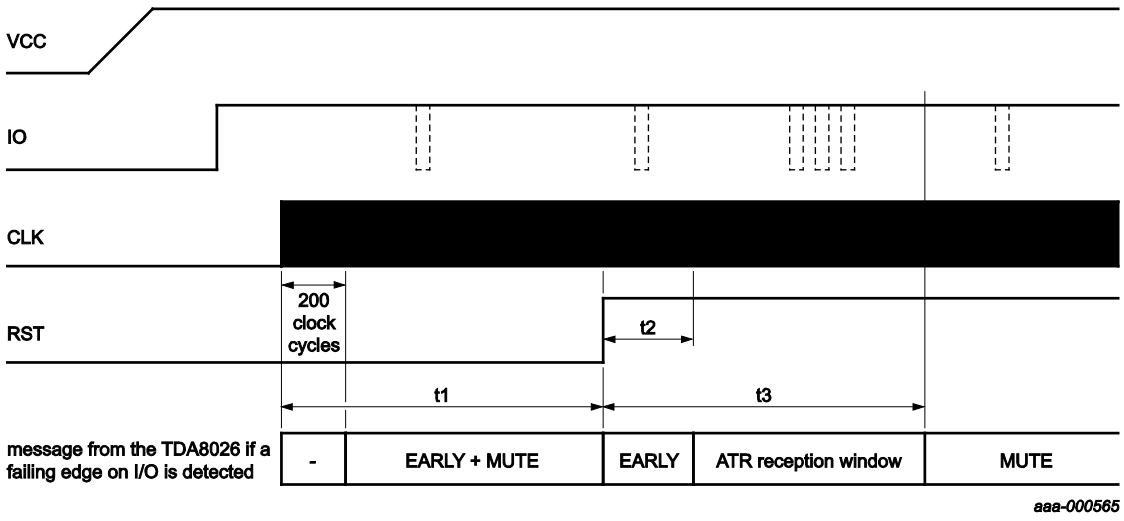
Table 2. @40h write for card activation

Smart card voltage level	@40h value to write
1.8V	C1h
3V	41h
5V	45h

The VCC voltage level can not be changed when the card is activated. This means that even if the @40h register value is changed, the VCC voltage level will stay the same.

6.4 ATR

When the TDA8026 activates a card, it checks the timings for the ATR reception. The timings described in Fig 36 are monitored by the TDA8026.



(1) t1 is always equal to t3

Fig 36. ATR timings

When a delay is not within the specification, the TDA8026 does not deactivate the card but send an interrupt and set its corresponding bit.

In case of a smart card that is not within the specification, it is possible to force the acceptation by changing the allowed timings. This can be done by the registers accessible at address 42h for each slot.

Table 3 gives the correspondence between the timing described in Fig 36and the counter value in the slots registers.

Table 3. ATR counters value

Time	Value	Default (decimal)	Unit
t1 = t3	C[15:0]	42100	Clock cycles (based on card clock)
t2	200+D[7:0]	370	Clock cycles (based on card clock)

6.5 Warm reset

To perform a warm reset, the action is almost the same as activation, but the WARM bit is to set instead of the START bit.

The value to write to the register is then the same with WARM bit set. For example, the value for activation at 5V is 45h; it becomes 47h for a warm reset at 5V.

The MUTE bit must be reset (read) before performing a warm reset. Otherwise, WARM bit is reset by MUTE bit and the warm reset is not achieved.

6.6 APDU exchange

The TDA8026 monitors some normalized parameters in the case of an ATR reception, but not for an APDU exchange.

During exchange of data between the host and the smart card, the TDA8026 only behaves as a level shifter. The data are referenced to $V_{DD(INTF)}$ on I/OUC line while they are referenced to VCC on the card I/O line.

6.7 Deactivation

The deactivation is managed entirely by the TDA8026 sequencer. There are two ways to start a deactivation: normal deactivation performed by the host or emergency deactivation on behalf of the TDA8026.

6.7.1 Normal deactivation

To deactivate the card, the host only needs to clear the START bit. Then an automatic deactivation is performed by the TDA8026.

6.7.2 Emergency deactivation

Deactivation occurs when one of the following events happens:

Card removal

Overheating

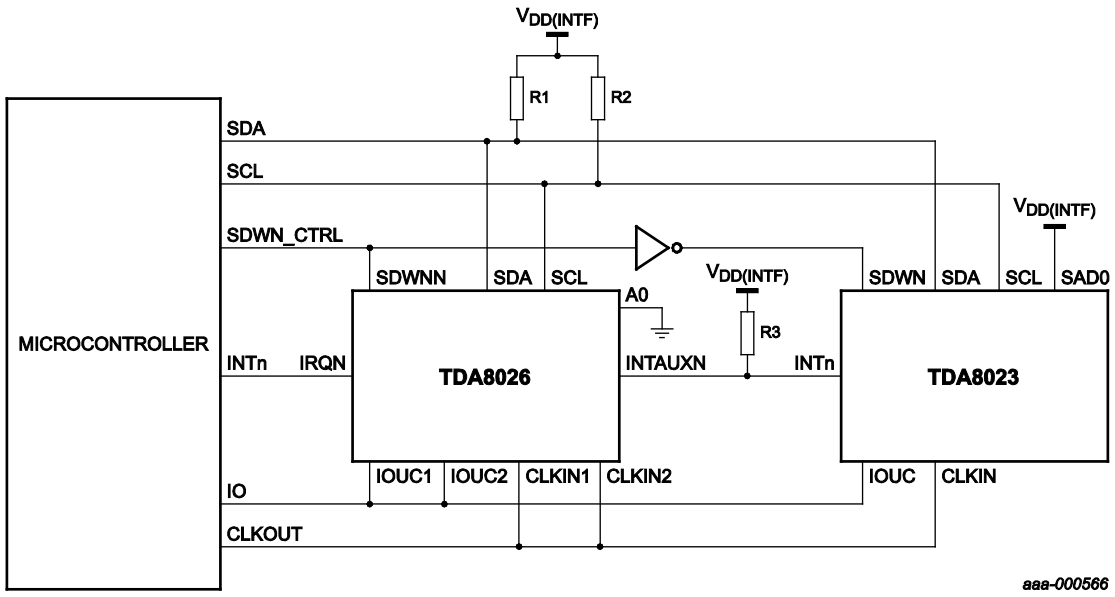
Short-circuit or high current on VCC

VDD or $V_{DD(INTF)}$ drop

7. 6 slots reader

It is possible to add simply an extra smart card interface to the TDA8026.

A TDA8023 can be connected to the TDA8026 as follows:



(1) Only the TDA8023's pins needed for the interface are presented on this schematic. For a complete schematic refer to the TDA8023 datasheet and application note

Fig 37. TDA8023 + TDA8026 association

This association is seen by the host as a 6 slots interface.

The output interrupt of the TDA8023 is connected to the TDA8026 INTAUXN input, and is handled by the TDA8026 as described in the interrupt chapter (auxiliary interrupt).

As the TDA8026 as the same set of register for 1 slot as the TDA8023, it is really easy to adapt the TDA8026 driver to access the TDA8023.

The only difference is the I²C address. In the above schematic, the TDA8023 is accessed with addresses 44h and 46h instead of 40h and 42h.

8. EMV Certification

8.1 Layout

The TDA8026 is compliant with the electrical EMV standards and a design based on this smart card reader should pass the EMV certification without external components on IO RST or CLK lines.

However, some parameters like the allowed ripple level on the card signals hardly depend on the layout. To maintain the ripple in the limit conditions, the following guidelines must be respected for the layout:

- Short and low resistive lines between the TDA8026 and the Smart Card connector
- Shielded clock line: this line is mostly responsible for the noise seen on IO, VCC and RST.
- The clock line must also be drawn far from other sensitive signals (IO, RST, VCC)
- Optimized DCDC layout: Good ground connections, short tracks… The DCDC can generate noise on the whole design when functioning, due to the current pulses.

A DC/DC converter layout example is given with the evaluation board User Manual: UM10319.

8.2 Clock slew rates

If the design does not allow a good shielding of the CLK line or if the noise seen during the electrical tests is above the accepted limit (this can be due to the smart card probe, or the tester probe with long lines…), it is possible to lower the impact of the Clock on the noise.

This can be done simply by increasing the rising and falling times of the clock signal.

To increase this time, the slew rates of the clock have to be changed to the lowest one: Slew Rate register = xxxx00xxb (refer to chapter 4.5)

9. Hardware Update

9.1 Change from version C2 to C3

End of 2015, EMVCo introduced a new Analog test suite, following the EMVCo 4.3 specifications. This new test suite now implements a Vil test on I/O line, corresponding to the EMVCo 4.3 specifications: The I/O Vil must be set to 0.2 x VCC at maximum.

For TDA8026/C2, the margin with this new limit on VIL is very narrow depending on production batches (close to 1V for Vcc=5V) and a hardware upgrade has been done to avoid any issue during EMVCo certification; new part numbers have been created.

The Hardware change modifies the Vil of TDA8026. It was set to 0.8V max in TDA8026/C2 version, and is now set to 1V max in TDA8026/C3 version.

The TDA8026/C3 version can be used as a direct replacement of TDA8026/C2 without any other change on the application, either SW or HW.

Note: as only the analog part has been changed in the IC, the digital part remains the same. For this reason the Product Version is still “C2” even in C3 version.

The TDA8026/C3 version can be used as a direct replacement of TDA8026/C2 without any other change on the application, either SW or HW.

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