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Differences between Philips 4-channel SC16C devices and Philips low power SC16CxxxB devices

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Document information

Info	Content
Keywords	UART, IrDA, Serial communications, connectivity, RS-232
Abstract	This application note details the differences between Philips four-channel SC16Cxxx devices and Philips low power SC16CxxxB devices. Revision B devices can be identified by the letter B attached at the end of the part number. For example, SC16C654**B** or SC16C754**B**.

PHILIPS

Revision history

Rev	Date	Description
1	20040826	Application note, initial version (9397 750 13348).

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1. Differences between SC16C554 and SC16C554B, SC16C554D and SC16C554DB

Table 1: Differences between SC16C554 and SC16C554B, SC16C554D and SC16C554DB

SC16C554, SC16C554D	SC16C554B, SC16C554DB
Has a register called EFR. The following features are supported: auto hardware flow control using EFR bit 7 and bit 6, auto software flow control, special character select, sleep mode, XOFF interrupt, CTS and RTS interrupt, IrDA.	EFR register was removed. The following features are not supported: auto hardware flow control using EFR bit 7 and bit 6, auto software flow control, special character select, sleep mode, XOFF interrupt, CTS and RTS interrupt, IrDA.
Cannot read ISR register when LSR bit 7 is '1'.	ISR register can be read when LSR bit 7 is '1' or '0'.
Clearing of the transmit empty interrupt requires a read of the ISR register and a write to TXFIFO.	Transmit empty interrupt can be cleared by reading of the ISR or a write to TXFIFO.
Does not support hardware flow control using MCR bit 5.	Support hardware flow control using MCR bit 5.
Timeout interrupt cannot be disabled with data still in the RXFIFO.	Timeout interrupt can be disabled with data in the RXFIFO.
In non-interrupt mode for LSR register to report break condition correctly the software must read ISR and LSR.	In non-interrupt mode LSR will report break condition correctly; software does not need to read ISR.
In non-interrupt mode for LSR register to report parity error correctly the software must read ISR and LSR.	In non-interrupt mode LSR will report parity error correctly; software does not need to read ISR.
In non-interrupt mode for LSR register to report framing error correctly the software must read ISR and LSR.	In non-interrupt mode LSR will report framing error correctly; software does not need to read ISR.
In FIFO mode (FCR = 0x01) and receive ready interrupt is enabled, once a character is received by the UART the software must read the LSR register first, prior to reading the receive FIFO. If the software reads just the receive FIFO, then interrupt signal will remain active (logic 1).	Software can just read the receive FIFO without having to read the LSR register.
Maximum baud rate depends on the width of the write pulse (see data sheet under timing table footnote).	Maximum baud rate does not depend on the width of the write pulse.
C1 and C2 (see Figure 7 of the data sheet) recommended values are 47 pF and 100 pF.	C1 and C2 (see Figure 11 of the data sheet) recommended values are 22 pF and 33 pF.
In DMA mode 0 the delay between back-to-back writes must be greater than X1 clock period, otherwise, the transmitter will at times miss sending out a character.	This condition is no longer applicable.
Reset signal is synchronized to X1 clock.	Reset signal is not synchronized to X1 clock.
Non-5 V tolerant pins (Intel mode): $\overline{CSB}$, $\overline{CTSB}$, $\overline{DSRB}$, $\overline{CDB}$, $\overline{RIB}$, RXB, A1, A0, $\overline{DSRC}$, RXD, INTSEL. Non-5 V tolerant pins (Motorola mode): A3, $\overline{CTSB}$, $\overline{DSRB}$, $\overline{CDB}$, $\overline{RIB}$, RXB, A1, A0, $\overline{DSRC}$, RXD.	All input pins are 5 V tolerant.
Sleep Current: 1.0 mA	Not supported.

2. Differences between SC16C654 and SC16C654B, SC16C654D and SC16C654DB

Table 2: Differences between SC16C654 and SC16C654B, SC16C654D and SC16C654DB

SC16C654, SC16C654D		SC16C654B, SC16C654DB	
This UART only supports single XON/XOFF sequence.		Supports double XON/XOFF, as well as single XON/XOFF sequence.	
Cannot read ISR register when LSR bit 7 is '1'.		ISR register can be read when LSR bit 7 is '1' or '0'.	
Clearing of the transmit empty interrupt requires a read of the ISR register and a write to TXFIFO.		Transmit empty interrupt can be cleared by reading of the ISR or a write to TXFIFO.	
The software must fill up the transmit FIFO to transmit trigger level in one bit time, otherwise, the UART might give multiple transmit empty interrupts. This is due to the fact that the UART evaluates transmit FIFO empty condition after the start bit is sent, and if the data in the FIFO is still below the trigger level, the UART will keep generating interrupts.		The software has one character time to fill up the transmit FIFO to transmit trigger level. The UART now evaluates the transmit FIFO empty condition after the stop bit is sent and the transmit empty interrupt is only generated once—the first time the number of bytes in the transmit FIFO falls below the trigger level.	
The $\overline{\text{TXRDY}}$ pin state follows the transmit trigger level, that is, it goes HIGH once the transmit FIFO is full, and goes LOW if the data in the FIFO is below the trigger level.		Once transmit FIFO is full, the $\overline{\text{TXRDY}}$ pin goes HIGH, and it goes LOW as soon as one byte is sent.	
Timeout interrupt cannot be disabled with data still in the RXFIFO		Timeout interrupt can be disabled with data in the RXFIFO.	
Interrupt signal on TX empty $1 \rightarrow 0$	Interrupt signal on TX empty $0 \rightarrow 1$	Interrupt signal on TX empty $1 \rightarrow 0$	Interrupt signal on TX empty $0 \rightarrow 1$
1	8	8	7
1	16	16	15
1	32	32	31
1	56	56	55
(bytes in TXFIFO)	(bytes in TXFIFO)	(bytes in TXFIFO)	(bytes in TXFIFO)
In non-interrupt mode, for LSR register to report break condition correctly the software must read ISR and LSR.		In non-interrupt mode, LSR will report break condition correctly; software does not need to read ISR.	
In non-interrupt mode, for LSR register to report parity error correctly the software must read ISR and LSR.		In non-interrupt mode, LSR will report parity error correctly; software does not need to read ISR.	
In non-interrupt mode, for LSR register to report framing error correctly the software must read ISR and LSR.		In non-interrupt mode, LSR will report framing error correctly; software does not need to read ISR.	
In FIFO mode (FCR = 0x01) and receive ready interrupt is enabled, once a character is received by the UART the software must read the LSR register first prior to reading the receive FIFO. If the software reads just the receive FIFO, then interrupt signal will remain active (logic 1).		Software can just read the receive FIFO without having to read the LSR register.	
Maximum baud rate depends on the width of the write pulse (see data sheet under timing table footnote).		Maximum baud rate does not depend on the width of the write pulse.	
C1 and C2 (see Figure 6 of the data sheet) used to be 22 pF and 33 pF; the new recommended values are 47 pF and 100 pF.		C1 and C2 recommended values are 22 pF and 33 pF.	
In DMA mode 0 the delay between back-to-back writes must be greater than X1 clock period, otherwise, the transmitter sometimes will miss sending out a character.		This restriction is no longer applicable.	

Table 2: Differences between SC16C654 and SC16C654B, SC16C654D and SC16C654DB *…continued*

SC16C654, SC16C654D	SC16C654B, SC16C654DB
Reset signal is synchronized to X1 clock.	Reset signal is not synchronized to X1 clock.
Non-5 V tolerant pins (Intel mode): $\overline{CSB}$, $\overline{CTSB}$, $\overline{DSRB}$, $\overline{CDB}$, $\overline{RIB}$, RXB, A1, A0, $\overline{DSRC}$, RXD, INTSEL. Non-5 V tolerant pins (Motorola mode): A3, $\overline{CTSB}$, $\overline{DSRB}$, $\overline{CDB}$, $\overline{RIB}$, RXB, A1, A0, $\overline{DSRC}$, RXD.	All input pins are 5 V tolerant.
Sleep current: 1.0 mA	Sleep current: 50 μA

3. Differences between SC16C754 and SC16C754B

Table 3: Differences between SC16C754 and SC16C754B

SC16C754	SC16C754B
This UART only supports single XON/XOFF sequence.	Supports double and single XON/XOFF sequence.
Cannot read ISR register when LSR bit 7 is a '1'.	ISR register can be read when LSR bit 7 is '1' or '0'.
Clearing of the transmit empty interrupt requires a read of the ISR register and a write to TXFIFO.	Transmit empty interrupt can be cleared by reading of the ISR or a write to TXFIFO.
The software must fill up the transmit FIFO to transmit trigger level in one bit time, otherwise, the UART might give multiple transmit empty interrupts. This is due to the fact that the UART evaluates transmit FIFO empty condition after the start bit is sent, and if the data in the FIFO is still below the trigger level, the UART will keep generating interrupts.	The software has one character time to fill up the transmit FIFO to transmit trigger level. The UART now evaluates the transmit FIFO empty condition after the stop bit is sent and the transmit empty interrupt is only generated once—the first time the number of bytes in the transmit FIFO falls below the trigger level.
Timeout interrupt cannot be disabled with data still in the RXFIFO.	Timeout interrupt can be disabled with data in the RXFIFO.
In non-interrupt mode, for LSR register to report break condition correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report break condition correctly; software does not need to read ISR.
In non-interrupt mode, for LSR register to report parity error correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report parity error correctly; software does not need to read ISR.
In non-interrupt mode, for LSR register to report framing error correctly the software must read ISR and LSR.	In non-interrupt mode, LSR will report framing error correctly; software does not need to read ISR.
In FIFO mode (FCR = 0x01) and receive ready interrupt is enabled, once a character is received by the UART the software must read the LSR register first—prior to reading the receive FIFO. If the software reads just the receive FIFO, then interrupt signal will remain active (logic 1).	Software can just read the receive FIFO without having to read the LSR register.
Maximum baud rate depends on the width of the write pulse (see data sheet under timing table footnote).	Maximum baud rate does not depend on the width of the write pulse.
C1 and C2 (see Figure 13 of the data sheet) recommended values are 47 pF and 100 pF.	C1 and C2 recommended values are 22 pF and 33 pF.
In DMA mode 0, the delay between back-to-back writes must be greater than X1 clock period, otherwise, the transmitter sometimes will miss sending out a character.	This condition is no longer applicable.
RX FIFO and TX FIFO status bits in the FIFO Rdy register do not work correctly.	RX FIFO and TX FIFO status bits in the FIFO Rdy register now work correctly.
If TCR register is used for hardware or software flow control, FCR[7:4] must be set to a value other than 0xC.	This restriction is no longer applicable.
Reset signal is synchronized to X1 clock.	Reset signal is not synchronized to X1 clock.
Non-5 V tolerant pins: $\overline{CSB}$, $\overline{CTSB}$, $\overline{DSRB}$, $\overline{CDB}$, $\overline{RIB}$, RXB, A1, A0, $\overline{DSRC}$, RXD, INTSEL.	All input pins are 5 V tolerant.
Sleep current: 1.0 mA	Sleep current: 50 µA

4. What you need to know if you plan to switch from Philips SC16Cxxx/SC16CxxxD to SC16CxxxB/SC16CxxxDB device

Table 4: Guideline for switching from SC16Cxxx to lower power SC16CxxxB devices

Function	Part number	Package	Recommended part number	Comment
554	SC16C554	A68 (PLCC68) B64 (LQFP64)	SC16C554B or SC16C654B	If you are using the following features: HW flow control, SW flow control, or IrDA, you need to replace the SC16C554 with SC16C654B.
554D	SC16C554D	B64 (LQFP64)	SC16C554DB or SC16C654DB	If you are using the following features: HW flow control, SW flow control, or IrDA, you need to replace the SC16C554D with SC16C654DB.
654	SC16C654	A68 (PLCC68) B64 (LQFP64)	SC16C654B	Backwards compatible to SC16C654.[1]
654D	SC16C654D	B64 (LQFP64)	SC16C654DB	Backwards compatible to SC16C654D.[1]
754	SC16C754	A68 (PLCC68) B80 (LQFP80)	SC16C754B	Backwards compatible to SC16C754.

[1] In very rare occasions, the TXRDY pin is used. If that is the case, a software modification is required.

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6. Contents

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