High-performance Dual Core Processor

MPC8641D

Not Recommended for New Designs

This page contains information on a product that is not recommended for new designs.

Last Updated: Oct 17, 2022

MPC8641 device is "Not recommended for new designs", please use the replacement families Power Architecture (T208x), Arm Architecture (LS2044).

The MPC8641D uses two high-performance superscalar e600 cores running at up to 1.5 GHz. This three-issue machine has a compact 7-stage pipeline which is particularly efficient with code that branches unpredictably. It avoids the extensive delays associated with flushing a long pipeline on mispredicted branches . Unpredictable branching is typical of code paths driven by largely random arrival of different types of packets. These processors support up to 8 out-of-order instructions on the system bus that allows for making forward progress even while waiting for previous instructions to finish (ie, access to main memory required). The e600 has an on-board 128-bit vector processor for efficient data movement (useful for copying TCP payloads from kernel space to user space) and for math functions that rival a DSP.

With a large backside L2 cache for each core, the e600 benefits from high bandwidth and low latency between the processor and the L2 cache. With each core having its own L2 cache, it can be particularly efficient when the two cores are running separate operating systems and data sharing is limited. For applications that do share data between cores, low latency data sharing features are also present.

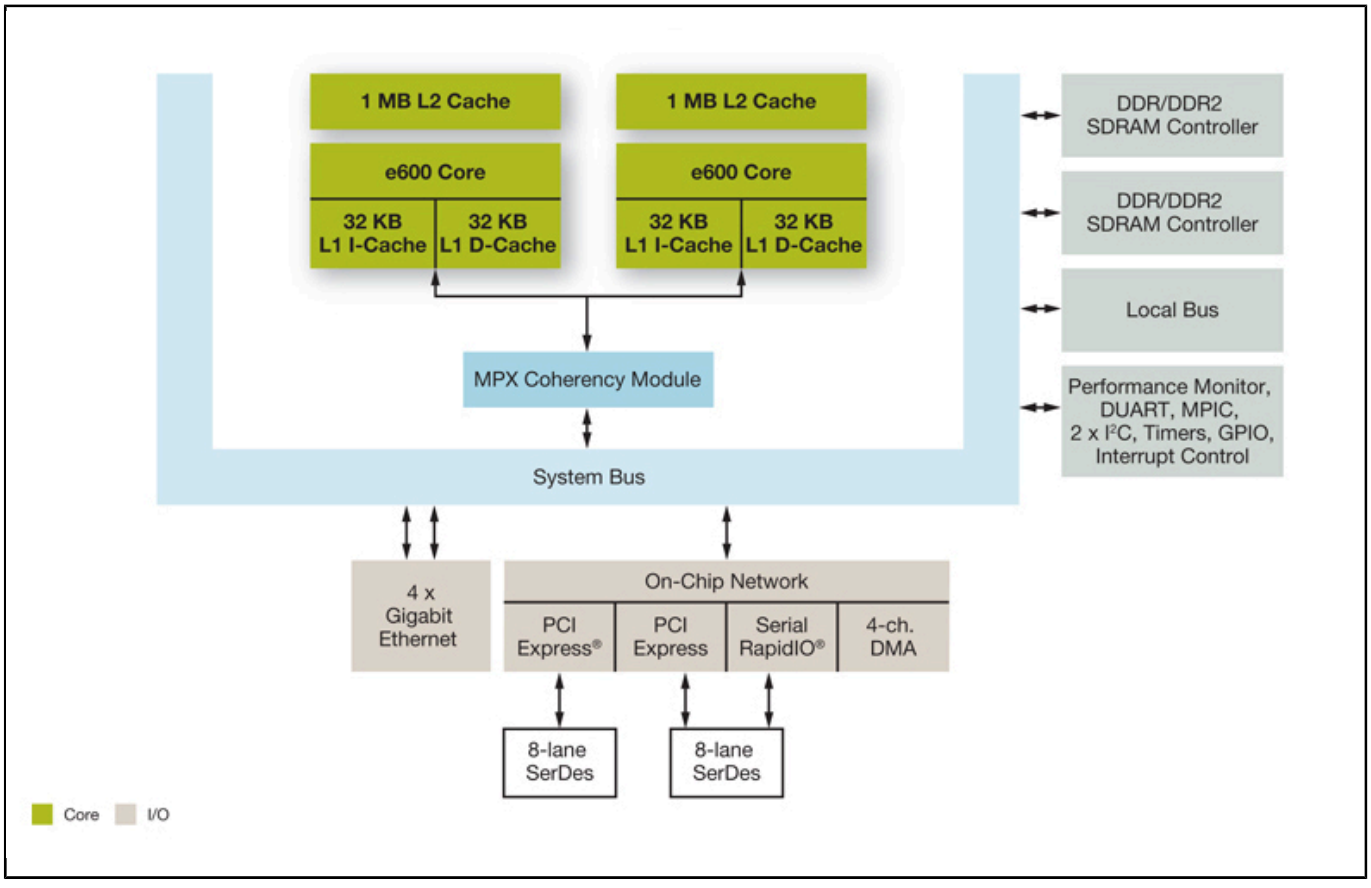
The device has dual 64 bit (72b with ECC) DDR2 memory controllers to match the bandwidth requirements of the two cores. The memory controllers can be assigned to each core for increased OS isolation, or can be shared between the cores to ensure the most efficient usage of the memory bandwidth. Accesses can be interleaved across both memory controllers, reducing the average latency to memory by increasing the number of open pages in a target memory region. Error correction codes implementing single error correction and double error detection can be optionally enabled to ensure that bit errors on the memory controller interface are corrected or at least reported to the cores. This is a requirement for any high-availability application.

There are two flexible high-performance I/O ports. Dual 8-lane PCI Express ports leverage PCI legacy with a high-performance serial point-to-point link that is commonly used to connect to a variety of other on-board high-performance devices. The 4-lane serial RapidIO port, with its low software overhead, configuration simplicity, hardware error correction, and support for both memory mapped and packet-based transactions, is very well suited as a backplane interface.

There are four Ethernet controllers, supporting 10 Mbps, 100 Mbps, and 1000 Mbps. The Ethernet controllers have advanced capabilities for TCP and UPD checksum acceleration, QoS support, and packet header manipulation. Each Ethernet controller can be converted into a FIFO mode for high-efficiency ASIC connectivity.

The MPC8641D supports flexible software implementations: symmetric multiprocessing (SMP) and Asymmetric multiprocessing. With SMP, one operating system runs on both cores, but from a programming perspective, it appears that the developer is writing a program for a single core. With Asymmetric multiprocessing, two instances of the same operating system or two entirely separate operating systems can be run on the two cores, largely unaware of each other.

MPC8641D Block Diagram Block Diagram



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Note: The information on this document is subject to change without notice.